INSTRUCTIONS

1. Please check to ensure that you have a complete exam booklet. There are 22 numbered problems. Note that Problem 2 occupies 2 pages, Problem 8 occupies 2 pages, Problem 12 occupies 2 pages, Problem 22 occupies 2 pages. Including the cover sheet, you should have 27 pages. There should be no blank pages in the booklet.

2. The examination is closed book and closed notes. No reference material is allowed at your desk. A calculator is permitted.

3. All wireless devices must be turned off for the entire duration of the exam.

4. You may work a problem directly on the problem statement (if there is room) or on blank sheets of paper available from the exam proctor. Do not write on the back side of any sheet.

5. Your examination code number MUST APPEAR ON EVERY SHEET. This includes this cover sheet, the problem statement sheets, and any additional work sheets you turn in. DO NOT write your name on any of these sheets. Use the preprinted numbers whenever possible, or WRITE LEGIBLY!!!

6. Under the rules of the examination, you must choose 8 problems to be handed in for grading. Each problem to be graded should be separated from the rest of the materials, stapled to the associated worksheets, and placed on the top of the appropriate envelope in the front of the exam room. DO NOT TURN IN ANY SHEETS FOR THE OTHER 14 PROBLEMS!!

7. The examination lasts 4 hours, from 9:30 AM to 1:30 PM EST.

8. When you hand in the exam:

   (a) Separate the 8 problems to be graded as explained above.
   (b) Check to see that your Code Number is in EVERY sheet you are turning in.
   (c) On the section at the bottom of this page, CIRCLE the problem numbers that you are turning in for grading.
   (d) Turn in this cover sheet (containing your code number) and the 8 problems to be graded.
   (e) All other material is to be placed in the discard box at the front of the room. You are not allowed to take any of the exam booklet pages from the room!
A. (3 points) A function F(A,B,C,D) is defined by the Karnaugh map below (x = “don’t care”). List ALL of the prime implicants of this function in algebraic form and circle them in the map. For each prime implicant, circle “ess” if it is an essential prime implicant of this function. (You may not need all of the lines.)

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Prime implicants:

- ________ ess
- ________ ess
- ________ ess
- ________ ess
- ________ ess
- ________ ess

B. (1 point) Write a minimal sum-of-products (SOP) expression for this function.

\[
F(A, B, C, D) = \text{(expression)}
\]

C. (3 points) In the space below, draw the schematic diagram for a MINIMAL circuit implementing F(A,B,C,D) using only NAND gates and INVERTERs. Assume that input variables are available only in uncomplemented form.

D. (3 points) In the space below, draw the schematic diagram for a MINIMAL circuit implementing F(A,B,C,D) using only NOR gates and INVERTERs. Assume that input variables are available only in uncomplemented form. A copy of the Karnaugh is provided for your optional use.
Problem 2 (Core: DSP - ECE 2026)  
Code Number: __________

**PROBLEM**

The block diagram above defines a system for discrete-time filtering of continuous-time signals.  
*Note: all parts of this question can be worked independently.*

(a) Suppose that the discrete-time LTI system is a bandpass filter whose (causal) finite-length impulse response has the following form:

\[ h[n] = \begin{cases} 
0 & n < 0 \\
e^{0.6\pi n} & 0 \leq n \leq 9 \\
0 & n > 9 
\end{cases} \]

and whose frequency response magnitude \( |H(e^{j\omega})| \) is shown below.

Determine all the poles and zeros of the system. Give your answer as **pole-zero plot** plot.  
Label carefully the locations of the poles and zeros; also note multiplicities if appropriate.
(b) Suppose that a different system function for the LTI system is

\[ H(z) = \frac{10z^{-3} - 5z^{-4}}{4 + 3z^{-1}} \]

Determine the output \( y[n] \) when the input signal is

\[ x[n] = 7(0.5)^n u[n] \]

Simplify your answer as much as possible.

\[ y[n] = \text{[Your Solution Here]} \]
Consider a doubly linked list that is implemented using the following `struct` definitions.

```c
typedef struct node_t {
    int data;
    struct node_t* prev;
    struct node_t* next;
} Node;

typedef struct dll_t {
    struct node_t* head;
    struct node_t* tail;
} DLList;
```

**Part A.** Suppose the C function `Find_Node` takes an integer `k` and a pointer to a sorted doubly linked list `dll` which might be empty. Its nodes are sorted in order of increasing `data` values. Complete the function to efficiently search `dll` for a node with `k` as its `data` value (use the fact that it is sorted). Return a pointer to that node if found or return `NULL` otherwise.

```c
Node* Find_Node(int k, DLList* dll){
```

**Part B.** Complete the procedure `Delete_Node` below which takes a pointer to a `Node` (which may be `NULL`) and deletes it from the doubly linked list `dll`, deallocating the node’s memory. Be sure to update the `head` and `tail` of `dll` if necessary. Also, be sure to guard against dangling pointers.

```c
void Delete_Node(Node* n, DLList* dll){
```
Problem: For the resistor, $R$, in the following figure,

i) find its resistance such that it consumes the maximum power;

ii) find the maximum power consumed by the resistor, $R$. 

\[ \text{Diagram of a circuit with } 1 \text{ A source, } 2 \Omega \text{ resistors, and } R. \]
A transmission line system has a DC source voltage $V_s = 10\, \text{V}$, $R_g = 20\, \Omega$, $Z_0 = 100\, \Omega$, and $R_l = 1800\, \Omega$.

(a) If the uncharged line is suddenly connected to the source, what is the initial power expended by the DC source?

(b) What is the power expended by the DC source upon reaching the steady state when $t \to \infty$?

(c) Where did the extra power go?

(d) If a transmission line fans out to $N$ identical lines in parallel, each having the same characteristic impedance $Z_0$ as the primary line, the reflection coefficient at the end of the primary line is ______.
Consider a DRAM circuit.

a. Draw a schematic for a 1-transistor DRAM cell and associated bit line.

b. Draw the voltages of all relevant signals during a read operation in which the cell stores a low value.

c. The cell capacitance is $C_{cell} = 10 \text{ fF}$ and the bit line capacitance is $C_{bit} = 25 \text{ fF}$. The bit line is charged to 1V and the cell is charged to 0V. How much will the bit line voltage dip during the read operation?
The figure depicts the current density of one carrier type in a forward biased silicon pn junction versus position. The total current density is also shown. The currents and positions are drawn to scale.

a) Identify the carrier type of the depicted (dotted line) current density
Explain

b) Accurately sketch the current due to the other carrier type
Explain

c) What is the approximate ratio of dopant concentrations, \( N_A/N_D \)?
Explain

d) For the diffusion coefficients, is \( L_n > L_p \)?
Explain

e) Sketch the conduction band minimum \( E_c \) and valence band maximum \( E_v \) vs. position for a forward biased pn diode. Include the Quasi Fermi levels vs. position for both electrons and holes.
Consider the incomplete full-wave rectifier circuit below, with a 60 Hz 120V RMS source connected to the transformer’s primary winding. You may assume that $R_{Load}$ is 50 Ohms, and that the ripple is negligible. You may also assume that all 4 diodes are identical, and their I/V characteristic follows the ideal diode equation with an ideality factor of 1. It is also known that the voltage delivered to the load is at most 1.5 Volts less than the peak voltage which appears across the secondary winding of the transformer. The ambient temperature is 300K.

a) Observing the proper polarities, draw the missing diodes, D1, D2, D3 and D4 in the schematic above to complete the circuit.

b) What is the ratio of the number of turns on the primary winding of the transformer to the number of turns on the secondary?

c) The saturation current of diodes D1 through D4 is AT LEAST / AT MOST (circle one) how many Amps? Provide a numerical answer in addition to circling the correct inequality.
d) The breakdown voltage of diodes D1 through D4 must necessarily be AT LEAST / AT MOST (circle one) how many Volts? Provide a numerical answer in addition to circling the correct inequality.
Assume a single cycle non-pipelined implementation of a processor that operates at a clock frequency of 100 MHz (clock time of 10 ns). Your job is to convert this design into a five stage pipelined implementation. You are considering two designs: M1 and M2. Shown below are the critical paths for each of the five stages for these two designs.

**M1**

- Fetch (2.5ns)
- Dec (2.4ns)
- AG/EX (2.4ns)
- MEM (2.5ns)
- WB (2.2ns)

**M2**

- Fetch (2ns)
- Dec (2ns)
- AG/EX (3ns)
- MEM (2ns)
- WB (2ns)

a) What is the maximum clock frequency at which M1 can operate correctly?

b) What is the maximum clock frequency at which M2 can operate correctly?

c) Which design would you recommend for highest performance?

d) For the recommended design, what is the expected speedup compared to the non pipelined implementation. Assume that the Instructions Per Cycle (IPC) of the pipelined machine is 0.75.
Problem 10 (Core: POWER - ECE 3072)  

A 3 phase 7.5 kV rms (line-neutral) 60 hertz source feeds two balanced three phase loads, an induction motor rated at 1 MW @ 0.9 PF, and the second a delta connected load with impedances shown.

a) Calculate the current and power factor at the source under steady state conditions.

b) Find the value of a wye connected capacitor C in microfarads needed to realize unity power factor at the source (power factor compensated case)

c) Find the percentage reduction in line losses, measured upstream of the capacitor, under normal and power factor compensated conditions.

d) If the motor draws 6X of the normal operating current at start-up with a power factor of 0.4, how much real power does the motor consume at start-up?
Problem 11 (Core: DSP/TLCOM - ECE 3077)   Code Number: __________

**PROBLEM**

For this problem it will be helpful to recall that an exponential random variable \( X \sim \text{Exp}(\lambda) \) with rate parameter \( \lambda > 0 \) has a probability density function (PDF) given by

\[
f_X(x) = \begin{cases} 
\lambda e^{-\lambda x} & x \geq 0, \\
0 & x < 0.
\end{cases}
\]

A room is lit by two light bulbs. Let \( A \) and \( B \) be random variables that denote the lifetimes of these two light bulbs (in units of days). Assume that \( A \sim \text{Exp}\left(\frac{1}{3}\right) \), that \( B \sim \text{Exp}(1) \), and that \( A \) and \( B \) are independent of each other.

1. What is the probability that light bulb “A” lasts longer than light bulb “B”? In other words, what is \( P[B < A] \)?

2. Let \( Z = \max(A, B) \) be the amount of time until both light bulbs burn out and the room goes dark. What is the probability that \( Z \leq 2 \)?

3. Again letting \( Z = \max(A, B) \), what is the expected value \( E[Z] \)?

4. You visit the room after 2 days to find both bulbs still lit, and again after 4 days to find that only bulb \( B \) has burned out. Given this information, what is the probability that bulb \( B \) lasted at least 3 days?
(a) Find the Fourier transform of $x(t)$. (5 points)
(b) Now consider the periodic signal $y(t)$ with a period of $T_0 = 6$ seconds. Find the Fourier series coefficients $a_k$ of $y(t)$. (5 points)
Consider the design of a full adder cell for a ripple carry adder in standard static CMOS style. All gates should be sized for equal worst case rise and fall times. Delay should be calculated in units of \( \tau = R_n C_{\text{inv}} \), where \( R_n \) is the equivalent resistance of a minimum sized nFET \( (W = W_{\text{min}} \text{ and } L = L_{\text{min}}) \), and \( C_{\text{inv}} = 3 C_{\text{fet}} \) is the input capacitance of a minimum sized inverter with equal rise and fall times. Note that we are assuming that the transconductance ratio of identically sized nFET to pFET \( \beta_n / \beta_p = 2 \). Also, assume that the parasitic delay of a minimum sized inverter \( p_{\text{inv}} = \tau \). You may wish to use the method of logical effort to solve this problem.

(a) (2) Write the equations for the full adder sum \( s_i \) and carry out \( c_{i+1} \) in terms of inputs \( a_i, b_i \) and \( c_i \)

(b) (2) Design and draw two alternative implementations of \( c_{i+1} \) using
   (i) 3 NAND2 gates and 1 NAND3 gate, and (ii) 2 NAND2 gates and 1 OAI21 gate. (Hint: factor a term).

(c) (6) Size each circuit in (b) for minimum delay in a ripple carry adder. In each case size the first stage of logic as small as feasible given the design rules, and minimize the load from any logic that is not on the critical path. Calculate the per bit delay on the critical path for each circuit. Note that you may leave sizes in terms of input capacitance.
A 6-pole, 230-V (L-L), 60 Hz, Y-connected stator, three phase induction motor has the following parameters on a per phase basis, all referred to the stator side:

- Stator resistance = 0.5 ohm
- Stator leakage reactance = 0.75 ohm
- Rotor resistance referred to stator side = 0.25 ohm
- Rotor leakage reactance referred to stator side = 0.5 ohm
- Core loss equivalent resistance referred to the stator side = 500 ohm
- Magnetizing current is small enough to be neglected.
- Neglect mechanical losses.

Use the approximate equivalent circuit for the motor, which has the core loss resistance across the input terminals to the circuit. Draw the circuit, insert your symbols, and then determine the efficiency of the motor at its rated slip of 2.5%.
Analyze the following feedback circuit. Assume the op-amp is ideal with infinite voltage gain, infinite bandwidth, infinite input impedance, and zero output impedance. The op-amp is powered by ±25V. The diode D1 is an ideal diode with turn-on voltage of 0.7V. The NMOS MOSFET M1 has its device parameters as $K' = 25 \mu A/V^2$, $W/L = 40 \mu m/1 \mu m$, and $V_{TN} = 0.5V$.

Recall that for a MOSFET in saturation $I_D = \left( \frac{K'}{2} \right) \left( \frac{W}{L} \right) (V_{GS} - V_{TN})^2 = \left( \frac{K'}{2} \right) \left( \frac{W}{L} \right) (V_{od})^2$, while for a MOSFET in triode $I_D = K' \left( \frac{W}{L} \right) [V_{od} \times V_{DS} - \left( \frac{V_{DS}}{2} \right)^2]$, where $V_{od} = V_{GS} - V_{TN}$.

Neglect the channel-length-modulation and body-effect of the MOSFET transistor. Use the constant voltage drop model for the diode. Please answer the following questions.

1. Label the op-amp Plus “+” and Minus “-” inputs to ensure a negative feedback.

2. Assume the input voltage $0 < V_{in} < 5V$. Is diode D1 ON or OFF? Is NMOS MOSFET M1 in its Saturation, Triode, or Off region?

3. Assume the input voltage $0 < V_{in} < 5V$. Label the actual directions of all the branch currents ($I_{R1}$, $I_{R2}$, $I_{R3}$, $I_{R4}$, $I_{D1}$, and $I_{M1}$).

4. Assume the input voltage $0 < V_{in} < 5V$. Solve all the node voltages ($V_1$, $V_2$, $V_3$, $V_4$ and $V_{out}$) and branch currents ($I_{R1}$, $I_{R2}$, $I_{R3}$, $I_{R4}$, $I_{D1}$, and $I_{M1}$) as functions of $V_{in}$ and the given device parameters.

5. Assume the input voltage $-5V < V_{in} < 0$. Is diode D1 ON or OFF? Is NMOS MOSFET M1 in its Saturation, Triode, or Off region?

6. Assume the input voltage $-5V < V_{in} < 0$. Label the actual directions of all the branch currents ($I_{R1}$, $I_{R2}$, $I_{R3}$, $I_{R4}$, $I_{D1}$, and $I_{M1}$).

7. Assume the input voltage $-5V < V_{in} < 0$. Solve all the node voltages ($V_1$, $V_2$, $V_3$, $V_4$ and $V_{out}$) and branch currents ($I_{R1}$, $I_{R2}$, $I_{R3}$, $I_{R4}$, $I_{D1}$, and $I_{M1}$) as functions of $V_{in}$ and the given device parameters.
Suppose you have a big ugly unknown electromechanical system, Σ, in front of you, that is full of nonlinear elements inside, but is otherwise such that its overall behavior from input to output is linear and time invariant.

You have a (perfect) sinusoidal signal generator in the lab, that produces signals \( A \cos \omega t \), with programmable amplitude \( A \), and frequency \( \omega \) ranging from zero to the “very large”.

You also have an (ideal) spectral analyzer that has two input lines and two outputs, and is such that if \( u_1(t) = \cos \omega t \) and \( u_2(t) = B \cos \omega (t + \theta) \) (same frequency!) it produces the outputs \( y_1 = A \) and \( y_2 = \theta \).

In addition you have an actuator mapping a voltage input to whatever form the input of Σ may take, with (for simplicity) transfer function \( G_a(s) = 1 \), and a sensor that takes the output of Σ and maps it to a voltage, also with transfer function \( G_s(s) = 1 \).

i) As you have no idea what the system Σ is doing, you start to experiment and apply some pure sinusoids of various frequencies at the input \( \omega_1, \ldots, \omega_N \). In each case the output grows unboundedly and you have to shut the system off for safety. Could you actually have concluded that if the system goes unstable at one frequency, it must do so at all frequencies?

ii) Now you remember you learned something about feedback. Indeed, when you feed the output of Σ back to the input in the usual feedback scheme, you nd that unity feedback makes the output go to zero asymptotically when arbitrary initial conditions are set up in Σ, but otherwise no external input is applied. Would this imply that for any sinusoidal input, the output of the feedback system is bounded?

iii) You also remember that the Nyquist criterion may help in deciding for which feedback gains, \( k \) around Σ, a closed loop system would be stable. Would it be possible to determine using experimental and analytic methods, all values of the proportional feedback gain, \( k \) for which the unknown system would remain asymptotically stable in closed loop. If so, describe how? If not, explain why not.
Problem 17 (Breadth: TELECOM - ECE 3600) Code Number: __________

PROBLEM

Given that the end-end delay between Host A and Host B is 10 milliseconds, and a bottleneck link has bandwidth 120 Mbps. Assume that the bottleneck link dominates the end-end delay which is half of the round trip delay (RTT). Assume maximum segment size (MSS) is 1500 bytes, and all segments are MSS.

(a) (3pts) Assume TCP now uses a window size $n$ to sent segments. What should $n$ be to fill the “bit pipe” at the bottleneck link in one RTT? (In other words, what is the bandwidth-delay product when the delay is considered as RTT?)

(b) (3ts) Consider that TCP starts from slow-start. Assume that there is no loss. How many RTTs are needed for the TCP congestion window size to grow to be at least $n$ as in (a)? (Provide your solutions in terms of $n$ first, then plug in numbers.)

(c) (3pts) Now consider that TCP starts from window size of one MSS, and increases the window size through additive increase. Assume that there is no loss. How many RTTs are needed for the TCP congestion window size to grow to be at least $n$ as in (a)? (Provide your solutions in terms of $n$ first, then plug in numbers.)

(d) (1pt) Using the results you have obtained from (b) and (c), provide an explanation why the practical TCP (i.e., the one we use now) adopts slow-start and additive-increase at different (i.e., the beginning and later) stages of a TCP session.
Consider the symmetric 2-port network made from three resistors as shown, for use in a 50 Ω system:

The incident and reflected voltage waves defined at the indicated ports are related by

\[
\begin{bmatrix}
V_1^- \\
V_2^-
\end{bmatrix} =
\begin{bmatrix}
S_{11} & S_{12} \\
S_{21} & S_{22}
\end{bmatrix}
\begin{bmatrix}
V_1^+ \\
V_2^+
\end{bmatrix}
\]

where the 2 by 2 matrix is known as the scattering matrix or \(S\)-matrix.

(a) Find the \(S\)-matrix for the above system.

(b) If port 2 is (improperly) terminated in a load resistor with \(R = 25 \ \Omega\), what is the reflection coefficient looking into port #1?
The figure below shows five situations in which light of free-space wavelength $\lambda_0 = 600$ nm is incident normally on a very thin film (the middle layer in each case). The indicated refractive indices are $n_1 = 1.5$ and $n_2 = 2.2$.

a) In each case, consider what happens to the reflected light in the limit where the thickness of the thin layer approaches zero. Please circle “enhanced” or “suppressed”. No need to explain your answers.

Case A:  Enhanced  Suppressed
Case B:  Enhanced  Suppressed
Case C:  Enhanced  Suppressed
Case D:  Enhanced  Suppressed
Case E:  Enhanced  Suppressed

b) What fraction of the light power is reflected in case A and case C, respectively, when the thickness of the thin layer goes to zero?

c) Between case C and case E, which case may lead to a better elimination of the reflection? What is the optimal thickness of the thin film in that case?

d) For the best anti-reflective case you considered in part (c), where the reflection of light at $\lambda_0 = 600$ nm is efficiently suppressed under normal incidence, what wavelength (within the visible spectrum) is minimally reflected when the light is incident at $30^\circ$?
A step-index optical fiber consists of a cylindrical core surrounded by a cladding as shown in the figure below. The refractive index of the core $n_{\text{core}}$ is greater than the index of the cladding $n_{\text{clad}}$.

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<tr>
<td>Core</td>
<td>$n_{\text{core}}$</td>
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<tr>
<td>Cladding</td>
<td>$n_{\text{clad}}$</td>
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For this optical fiber, draw the dispersion curve ($\omega$ vs. $\beta$) for the fundamental mode of this fiber on the axes provided below. For purposes of simplification assume that the core and cladding materials are dispersionless (their refractive indices do not vary with frequency). On your dispersion diagram include the “light lines” for the core and the cladding. Also, on your diagram, label the “zero dispersion frequency.”
A. Draw a standard electrocardiogram for a healthy human being. Label the intervals and describe the relevant heart function for each interval.

B. The resting (or filling) phase of the heart cycle is called the ________________.

C. The contractile (or pumping) phase of the heart cycle is called the ________________.
(10 pts) Body Posture / Position Sensing. In assessing a person’s overall health / wellness, it is important to determine the person’s body posture or position in real-time. Such information can facilitate the classification of daily living activities that the person is involved in, and also provide a context for other sensed parameters (such as heart rate). In two sentences or less, describe qualitatively what sensor(s) you can use to determine a person’s body position as unobtrusively as possible, without getting in the way of the person’s activities.

Draw three positions for the person (standing upright, seated, and supine), and the resultant signals measured using your sensing hardware to the right of each position. Be clear with your labeling.
In three sentences or less, describe the steps you would use for an automated algorithm to determine the person’s position from the sensed data shown in the figures you have drawn. Be specific – statements such as, “I will input the sensor data into a machine learning algorithm” will not be accepted.

What are two confounding factors that can potentially cause errors in your detection of body position from your sensed signals? Your answer should only provide the two factors, and one sentence about each describing why it can reduce your accuracy.