INSTRUCTIONS

1. Please check to ensure that you have a complete exam booklet. There are 25 numbered problems. Note that Problem 2 occupies 3 pages, Problem 4 occupies 2 pages, Problem 14 occupies 2 pages, Problem 17 occupies 2 pages, and Problem 20 occupies 2 pages. Including the cover sheet, you should have 32 pages. There should be no blank pages in the booklet.

2. The examination is closed book and closed notes. No reference material is allowed at your desk. A calculator is permitted.

3. All wireless devices must be turned off for the entire duration of the exam.

4. You may work a problem directly on the problem statement (if there is room) or on blank sheets of paper available from the exam proctor. Do not write on the back side of any sheet.

5. Your examination code number MUST APPEAR ON EVERY SHEET. This includes this cover sheet, the problem statement sheets, and any additional work sheets you turn in. DO NOT write your name on any of these sheets. Use the preprinted numbers whenever possible, or WRITE LEGIBLY!!

6. Under the rules of the examination, you must choose 8 problems to be handed in for grading. Each problem to be graded should be separated from the rest of the materials, stapled to the associated worksheets, and placed on the top of the appropriate envelope in the front of the exam room. DO NOT TURN IN ANY SHEETS FOR THE OTHER 17 PROBLEMS!!

7. The examination lasts 4 hours, from 9:30 AM to 1:30 PM EST.

8. When you hand in the exam:
   (a) Separate the 8 problems to be graded as explained above.
   (b) Check to see that your Code Number is in EVERY sheet you are turning in.
   (c) On the section at the bottom of this page, CIRCLE the problem numbers that you are turning in for grading.
   (d) Turn in this cover sheet (containing your code number) and the 8 problems to be graded.
   (e) All other material is to be placed in the discard box at the front of the room. You are not allowed to take any of the exam booklet pages from the room!
A function $F(A,B,C,D)$ is defined according to the truth table below. Here ‘x’ means ‘don’t care’.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>1</td>
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<td>1</td>
<td>x</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>x</td>
</tr>
</tbody>
</table>

(a) Express the function in a sum-of-minterms and ‘don’t cares’ form.

$$F(A,B,C,D) = \text{_______________________________}$$

(b) Show the function in a Karnaugh map, and identify (circle) all Prime Implicants.

![Karnaugh Map]

(c) Express the function as a minimized sum-of-products form.

$$F(A,B,C,D) = \text{_______________________________}$$

(d) List the Essential Prime Implicants.
The state transition table of a 4-state FSM (2 flip flops) is given below.

<table>
<thead>
<tr>
<th>Present State = A(t), B(t)</th>
<th>Input = I</th>
<th>Next State = A(t+1), B(t+1)</th>
<th>Output = Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>0</td>
</tr>
</tbody>
</table>

You are to design a finite state machine that realizes the above state transition diagram/state transition with one toggle flip flop (realizing the state A) and one D flip flop (realizing the state B) instead of two D flip flops. A toggle flip flop works as follows. When the input T(A) of the toggle flip flop is 1, the output A(t+1) of the flip flop becomes the complement of A(t). When the input T(A) of the flip flop is 0, the output A(t+1) of the flip flop is the same as its previous value A(t). This is shown in the state transition table for the T flip flop below. Both flip flops are positive edge triggered.

<table>
<thead>
<tr>
<th>T(A)</th>
<th>A(t)</th>
<th>A(t+1)</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>hold</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>hold</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>toggle</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>toggle</td>
</tr>
</tbody>
</table>

In contrast, the state transition table of a D flip flop is as follows:

<table>
<thead>
<tr>
<th>D(B)</th>
<th>B(t)</th>
<th>B(t+1)</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>B(t+1) = D(B)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>B(t+1) = D(B)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>B(t+1) = D(B)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>B(t+1) = D(B)</td>
</tr>
</tbody>
</table>
Problem 2 (Core: VSDD-ECE2030)  

(a) Below, fill in the K-maps for $T(A)$, $D(B)$ and $Z$ and write the minimal Boolean expressions for the same.

$T(A) = \begin{array}{cccc}
00 & 01 & 11 & 10 \\
0 & & & \\
1 & & & 
\end{array}$

$D(B) = \begin{array}{cccc}
00 & 01 & 11 & 10 \\
0 & & & \\
1 & & & 
\end{array}$

$Z = \begin{array}{cccc}
00 & 01 & 11 & 10 \\
0 & & & \\
1 & & & 
\end{array}$
(b) Draw a circuit diagram for the finite state machine showing all logic, FSM input and output and the two flip flops corresponding to A and B.
The following RISC assembly language program is executed on a 32-bit MIPS processor. Fill in the register values that will be present, after execution of this program. A summary of MIPS instructions is included at the bottom of the page – for anyone unfamiliar with the MIPS instruction set. Prior to execution of the program, memory location 0x04000 contains 0x20313055. Note: 0x indicates hexadecimal and all answers must be in hexadecimal, default is decimal in the MIPS assembly language source file. A MIPS memory word or register contains 32-bits. Use XXXXXXXX for an undefined value.

```
lw $3, 0x04000
sll $4, $3, 7
sub $2, $4, $3
xor $3, $4, $2
lui $5, 10
ori $5, $5, 12561
add $6, $4, $3
bne $5, $6, LABEL1
addi $6, $0, -2035
LABEL1:
sw $6, 0x04000
```

After execution of the MIPS code sequence above,

R2 = 0x_____________________ (in hexadecimal)

R3 = 0x_____________________ (in hexadecimal)

R4 = 0x_____________________ (in hexadecimal)

R5 = 0x_____________________ (in hexadecimal)

Memory Location 0x04000 contains: 0x_____________________ (in hexadecimal)

The MIPS processor contains thirty-two 32-bit registers, $0 through $31. $0 always contains a zero. By default, all arithmetic operations use two’s complement arithmetic. Assume no branch delay slot is present.

### MIPS Instruction

<table>
<thead>
<tr>
<th>MIPS Instruction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDI</td>
<td>Rd, Rs, Immed - Rd = Rs + Immediate value</td>
</tr>
<tr>
<td>ADD</td>
<td>Rd, Rs, Rt - Rd = Rs + Rt (R – register ($) )</td>
</tr>
<tr>
<td>ORI</td>
<td>Rd, Rs, Immed - Rd = Rs low 16-bits bitwise logical OR Immediate value</td>
</tr>
<tr>
<td>LUI</td>
<td>Rd, Immed - Rd = 16-bit Immediate value high 16-bits, 0's low 16-bits</td>
</tr>
<tr>
<td>BNE</td>
<td>Rs, Rt, address - Branch to address, only if Rs not equal to Rt</td>
</tr>
<tr>
<td>LW</td>
<td>Rd, address - LOAD - Rd gets contents of memory at address</td>
</tr>
<tr>
<td>SLL</td>
<td>Rd, Rs, count - Shift left logical (use 0 fill) by count bits</td>
</tr>
<tr>
<td>SUB</td>
<td>Rd, Rs, Rt - Rd = Rs - Rt</td>
</tr>
<tr>
<td>SW</td>
<td>Rd, address - STORE - memory at address gets contents of Rd</td>
</tr>
<tr>
<td>XOR</td>
<td>Rd, Rs, Rt - Rd = Rs bitwise logical XOR Rt</td>
</tr>
</tbody>
</table>
Consider the following logic gate:

\[ V_{DD} \]

\( A \) \( \rightarrow \)

\( B \) \( \rightarrow \)

\( D \) \( \rightarrow \)

\( C \) \( \rightarrow \)

\( C_{ext} = 4C \)

\( A \) \( \rightarrow \)

\( B \) \( \rightarrow \)

(a) Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS of \( W/L = 1 \) and PMOS of \( W/L = 2 \). (You can put the sizing numbers on the transistor diagram). (5 point)
Problem 4 (Core: VSDD-ECE3060)  

(b) For the previous circuit and your sizing solution, compute the RC delay for the following transitions. Clearly show the values of all junction capacitances and the resistances of each device in the circuit schematic of part-a. Show your RC delay computation to receive full credits. (5 points)

<table>
<thead>
<tr>
<th>Transition</th>
<th>RC Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>(i) ABCD: (0111) → (0110)</td>
<td></td>
</tr>
<tr>
<td>(ii) ABCD: (1011) → (1010)</td>
<td></td>
</tr>
</tbody>
</table>

Make the following assumptions:

- The junction capacitance of NMOS and PMOS with width W is C.
- The resistance of NMOS of size W is R.
- The electron mobility is 2X higher than the hole mobility ($\mu_n/\mu_p = 2$).
- Threshold voltage, channel length, and oxide thickness of PMOS and NMOS are same.
- The total load capacitance at output need to consider this external load cap and the junction capacitances of the NMOS/PMOS connected to the output.
A square loop of current with side lengths $L$ lies on the $xy$-plane, centered on the origin. Given a line current $I$ within the loop, what is the magnetic field $H$ at points along the $z$-axis, i.e., what is $H(0,0,z)$?

*Hint:* The following integral might be useful:

$$\int \frac{du}{(a^2 + u^2)^{3/2}} = \frac{u}{a^2 \sqrt{a^2 + u^2}} + C$$
Albert lives in a quiet valley in North Georgia where he operates a winery and vineyard. Set apart from civilization, he has no access to cable, DSL, phone lines, or any other wired conduit of internet access. But Albert is a crafty graduate of the Georgia Institute of Technology and devises a clever way to steal wireless internet service from the nearby town of Unprotectedlinksville, population 53. This town is 10 kilometers away from Albert, on the other side of a large mountain, and has several unprotected home WiFi servers broadcasting local internet service. Albert’s plan is to purchase 3 identical dish antennas that operate at 2.45 GHz and arrange them in the following configuration:

With this set-up, a signal will propagate from the town to the first dish in the link, which is pointed toward the town. The received power of this dish is piped directly to another dish which is pointed towards Albert’s vineyard. Thus, this pair of dish antennas acts like a passive repeater that does not require any power or maintenance. A third dish is mounted on top of Albert’s home, where a minimum value of -95 dBm must be received in order to maintain a wireless internet link on his home computer. Answer the following questions assuming matched and lossless cables. Assume that the antenna gain of the WiFi access point in town is 5 dBi, that the transmit power of this link is 30 dBm, and that both links are essentially free space (no excess loss).

(a) What is the minimum gain in dBi of these antennas to make this system work? (Ignore the effects of small-scale fading.) (7 points)

(b) If these are ideal circular dishes with 100% efficiency, what is the minimum radius based on your answer in part (a)? (3 points)

Useful Formulas:

\[ P_R = P_T + G_T + G_R - 20 \log_{10}(4\pi/\lambda) - 20 \log_{10}(r) - \text{Extra Loss} \]

\[ f\lambda = c, \quad G_{peak} = \frac{4\pi A_{em}}{\lambda^2} \]
Problem 3 (EDA-ECE2040) Code Number: 

Find $R$ and $C$ in the circuit below, so that $R$ consumes maximum power.

$V_s(t) = \cos t \ [V]$
The figure below is a BJT differential amplifier. It is given that $V_{CC} = 12$ V, $V_{EE} = 12$ V, $I_{EE} = 400$ µA, $R_{EE} = 200$ kΩ, $V_T = 0.025$ V, $R_L = 2$ kΩ. For all transistors, $\beta = 100$, $r_o = 300$ kΩ, and $|V_{BE}| = 0.7$ V.

1. Draw the small-signal circuit.
2. Assume the current mirror and the current source $I_{EE}$ are ideal. If $R_L$ is not connected, derive and calculate the transconductance gain of the differential amplifier for differential-mode input signals.
3. With $R_L$ connected as in the circuit, calculate the differential-mode voltage gain.
A 100 hp (74,570 W) three-phase, wye-connected, 60 Hz, 4-pole, cylindrical rotor synchronous motor is operating at rated conditions and 80 percent power factor (leading). The efficiency, excluding field and stator losses, is 96 percent, and the synchronous reactance is 2.72 Ohms/phase.

Determine:

(a) developed torque;
(b) armature current;
(c) excitation voltage;
(d) power angle;
(e) maximum torque (also called pull-out torque).
Transformer Problem

A 15 kVA, 2300/230 volt, 60 Hz, single phase transformer has the following equivalent circuit with the following parameters referred to the 2300 volt side:

\[ R_{eq} = 4.45 \, \text{ohm}; \quad X_{eq} = 6.45 \, \text{ohm}; \quad R_c = 105 \, \text{kilo ohm}; \quad X_m = 11 \, \text{kilo ohm}; \]

(a) Calculate the magnitude of the input voltage \( V_{in} \) to the transformer when it supplies rated kVA to a load at a power factor of 0.8 lagging, at rated voltage.

(b) Calculate the efficiency for the conditions in (a).
In the diagram below, sketch and label the energy vs. distance ($E$ vs. $x$) diagram for an $N^+P-N^+$ BJT in the **NORMAL ACTIVE REGION** of operation. Assume that the BASE terminal is grounded (i.e., the base terminal is the reference terminal) and show the arrows corresponding to the energies related to the BASE-EMITTER and BASE-COLLECTOR voltages, $V_{BE}$ and $V_{BC}$ and their polarities. Draw and label the “quasi-Fermi level energies”, $F_n$ or $F_p$, for MAJORITY carriers in each region outside the depletion regions (DRs). I have given you the energies $E_C$ and $E_V$ in the base.

![Diagram of energy vs. distance for an N^+P-N^+ BJT in the NORMAL ACTIVE REGION of operation.](image-url)
The doping concentration in an ideal Si MOS capacitor is \( N_D = 10^{15} \text{ cm}^{-3} \) and its SiO\(_2\) insulator is 1nm thick. The device is at room temperature. Ideal here means no charges in oxide or interface and flat-band condition.

1. What is the Fermi potential of the substrate in this MOS capacitor? (Reminder: Fermi potential is defined as \( (E_{i-Bulk} - E_F)/q \).)

2. What is the Si surface potential when the device is at the onset of inversion?

3. If the electric field at the surface of Si is −10KV/cm, what would be the electric field at the middle of the insulator?

4. Assume a second MOS capacitor that is identical with this MOS capacitor except for a charge that is trapped at the interface of the Si and SiO\(_2\) regions of the second device. If the charge density is \( 3.4 \times 10^{-6} \text{ C/cm}^2 \), what would be the difference between the threshold voltages of the two MOS capacitors?

\( kT = 26 \text{ meV at room temperature. } k_{Si} = 11.8, k_{SiO2} = 3.9, n_i = 10^{10} \text{ cm}^{-3} \)
Problem 13 (Core: DSP-ECE2026)  

**PROBLEM**

A *Linear and Time-Invariant* system is described by a difference equation

\[ y[n] = 0.7x[n - 1] - 0.4y[n - 1] \]

where \( y[n] \) is the output signal and \( x[n] \) is the input.

(a) This system is **FIR** **IIR** (circle one)

(b) Determine the system function, \( H(z) = \)

(c) Determine an equation for the impulse response, \( h[n] = \)

(d) Determine the output when the input \( x[n] = 10\cos(\pi n - 0.2\pi) \). \( y[n] = \)

(e) Determine the input signal so that the output is \( y[n] = \delta[n - 3] \). \( x[n] = \)
Two indistinguishable but biased coins lie on the table in front of you. When Coin A is flipped, it comes up heads \( (H) \) with probability \( \frac{3}{4} \). When Coin B is flipped, it comes up \( H \) with probability \( \frac{2}{5} \). You choose one of them at random and start flipping it.

1. What is the probability that you see the first \( H \) on the fourth flip?

2. Suppose you do see the first \( H \) on the fourth flip. What is the probability you are holding Coin A?
3. Given the observation of the first $H$ coming on the fourth flip, what is the probability that the fifth flip will also be $H$?
Problem 15 (Core: S&C-ECE3550)  

Consider the feedback configuration below. Assume that $C(s)$ is chosen cleverly enough such that the output $y$ of the closed-loop system is bounded for all bounded reference signals $r$, no matter what $k$ is. The plant and controller are of the form

$$G(s) = \frac{P(s)}{Q(s)}, \quad C(s) = \frac{P_C(s)}{Q_C(s)},$$

where $P, Q, P_C, Q_C$ are polynomials in $s$, and where $P(0) \neq 0, Q_C(0) \neq 0$.

**Problem**

For what values of $k$ can perfect tracking be guaranteed, in the sense that the steady-state tracking error of a constant reference signal is zero?

b

Same question as in a but now the reference signal $r(t)$ is a *decaying exponential*,

$$r(t) = 1 - e^{-t}.$$

c

Same question as in a but now the reference signal $r(t)$ is a *sinusoid*,

$$r(t) = \sin(t).$$
The feedback gains of the control system shown below have been chosen to place both eigenvalues of the overall system at $s = -1$ under the false assumption that the actuator transfer function is equal to unity. Determine the full range of actuator eigenvalue $\lambda$ for which the actual third-order overall system is internally stable.

\[ r + \int + 1 + \frac{\lambda}{s + \lambda} + \frac{1}{s - 1} \rightarrow y \]
Question 1:

This question involves stack frame and function calls. The following convention is used:

1. The system is a 32-bit MIPS computer. Function calls are implemented via ‘jal’ and function call returns are implemented via ‘jr $31’.
2. The stack grows downwards (towards the lower end of the address space).
3. Frame pointer is not used, so it doesn't need to be preserved and restored.
4. All parameters are passed via the stack (none are passed via registers).
5. Caller only allocates part of the activation frame for the callee before calling 'jal' - it only allocates the input parameters on the stack, and updates the stack pointer accordingly (right on top of the input parameters).
6. Caller pushes input parameters onto the stack in the reverse order as the parameters are declared.
7. Callee is responsible of populating the rest of the activation frame, which includes the return address, return value, and local variables.
8. Caller is responsible of deallocating the entire activation frame (of the callee) when the callee returns.
9. The activation frame of a function is populated in the following order:
   1) Input parameters (allocates only if there are any input parameters)
   2) Return address
   3) Return value (allocates only if the function does return a value)
   4) Local variables (if any)
10. The local variables are allocated in the same order as they were defined.
11. Stack pointer points to the next available slot on the stack.

The question is on the next page:
We have the following program:

```c
#define N 10

int foo (int A) {
    int w[10];
    int i;
    for(i=0;i<10;i++) w[i] = i;
    for(i=0;i<N; i++) w[i] = w[i] - 4;
    return w[0];
}

int main () {
    return foo(3);
}
```

What may happen to the code if we change the definition of \(N\) to the following values?

1. \#define N 11

2. \#define N 12
A priority queue is an abstract data structure that stores numeric values as they arrive to the queue and, when a value is requested from the queue, it dequeues (removes) the largest value currently in the queue.

a) Describe a (real) data structure that can be used to implement a priority queue and which requires $O(\log n)$ time for each operation in an arbitrary sequence of enqueue and dequeue operations, where $n$ is the length of the queue. The enqueue operation adds an arbitrary item to the queue and the dequeue operation removes the largest item. Be sure to justify why the enqueue and dequeue operations require $O(\log n)$ time for your data structure.

b) Write pseudo-code for the enqueue and dequeue operations for your data structure.
Problem 19 (Specialized: Telecom-ECE3076)   Code Number: _________

PROBLEM

What four items of information are needed before a Internet host can operate normally on the network:

1. ________________________________
2. ________________________________
3. ________________________________
4. ________________________________

If these are not configured manually, what protocol can be used to get them over the network?

5. ________________________________

6. Every Internet Autonomous System must have an Authoritative DNS. What does it do?

7. ____________________________________________________________

Why has Georgia Tech migrated its campus WiFi wireless network from WEP to WPA-Enterprise?

8. ____________________________________________________________

What circumstance has made the immediate transition from IP version 4 to IP version 6 necessary?

9. ____________________________________________________________

If Georgia Tech OIT assigns you the 130.209.123.0/24 block of IP addresses for the subnet in your lab:

9. What is the lowest address that you can assign to a host? ____________________________

10. What is the IP subnet broadcast address? ________________________________________
Problem 20 (Specialized: Optics-ECE4500)  

**Problem**

Grating Spectrometer - Wavelength Demultiplexing

A waveguide reflection grating spectrometer is used for wavelength division demultiplexing. Three telecommunication signal waves from the waveguide are incident in air upon the metallic grating at an angle of 15° counter-clockwise from the normal as shown in figure. The three waves have frequencies of 195.5 Terahertz, 196.0 Terahertz, and 196.5 Terahertz which are frequencies on the ITU standard grid. The three wavelengths are dispersed by the grating into $i = +1$-order backward-diffracted waves as shown in the figure. The grating is designated as having “800 lines per mm.” An array of photodetectors is oriented normal to the 196.0 Terahertz (no. 2) beam as shown.

![Diagram of grating spectrometer](image)

1) Calculate, showing all work, the wavelengths in nanometers of the waves numbered 1, 2, and 3 in the figure.

2) Calculate, showing all work, the backward-diffracted wave angles (measured counter-clockwise from the normal) in degrees for these waves.
Express wavelengths accurately to five significant figures. Express the angles in degrees accurately to within ±0.01°. Put your answers in the spaces provided.

<table>
<thead>
<tr>
<th>Wave No.</th>
<th>Wavelength (nm)</th>
<th>Angle of Diffraction (°)</th>
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An optical fiber communication link is assembled using binary on-off keying with direct detection. The optical transmitter consists of a cw (continuous wave) laser whose output is externally modulated to produce the binary NRZ signal. At the other end, an optical receiver is used in which thermal noise is the dominant noise contributor (all other noise mechanisms are negligible). At room temperature (300° K), the noise current is found to be $\sigma_T = 60.0$ nA. The average optical power at the receiver is $P_{\text{rec}} = 1.5 \mu$W, with incomplete extinction — that is, the modulator does not completely block the laser power. As a result, 20% of the optical power resides in the “zero” bit slots, with the rest in the “one” bits. Upon detection, the resulting current levels in the “one” and “zero” bits are $I_1 = 0.4 \mu$A and $I_0 = 0.1 \mu$A respectively.

a. Evaluate $Q = (I_1 - I_0)/(\sigma_1 + \sigma_0)$.

It is desired to operate the link at a BER of $10^{-9}$, which means that $Q$ must attain a value of 6. This is to be accomplished by doing two things simultaneously: 1) cool the receiver with liquid nitrogen ($T = 77^\circ$ K), and 2) increase the average optical power.

b. What is the new required average optical power, and what is the equivalent decibel reduction in link loss needed to accomplish this?

c. Suppose an ideal modulator is used, such that complete extinction is achieved (zero power in the “zero” bit slots), but with the laser output power unchanged. With this accomplished, in addition to the aforementioned temperature reduction, re-answer part b.
Design a process flow using to pattern a thin film deposited layer of copper on a silicon substrate using negative photoresist. The process flow should consist of a step-by-step cross sectional flow diagram of the process with a short description of each step next to the cross section. The process flow should include a cross section of the mask design at the appropriate point in the flow diagram.
Problem 23 (Specialized: BioEng-ECE4781)  

**PROBLEM**

Draw a sketch of a typical motor neuron in humans, labeling five different anatomical parts. (2 points)

Why do motor neurons have more than one leg? (2 points)

What happens inside a motor neuron that makes naturally occurring Action Potentials travel in one direction down the motor neuron? (2 points)

Design a data acquisition system for measuring the human EMG using skin electrodes. You can represent each stage of your data acquisition system using a block diagram, but specify details like the gain and other features of each amplifier stage, filters with corners specified, and exactly how you will isolate the patient from line voltage and line ground. (4 points)
Problem 24 (Specialized: BioEng-ECE4782)  Code Number: __________

PROBLEM

Why do hospital diagnostic labs use pulse stimuli when they know that all biological systems are nonlinear, and what can they do to make the system appear to be more linear? (2 points)

How does adaptation affect the convolution integral representation of the system? (2 points)

What changes in the convolution integral if the system is noncausal? (2 points)

What is the best way to deal with periodic noise when using pulse stimuli? (2 points)

Why is it difficult to measure a Visual Evoked Response using pulse stimuli of light and surface electrodes on the scalp? (2 points)
For a voltage clamped membrane, find the minimum seal resistance to achieve a signal to noise ratio of 75 for a potassium channel with the following characteristics. 
\[ g_k = 20 \text{ pS}, \quad V_m = -40 \text{ mV}, \quad E_k = -90 \text{ mV}, \quad T = 25 \text{ C}, \quad \text{frequency range} = 100 \text{ Hz} \]