JAE YOUNG CHOI

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OBJECTIVE

Full-time engineering position in power/signal integrity analysis, electronic packaging design, or related area

EDUCATION

Georgia Institute of Technology – Atlanta, Georgia

Ph.D. in Electrical & Computer Engineering **Expected Graduation Date: Oct. 2012**

- Overall graduate GPA: 3.7/4.0

M.S. in Electrical & Computer Engineering/ Minor in Mathematics **Aug. 07 – Dec. 09**

- Related courses: Power integrity modeling and design, Applied electromagnetics, Microwave design, Electromagnetic compatibility, Electromagnetic radiation & antennas, Computational electromagnetics, Microelectronic system packaging

Yonsei University – Seoul, South Korea

B.S. in Electrical & Electronic Engineering **Mar. 99 – Feb. 07**

- Dean's list: Fall 2000 and Fall 2003 through Spring 2005, GPA: 3.5/4.3
- Off campus for military service (2001 – 2003)

ACADEMIC EXPERIENCE

Mixed Signal Design Group – Georgia Institute of Technology, Atlanta **Jan. 08 – Present**

- *Graduate research assistant (Advisor: Dr. Madhavan Swaminathan)*
- Modeling, simulation, and measurement of high-speed signal interconnects in combination with power distribution network
- Development of a modeling method for multi-layer power/ground planes - (Multi-layer triangular element method; MTEM)
- Design, simulation, and analysis of power distribution network of electronic packages and boards
- Development of an optimization tool for selection and placement of decoupling capacitors using finite element method and genetic algorithm

Microwave & Antenna Laboratory – Yonsei University, Seoul, South Korea **Mar. 07 – Jul. 07**

- *Post-undergraduate research internship (Advisor: Dr. Young-Joong Yoon)*
- Design and analysis of a high-impedance surface (Phase-shift artificial magnetic conductor)
- Design and characterization of a circular polarized dipole antenna using an artificial magnetic conductor as a ground plane
- Design and fabrication of an artificial magnetic conductor and antennas, and measurement using an NSI near-field scanner and an anechoic chamber

Advanced Computational EM Laboratory – Yonsei University, Seoul, South Korea **Jul. 06 – Dec. 06**

- *Undergraduate independent research program (Advisor: Dr. Jong-Gwan Yook)*
- Design and characterization of a dual-band non-uniform helical antenna for mobile communications

INDUSTRY EXPERIENCE

INTEL CORP. – Chandler, Arizona **May 11 – Aug. 11**

- *Internship – Sort Test Technology Development*
- Implementation of a script for statistical modeling of a chipset test-contactor and a test-interface-unit for signal integrity analysis

- Completion of basic training in chipset test flow and test methodologies

APPLE INC. – Cupertino, California **May 10 – Aug. 10**

- *Internship – Signal Integrity team*
- Testing and characterization of a clock-recovery-unit used for a high-speed channel interface
- Measurement and evaluation of the high-speed interface installed in system prototypes

APPLE INC. – Cupertino, California **May 09 – Aug. 09**

- *Internship - Signal Integrity team*
- Modeling, simulation, and measurement of high-speed transmission lines to characterize loss and crosstalk for next-generation applications
- Correlation of measured data to theoretical results to characterize channel performance

PARSONS BRINCKERHOFF – Boston, Massachusetts **Mar. 06 – May 06**

- *Internship - Mechanical & Electrical department*
- Research on roadway lighting and safety and publication to the North America Illuminating Engineering Society

SAMSUNG ELECTRONICS – Suwon, South Korea **Jan. 05 – Feb. 05**

- *Industrial and educational training - Advanced Technology Training Institute*
- Mobile communication training on UMTS, CDMA2000, and digital MODEM
- Team research project on W-CDMA communication receiver systems

SKILLS

Software	PCB Design (Allegro), HFSS (Ansys), CST, PowerSI (Sigrity), ADS (Agilent), Sonnet (Sonnet software), Agilent PLTS, Zealand IE3D, Microwave Office (AWR), Designer (Ansys), PSPICE, HSPICE, MATLAB, Visual Basic, C/C++, AutoCAD
Hardware	NSI near-field scanner, Anechoic chamber [10x10x5m, ~50GHz], Tektronix BERT Scope, VNA [4-port, ~50GHz], TDR/TDT [~20GHz], Spectrum Analyzer, Probe station

PUBLICATIONS

- J. Y. Choi and M. Swaminathan, “Decoupling Capacitor Placement in Power Delivery Networks Using MFEM,” *IEEE Trans. on CPMT*, Vol. 1, No. 10, pp. 1651–1661, 2011.
- J. Y. Choi and M. Swaminathan, “Practical Aspects of Modeling Apertures for Signal and Power Integrity Co-simulation,” *IEEE Proc. on EPEPS*, Oct. 2011.
- J. Y. Choi and M. Swaminathan, “Modeling Methods for Power/Ground Plane Structures in Electronic Packages,” *IEEE Proc. on ICEAA*, pp. 1380–1383, Sep. 2011.
- J. Y. Choi and M. Swaminathan, “An Effective Modeling Method for Multi-scale and Multilayered Power/Ground Plane Structures,” *IEEE Proc. on ECTC*, pp. 477–483, May 2011.
- K. Bharath, J. Y. Choi, and M. Swaminathan, “Use of the finite element method for the modeling of multi-layered power/ground planes with small features,” *IEEE Proc. on ECTC*, pp. 1630–1635, May 2009.

PATENT

- “Modeling of multi-layered power/ground planes using triangle elements,” US Patent Application: 12/710991, filed on 2/23/2012.

REFERENCES

- Available upon request.