

MIPS Instruction Set (core)

<i>instruction</i>	<i>example</i>	<i>meaning</i>
arithmetic		
add	add \$1,\$2,\$3	$S1 = S2 + S3$
subtract	sub \$1,\$2,\$3	$S1 = S2 - S3$
add immediate	addi \$1,\$2,100	$S1 = S2 + \text{sign_extend}(100)$
add unsigned	addu \$1,\$2,\$3	$S1 = S2 + S3$
subtract unsigned	subu \$1,\$2,\$3	$S1 = S2 - S3$
add immediate unsigned	addiu \$1,\$2,100	$S1 = S2 + \text{sign_extend}(100)$
set if less than	slt \$1, \$2, \$3	if ($S2 < S3$), $S1 = 1$ else $S1 = 0$
set if less than immediate	slti \$1, \$2, 100	if ($S2 < \text{sign_extend}(100)$), $S1 = 1$ else $S1 = 0$
set if less than unsigned	sltu \$1, \$2, \$3	if ($S2 < S3$), $S1 = 1$ else $S1 = 0$
set if < immediate unsigned	sltui \$1, \$2, 100	if ($S2 < 100$), $S1 = 1$ else $S1 = 0$
multiply	mult \$2,\$3	Hi, Lo = $S2 * S3$, 64-bit signed product
multiply unsigned	multu \$2,\$3	Hi, Lo = $S2 * S3$, 64-bit unsigned product
divide	div \$2,\$3	Lo = $S2 / S3$, Hi = $S2 \bmod S3$
divide unsigned	divu \$2,\$3	Lo = $S2 / S3$, Hi = $S2 \bmod S3$, unsigned
transfer		
move from Hi	mfhi \$1	$S1 = \text{Hi}$
move from Lo	mflo \$1	$S1 = \text{Lo}$
load upper immediate	lui \$1,100	$S1 = 100 \times 2^{16}$
logic		
and	and \$1,\$2,\$3	$S1 = S2 \& S3$
or	or \$1,\$2,\$3	$S1 = S2 S3$
and immediate	andi \$1,\$2,100	$S1 = S2 \& \text{zero_extend}(100)$
or immediate	ori \$1,\$2,100	$S1 = S2 \text{zero_extend}(100)$
nor	nor \$1,\$2,\$3	$S1 = \text{not}(S2 S3)$
xor	xor \$1, \$2, \$3	$S1 = S2 \oplus S3$
xor immediate	xori \$1, \$2, 255	$S1 = S2 \oplus \text{zero_extend}(255)$
shift		
shift left logical	sll \$1,\$2,5	$S1 = S2 \ll 5$ (logical)
shift left logical variable	sllv \$1,\$2,\$3	$S1 = S2 \ll S3$ (logical), variable shift amt
shift right logical	srl \$1,\$2,5	$S1 = S2 \gg 5$ (logical)
shift right logical variable	srlv \$1,\$2,\$3	$S1 = S2 \gg S3$ (logical), variable shift amt
shift right arithmetic	sra \$1,\$2,5	$S1 = S2 \gg 5$ (arithmetic)
shift right arithmetic variable	srav \$1,\$2,\$3	$S1 = S2 \gg S3$ (arithmetic), variable shift amt
memory		
load word	lw \$1, 1000(\$2)	$S1 = \text{memory}[S2+1000]$
store word	sw \$1, 1000(\$2)	$\text{memory}[S2+1000] = S1$
load byte	lb \$1, 1002(\$2)	$S1 = \text{memory}[S2+1002]$ in least sig. byte, sign extended (sign bit extends 24 bits to left)
load byte unsigned	lbu \$1, 1002(\$2)	$S1 = \text{memory}[S2+1002]$ in least sig. byte, zero extended (padded with 24 zeros to the left)
store byte	sb \$1, 1002(\$2)	$\text{memory}[S2+1002] = S1$ (byte modified only)
branch		
branch if equal	beq \$1,\$2,100	if ($S1 = S2$), $\text{PC} = \text{PC} + 4 + (100*4)$
branch if not equal	bne \$1,\$2,100	if ($S1 \neq S2$), $\text{PC} = \text{PC} + 4 + (100*4)$
jump		
jump	j 10000	$\text{PC} = 10000*4$
jump register	jr \$31	$\text{PC} = S31$
jump and link	jal 10000	$S31 = \text{PC} + 4$; $\text{PC} = 10000*4$