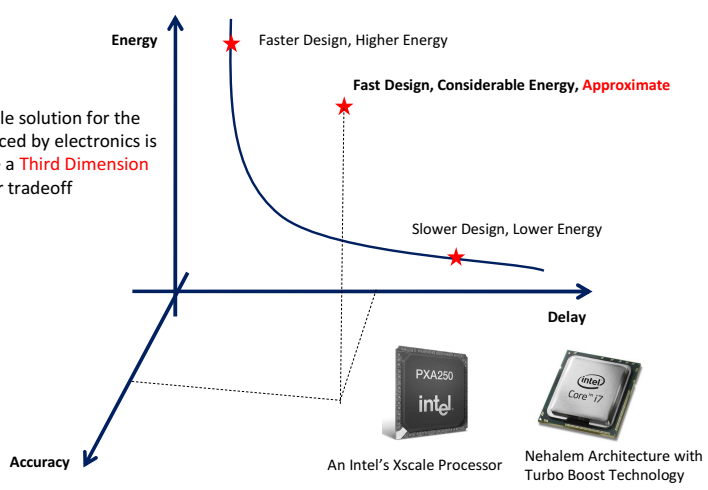
An Approach to Energy-Error Tradeoffs in Approximate Ripple Carry Adders

Zvi M. Kedem, Vincent J. Mooney, Kirthi Krishna Muntimadugu and Krishna V. Palem

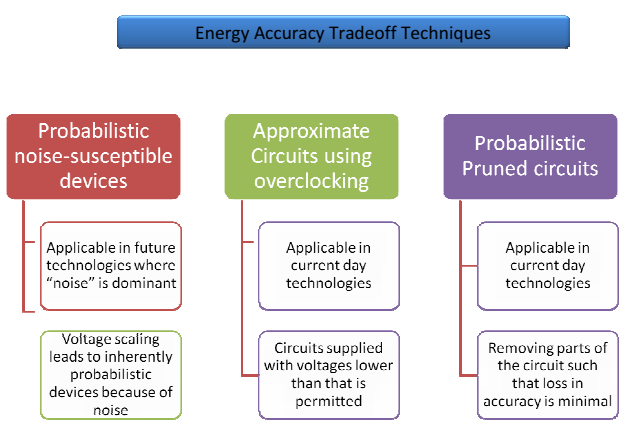
Courant Institute of Mathematical Sciences, New York University, New York, USA, Email: kedem@nyu.edu
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA, Email: mooney@gatech.edu
School of Electrical & Electronic Engineering and School of Computer Engineering, Nanyang Technological University, Singapore, Email: vjmooney@ntu.edu.sg
Department of Electrical and Computer Engineering, Rice University, Houston, Texas, USA, Email: (kirthi.krishna, palem)@rice.edu
'NTU-Rice Institute of Sustainable and Applied InfoDynamics (ISAID), Nanyang Technological University, Singapore

Three Dimensions of Trade-Off

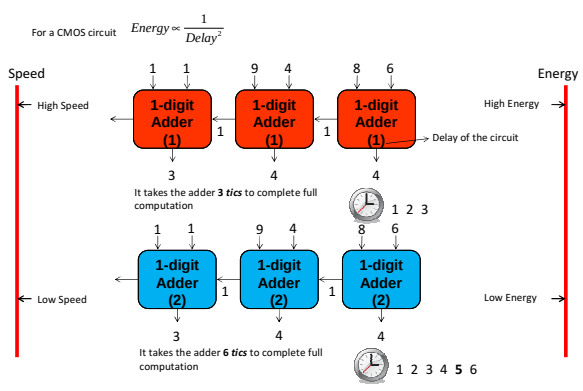
One possible solution for the challenges faced by electronics is to introduce a Third Dimension for tradeoff



Inexact Circuits

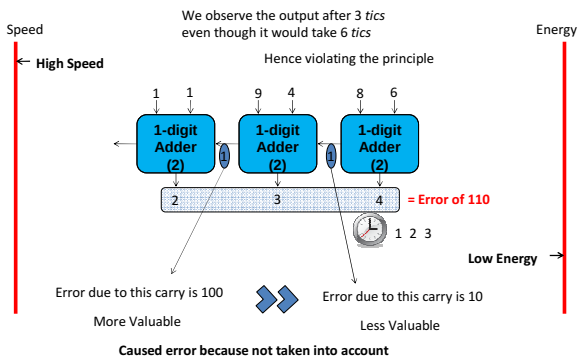


Conventional Circuit Design

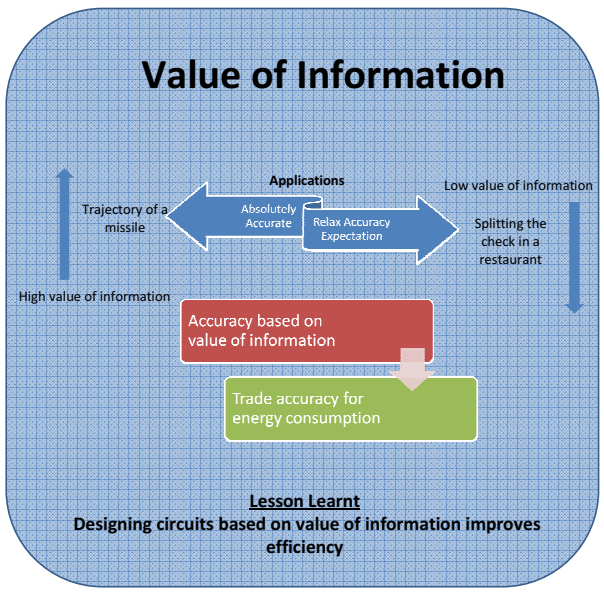


Approximate Arithmetic Circuits

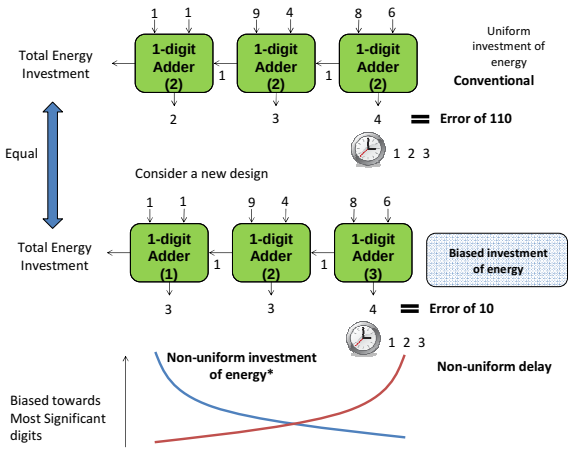
Breaking the conventional design principle



Value of Information



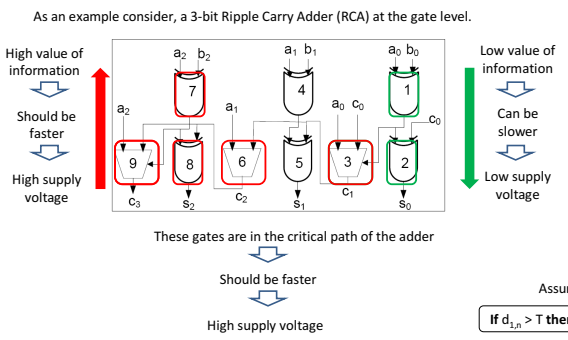
Biased Voltage Supply (BIVOS) Versus Uniform Voltage Supply (UVOS)



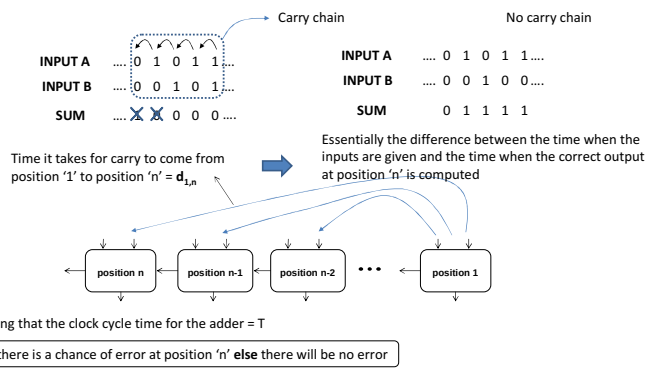
Problem Statement

- Given
  - A circuit of an *n*-bit adder at the gate level
  - Clock cycle time (T)
  - Energy Consumption Budget (**E**)
- Determine supply voltage for each gate in the adder
  - Based on value of information
- To minimize *the average error at the output of the adder* for given clock cycle time (T)
  - Such that the *total energy consumption* ≤ **E**

Optimization Challenge



Carry Chains and Approximate Adders



Error Model

- Consider specific n-bit inputs A and B
  - For these specific inputs define a Boolean variable

$$C_{ij}(A,B) = \begin{cases} 1 & \text{if there is a carry chain from i to j} \\ 0 & \text{otherwise} \end{cases}$$

  - Define an indicator function as follows

$$I(A,B,d,T,k) = \begin{cases} 1 & \text{if } d_{ik} > T, C_{ij}(A,B) = 1, i < k < j \\ -1 & \text{if } d_{ik} > T, C_{ij}(A,B) = 1, k = j \\ 0 & \text{otherwise} \end{cases}$$

    - Where *d* is the set of delays of all possible sum paths
  - The error at the output for two specific inputs A and B is

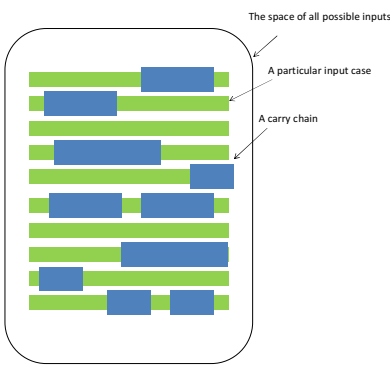
$$Er_1(A,B,d,T) = \sum_{k=0}^{n-1} I(A,B,d,T,k)2^k$$

  - The average error is the average over all possible input cases

$$Er(d,T) = \sum_{0 \le A,B < 2^n} p(A,B) Er_1(A,B,d,T)$$

p(A,B) is the probability of the input pair A and B given a benchmark

•There are 2^{2n} different input combinations.
• Becomes computationally very intensive for large *n*.



Computing the average error over all **possible inputs**

As only carry chains result in errors → Is equivalent to

Computing the average error over all **possible carry chains**

ADVANTAGE : The total number of possible carry chains is only $O(n^2)$ as opposed to $O(2^{2n})$

Solution using Geometric Programming & Supply Voltage Binning

$$\text{Minimize } Er_{avg}(d,T) = \sum_{0 \le i < j \le n-1} p_{ij} Er_2(i,j,d,T)$$

$$\text{Such that } E^A = \sum_{l=1}^{N} \left(E_l^D(v_l) W_l^A + P_l^S(v_l) T \right) \le \mathbf{E}$$

Where d is a function of the propagation delays of the gates ($\varepsilon_1, \varepsilon_2, \ldots \varepsilon_N$)
Hence, the decision variables are $\varepsilon_1, \varepsilon_2, \ldots \varepsilon_N$

- We model this optimization problem as a geometric program*
  - The objective function and constraints in a geometric program have to be posynomials
    - A posynomial is a special kind of positive polynomial
  - We use certain well known approximations to represent our objective function as a posynomial
    - We have to perform iterative geometric programming until the solution converges
- Geometric programming is a special case of convex optimization
  - Therefore there are very efficient algorithms which solve a geometric program
- We use a standard geometric programming toolbox to find the solution to our problem
- There is another constraint to the optimization problem
  - Limit the propagation delays of the gates to be between the permissible limits allowed by the process technology
    - In our case, this is 90nm

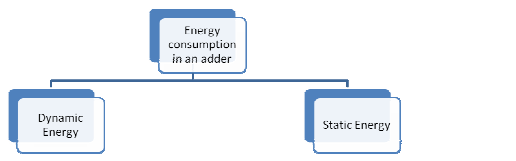
- Given
  - The 3-bit RCA circuit with XOR and MUX gates
  - Clock cycle time (T) = 120 ps
  - Energy Budget (**E**) = 11.1 fJ

Gate Index	ϵ_l (ps)	v_l (volts)	Binned v_l (volts)
1	44.6	0.84	0.8
2	46.9	0.8	0.8
3	34.0	1.16	1.2
4	44.6	0.84	0.8
5	40.8	0.92	0.9
6	33.3	1.2	1.2
7	39.3	0.96	1.0
8	38.5	0.98	1.0
9	33.3	1.2	1.2

Binned voltages
Chosen from a set of 4 specific voltages

From the geometric program

Energy Model



$$E^D = \sum_{l=1}^{N} E_l^D(v_l) W_l \qquad E^S = \sum_{l=1}^{N} P_l^S(v_l) T$$

Switching energy consumption of gate "l" at voltage "v_l"
Average switching activity of gate "l" – calculated through simulations
Average leakage power of gate "l" at voltage "v_l"
Clock cycle time of the adder

For an approximate adder, the main difference is in the switching activities while computing the dynamic energy consumption

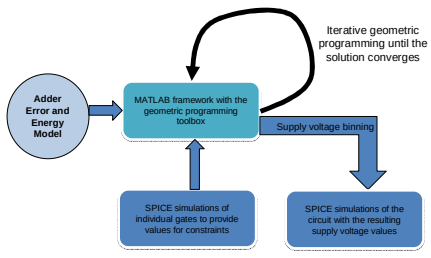
Because of over-clocking, the switching activities might reduce for certain gates

We use the same indicator function to check if the outputs of the gates switched for a given carry chain and clock cycle time.

Approximate adder energy consumption $E^A = \sum_{l=1}^{N} \left(E_l^D(v_l) W_l^A + P_l^S(v_l) T \right)$

Corrected switching activity for gate "l"

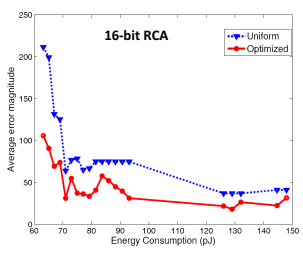
Simulation Methodology

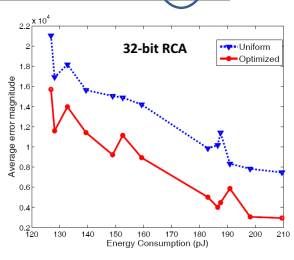


- Three cases of comparison
  - UVoS – Uniform voltage scaled approximate adder
  - N-BiVoS – Naïve Biased Voltage Scaling
    - Current best in literature : Ad-hoc assignment of voltages
  - BGPS – Binned Geometric Program Solution

Simulation Results

n-bit	*D* (ns)	Average Error Magnitude					Energy Consumption (fJ)	Energy Savings
		UVoS	n-BiVoS	BGPS	UVoS /BGPS	n-BiVoS /BGPS		
16-bit	0.4	36.83	50106	71.66	1.40	2.31	110.78	1.41
16-bit	0.4	36.83	45.97	17.96	2.05	2.56	128.14	1.22
16-bit	0.4	36.83	36.83	20.31	1.81	1.81	132.9	1.18
16-bit	0.4	40.92	36.83	23.25	1.76	1.58	139.92	1.12
32-bit	0.6	18171	33704	13978	1.30	2.41	132.74	2.07
32-bit	0.6	15634	24637	11412	1.37	2.16	139.41	1.97
32-bit	0.6	14892	15215	11142	1.34	1.37	152.54	1.8
32-bit	0.6	14199	10931	8931	1.59	1.22	159.3	1.73





Primary References

•Lakshmi N. B. Chakrapani, Kirthi Krishna, Lingamneni Avinash, Jason George, Krishna Palem, "Highly Energy and Performance Efficient Embedded DSP through "Somewhat" Erroneous Arithmetic", *International conference on Compilers, Architectures, and Synthesis for Embedded Systems*, Atlanta, GA, 2008.
•K.V. Palem, S. Cheemalavagu, P. Korkmaz, and B.E.S. Akgul, "Probabilistic and Introverted Switching to Conserve Energy in a Digital System," US Patent application, 27 Apr. 2005
•Zvi M. Kedem, Vincent John Mooney, Kirthi Krishna Muntimadugu, Krishna V. Palem, Avani Devarasetty, Phani Deepak Parasuramuni: Optimizing energy to minimize errors in dataflow graphs using approximate adders. *International conference on Compilers, Architectures, and Synthesis for Embedded Systems*, 2010,177-186