MODELING MULTI-OUTPUT FILTERING EFFECTS IN PCMOS

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ABSTRACT

A methodology has been proposed recently to predict error rates of cascade structures of blocks in Probabilistic CMOS (PCMOS). It requires characterization of unique probabilistic blocks to predict the error rates of a multi-block cascade structure. While the technique was shown to work for a probabilistic carry-select adder [4, 5], the technique needs a new model to work in a Wallace Tree Multiplier (WTM) where error propagates not only along the carry bit but also along the sum bit of the basic full adder building block utilized. In this paper we present a new model for characterization of probabilistic circuits/blocks and present a procedure to find and characterize unique circuits/blocks. Unlike prior approaches, our new model distinguishes distinct filtering effects per output. We apply the proposed model to a WTM and show that using our model, the methodology using a cascade structure [4] can predict WTM error-rates with reasonable accuracy in PCMOS.

I. INTRODUCTION

The ability to scale CMOS technology has been one of the major reasons for its wide use in building complex digital VLSI circuits. However, as transistor dimensions reduce, statistical behaviors such as noise, parametric variations, defects, etc., become more prominent. Instead of spending disproportionate effort to avoid errors completely, Probabilistic CMOS (PCMOS) computing proposes to include occasional errors caused by erroneous chips [1] with potential trade-offs between correctness of circuit operation and traditional measures of performance. It has been shown that a small amount of error can potentially be traded off for significant power savings [2] or increased circuit speeds [3].

Quick and accurate prediction of error-rates is essential for systematic design and performance evaluation of probabilistic circuits. The major need for prediction comes from the fact that the present generation low level circuit simulators like HSPICE are prohibitively time consuming. Recently, a methodology has been proposed in [4] to quickly predict the error rates of cascade structures of blocks as shown in Fig. 1. The methodology consists of two main steps, (i) characterization of each unique probabilistic block and (ii) evaluation of mathematical equations that model the dynamics of error propagation across the blocks. In short, a block is a collection of circuit elements with no restrictions on the number of inputs, outputs and type of circuit elements; note that characterization of a probabilistic block means to determine the block's output error probabilities. Information obtained from characterization of blocks is used to predict the error-rate of a multi-block circuit. In this paper we will refer to the methodology of [4, 5] as the cascade math model.

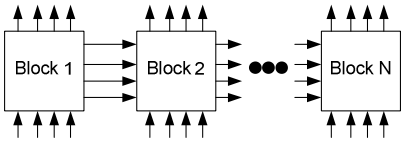

Figure 1. Cascade Structure of Blocks

The most important factor on which the success of the cascade math model [4] depends is the characterization of unique blocks. Since the methodology uses only this information to predict the error-rates of the whole circuit, improper characterization of blocks can lead to wrong predictions. The model that has been used for characterizing circuits and blocks in [4, 5] is explained in [6]. [6] shows the importance of the noise filtering effect [7] while characterizing circuits and adds a properly sized buffer after a probabilistic circuit to take into account the filtering effect of the load circuit.

The model in [6] works well for one dimensional circuits such as ripple carry adders, carry-select adders, etc., but breaks down for complex two dimensional circuits like multipliers. The major reason for its breakdown is that it neglects the fact that a circuit with multiple outputs while filtering a noisy input shows different filtering effects at its different outputs. Although this happens in one dimensional circuits also, the effect is not of first order as is the case with two dimensional circuits. In short, we found that the cascade math model of [4] with the probabilistic block characterization of method of [6] does not work well with a Wallace Tree Multiplier (WTM), therefore, this paper presents a new block characterization method which works with a WTM and for which [6] is a subset.

In this paper, we present a new model for characterizing probabilistic circuits/blocks which accounts for the different filtering effects seen in circuits with multiple outputs. The new model also serves as a criterion for identifying unique circuit elements/blocks in a multi-block probabilistic circuit. For complex 2-D structured circuits where differentiation of circuit elements in terms of their probabilistic behavior is not very obvious, this extra property of the new model becomes a real advantage over the previous model [6]. We apply the proposed model to a WTM, one of the most widely used arithmetic circuits and also a somewhat irregular circuit in terms of structure, and predict the error-rates. To the best of the authors' knowledge, this is the first instance of prediction of errors in a complex 2-D circuit, i.e., a WTM, with the cascade math model.

The rest of the paper is organized as follows. Section II proposes the new model for characterizing probabilistic circuit elements and gives the procedure for finding unique circuit elements in a probabilistic circuit. Section III shows the decomposition used for the WTM to allow the cascade math model to predict its bit error rates. Section IV applies the proposed models and the cascade math model to 4x4 and 6x6 WTMs and compares the predicted bit error rates with results obtained from HSPICE simulations. Section V concludes the paper.

II. A NEW MODEL FOR NOISE BASED PROBABILISTIC CIRCUITS

In this section we first discuss different filtering effects seen in noise based PCMOS circuits and then propose a new model for characterizing such circuits. Finally, we show a procedure for finding unique circuit elements with the proposed model.

A. Filtering Effects in Noise Based Probabilistic Circuits

There are two major types of filtering effects seen in noise based probabilistic circuits.

1) Filtering due to Propagation Delay:

Noise filtering happens when the duration of a noise pulse is shorter than the propagation delay of the circuit [7]. Here, propagation delay

of the circuit plays the major role in filtering noise. If one of the inputs of the circuit is noisy and the circuit has more than one output, then different outputs show different errors depending upon the loads the outputs are driving and the path from the noisy input to the outputs. Since different paths have different delays, different outputs show different noise filtering effects.

2) Logical Masking:

In digital circuits, when one or more of the inputs independently determines the output, then the change of logic values at the other inputs do not affect the output. For example, in a full adder (FA) an input logic combination of 00(11) determines the logic value of carry out as 0(1) independently of the third input. If the circuit is in such a state, then the errors from remaining inputs do not affect the output and hence are masked out by the circuit.

B. Characterizing Probabilistic Circuit Elements (PCEs)

To predict the error rate of a probabilistic circuit (PrC), our mathematical model [4] needs the error-rate(s) associated with each unique probabilistic circuit element (PCE) constituting that PrC. By unique PCE we mean a PCE whose error-rates are different from that of the other PCEs constituting that PrC. Determining error rates of PCEs is called characterization of probabilistic circuit elements [4, 5, 6]. Once the error rates of unique PCEs are known, the math model can predict the error rate of the PrC. In our earlier work [4, 5, 6], we did not account for the differences in the delays of the carry and sum bits. This was adequate for modeling a ripple-carry adder or similar structure. When applying the methodology to a more complex structure such as a WTM, these differences need to be accounted for. Hence, in this paper we propose a new model for characterizing PCEs**.**

C. A New Model for Characterizing PCEs

We have found empirically that the design of the following three components play a central role in the probabilistic response of a circuit.

1) *The Probabilistic Circuit Element Under Characterization (PCEUC):* Different circuits have different probabilistic responses to inputs.
2) *The Load of the PCEUC or Filter Circuit (FC):* We will refer to the load of a PCEUC as a Filter Circuit since it acts as a filter for the errors generated by the PCEUC. Different circuits have different filtering capability.
3) *The Load of the Load of the PCEUC or Load of Filter Circuit (LOFC):* The propagation delay of the filter circuit determines its filtering capability. It is known that the load of a circuit plays a major role in its propagation delay. Hence, the load of the filter circuit becomes important while characterizing a PCEUC.

The proposed model is a three stage model and is shown in Fig. 2. Instead of using a variably sized buffer as the FC [6], the new model uses circuit elements from the actual design itself to model circuits and hence is a very straightforward model. To avoid logical masking, the inputs of the FC which are not fed by PCEUC should be in a state where the FC outputs reflect the effect of noisy input from PCEUC.

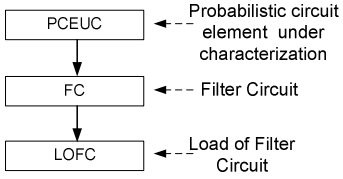

Figure 2. Proposed Three Stage Model for Circuits

Note that to simulate PrCs we use two buffers at each output of the PrC to capture their error rates; Fig. 3 shows the usage for WTM. The first buffer models the filtering effect of flip flops [6] while the second buffer is used for loading.

D. Finding Unique PCEs in a PrC

Since we need to characterize only unique PCEs for PrC error rate prediction, our proposed three stage model, Fig. 2, also becomes the criteria to differentiate PCEs based on their probabilistic behavior. We first create three stage models to cover all of the PCEs in a PrC; then, we compare these models with each other. If one or more elements in a particular three stage model are different, we have found a unique PCE.

We use a 4x4 WTM to illustrate the procedure for finding unique PCEs in a PrC. Fig. 3 shows a 4x4 WTM (PrC). We create the three stage models of all the FAs (PCEs) in the WTM and compare them to find the unique three stage models. Please note that, for simplicity, AND gates in the WTM are treated as deterministic circuits and hence are not PCEs. In Fig. 3 the FAs are labeled as N1-N2 where number N1 is used to differentiate the 12 FAs and N2 is used to differentiate them based on their probabilistic behavior (unique PCEs). Fig. 4 shows the three stage models of unique FAs in the 4x4 WTM, and the models are labeled with the same number N2 in Fig. 3. For example, Model-1 in Fig. 4 models FA 1-1 and FA 2-1 in Fig. 3.

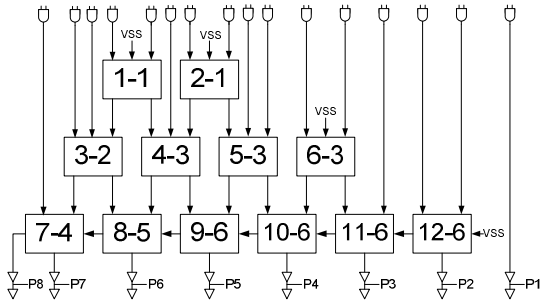

Figure 3. 4x4 Wallace Tree Multiplier

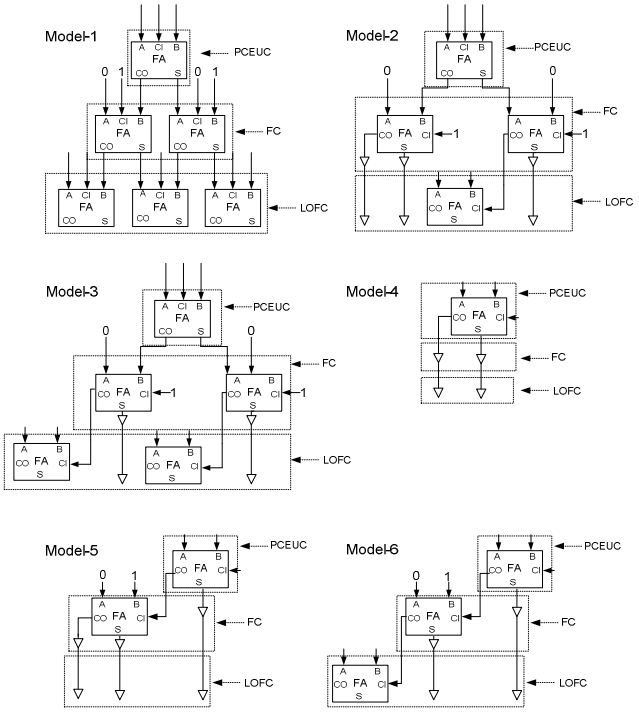

Figure 4. The Three Stage Models of FAs of WTM

E. Procedure for Characterizing PCEs

Characterization of PCEs is done by HSPICE simulations as described in detail in Section IV. We perform the experiment shown in Fig. 5. We have two duplicate three stage models of the circuit element under characterization (CEUC). One model is probabilistic (PCEUC) and produces noisy output while the other is deterministic (DCEUC), producing deterministic output. A probabilistic circuit is constructed from the deterministic circuit by adding equivalent noise sources at each of the outputs of the circuit [4, 5, 6]. Fig. 6 shows a probabilistic FA used in a probabilistic WTM. Note that FCs and

LOFCs for the two duplicates are kept deterministic so that we capture only the filtering effect of the filter circuit; also, the FCs are kept in such a state that there is no logical masking. For example, in an FA, sum is always sensitive to the inputs, but carry out can be logically masked. Hence, when a particular FA functions as an FC as occurs in models 1, 2, 3, 5 and 6 in Fig. 4, to avoid such masking we use 01 or 10 logic combination for the two FA inputs which are not driven by the noisy output of PCEUC. The two duplicates – PCEUC and DCEUC – are simulated with a large number of inputs (typically 100,000), and the outputs of the two filter circuits (FC) are compared as shown in Fig. 5. A mismatch in the digital result is treated as an error. We calculate the number of errors per output of the FC to determine the error-rate and assign it as the error rate of the output of PCEUC driving that FC. If an FC has, say, *n* outputs, then we assign *n* error rates to that specific PCEUC output corresponding to each output of FC. For example, the PCEUCs of models 1, 2 and 3 of Fig. 4 will have two error rates for each of their outputs since the filter gate of both of the outputs is an FA which has two outputs while the PCEUC of Model-4 will have only one error rate for each of its outputs. In fact, one can observe in Fig. 3 of [6] the case shown in Model-4; in short, this paper subsumes [6] as a special case.

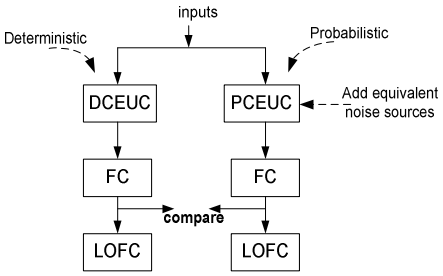

Figure 5. Characterizing PCEs

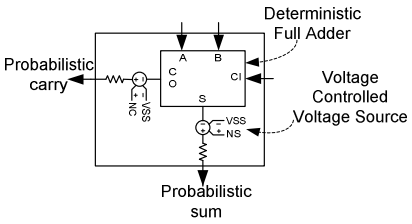

Figure 6. Probabilistic Full Adder

III. WTM FOR THE CASCADE MATH MODEL

The cascade math model [4] predicts error rates of multi block cascade structures and requires error rates of unique blocks for prediction. Since blocks are basically collections of circuit elements, PCEs in the previous section can be treated as blocks for the cascade math model and the PrC as the overall multi block structure design. All the techniques mentioned in the previous section for PrCs and PCEs are valid for multi-block cascade structures and blocks, but the techniques should be applied after creating the blocks and the cascade structure for each PrC.

We have decomposed the 4x4 WTM into a cascade such that each block contains only one full adder. Fig. 3 shows a 4x4 WTM, and Fig. 7 shows its mapping to a cascade structure where each block contains only one Full Adder (FA). Since each block here is an FA, we obtain the same unique PCEs whose three stage models are shown in Fig. 4 as the unique blocks of the multi-block cascade structure of the 4x4 WTM. In performing this decomposition for 6x6 WTM, 8x8 WTM, etc., we discovered that the six unique blocks (models) for the 4x4 WTM as shown in Fig. 4 are the only unique blocks (models) for any bit width WTM if decomposed into a cascade structure with each block containing only one FA. Hence, error-rates of any bit-width WTM can be predicted by characterization of these six unique blocks (models).

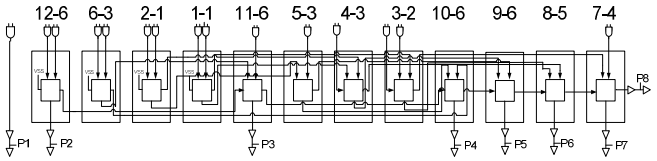

Figure 7. Cascade Structure of a 4x4 Wallace Tree Multiplier

A. WTM Implementation for the Cascade Math Model

In a WTM, we find two types of FCs, one is a full adder (FA) with two outputs and the other is a buffer with only one output. For cases where an FA acts as a Filter Circuit (FC), the sum and carry outputs each have different timing behavior (due to different transistor network) as well as may have different loads (LOFCs); as a result, in general, we have two error-rates for each input to an FA. To make our math model [4] take this into account, we describe each FA in our WTM as a 6-input and 4-output circuit as shown in Fig. 8. The reason for such an FA is explained in the next paragraph. For simplicity, even an FA with buffers as filters is treated as a 6-input and 4-output circuits, but the redundant outputs are neglected in the math model calculations.

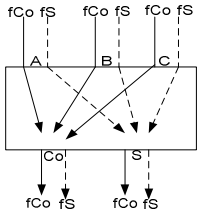

Figure 8. Full Adder of a WTM for Cascade Math Model

In Fig. 8, fCo stands for FOR_CARRYOUT, and fS stands for FOR_SUM; fCo and fS are used to denote in the math model that a particular FA input or output in fact has two error-rates associated with the input or output based on which signal path (sum or carry) is exercised. Out of the 6 inputs shown in Fig. 8, 3 inputs (fCo) are used by the math model for calculation of probabilities of the two carry outs (one for the carry out of the next FA, fCo, and the other for the sum, fS) and the other three inputs (fS) are used for the calculation of probabilities of two sums (again, one for the carry out of next FA and the other for the sum). The major reason to have a 6-input 4-output FA is because our math model calculates the joint probabilities of the outputs to take care of the re-convergent fan-out issues present in circuits [4], and hence to calculate the two fCOs (fSes) of Co and S, we need the error probabilities of the six inputs. 4x4 WTM for the cascade math model can be visualized as in Fig. 3 but with all the inputs and outputs as 2 bits wide and the description of its cascade structure as in Fig. 7 but again with 2 bit wide inputs and outputs. Please note that FA used in our WTM is a mirror adder which is almost symmetric for all inputs (A, B, Cin) and hence the filtering effect on errors from any input (A, B, Cin) to Co or to S is nearly the same; thus we do not differentiate error rates based on the FA inputs.

IV. HSPICE SIMULATIONS AND RESULTS

In this section, by HSPICE simulation, we validate the proposed model for blocks and the cascade math model for predicting error rates of a Wallace Tree Multiplier. In particular, we simulate 4x4 and 6x6 probabilistic WTM designs in HSPICE and use the cascade math model and the proposed models for predicting error rates of the product bits of each WTM. We show that using our models proposed in this paper, error rates of WTMs can be predicted with reasonable accuracy.

A. Simulating a Probabilistic Wallace Tree Multiplier

Following [2, 5, 6], we construct a probabilistic circuit by adding noise sources at the outputs of the initial deterministic circuit. We use Synopsys 90nm generic library for simulations. Noise sources are voltage controlled voltage source (VCVS) with a small resistor in

series (typically 1 ohm). Fig. 6 shows a probabilistic Full Adder (FA) used in a WTM. The random noise data for the noise sources are generated by MATLAB and have a Gaussian distribution with zero mean and non-zero root-mean-square (RMS) value. Following [4], we use 0.2V as the RMS value. This is intended to model a possible thermal noise in a future transistor technology, e.g., 12nm.

Probabilistic WTMs are constructed from probabilistic FAs. To keep the simulations, cascade structure and the math model simple, AND gates in the WTMs are kept deterministic. Inputs to the WTM are uniformly distributed random bits and are obtained from MATLAB. We simulate 4x4 and 6x6 WTM designs with 100,000 samples each. The inputs are fed to a 4x4 WTM at a clock period of 2ns and to a 6x6 WTM at a period of 4ns, and the noise samples are added to the outputs of each probabilistic Full Adder in each multiplier every 0.5ns. For 90nm technology, the nominal voltage of operation is 1.2V. Hence, we simulate the two WTM designs for five voltages which are 0.8, 0.9, 1.0, 1.1 and 1.2V. We obtain the error probabilities of the final product bits of the two WTMs for each of the five respective voltages.

B. Block Characterization

The experimental setup for block characterization is as described in Section II-E. The six unique blocks (models) mentioned in Section III and shown in Fig. 4 are simulated for five voltages (0.8 to 1.2V) for 100,000 samples for each voltage, and the error probabilities are obtained for random input patterns. The sample period is kept at 2ns and noise samples are added at every 0.5ns. The other details of the simulation are as in Section IV-A.

C. Results

The characterization results of the unique blocks of a WTM are used to predict the error-rates of 4x4 and 6x6 WTMs by the cascade math model. For mathematical prediction, we use the cascade structure shown in Fig. 7 for a 4x4 WTM and a similar structure for a 6x6 WTM. The implementation of the cascade math model is done in MATLAB. The results from prediction and HSPICE simulations are shown for a 4x4 WTM in Fig. 9 and for a 6x6 WTM in Fig. 10. The results obtained from prediction using the proposed model are labeled as *Prediction (3-stage)* and the HSPICE results are labeled as Simulation in the figures. Please note that P1 is the output of an AND gate and not a probabilistic Full Adder, hence the error rate for P1 is zero for all the voltages. For comparison, results obtained by utilizing the previous model with buffers [6] are also shown in the figures with dashed lines and are labeled as *Prediction (2-stage)*.

As can be seen from the figures, the predicted results from the proposed models are closer to the simulated results from that of the previous model. For our 4x4 WTM results, the average relative deviation of the predicted results from HSPICE results is under 7% and for a 6x6 WTM the deviation is under 8.5%. The average relative deviation of HSPICE results from the predicted results obtained using previous model is around 24% for a 4x4 WTM and 27% for a 6x6 WTM.

To give an idea about the computation time, the time taken by HSPICE to calculate the error rates of a 4x4 WTM for one voltage is 88300 seconds (1 day) and 264700 seconds (3 days) for a 6x6 WTM. The math model predicts the error rates of a 4x4 WTM in 1404 seconds and a 6x6 WTM in 3390 seconds. Time taken for characterization of blocks is not included in the math model prediction time because it is a one-time investment for prediction of *n* different WTMs.

V. CONCLUSION

We have proposed a new model for characterization of PCMOS circuits/blocks and have provided a procedure for finding and characterizing such blocks in a multi-block circuit. We have shown that using our proposed model, the cascade math model can predict the error-rates of WTM reasonably accurately. For our future work, we plan to extend our model to circuits with different topologies like Kogge-Stone adders, Dadda multipliers, etc.

VI. ACKNOWLEDGMENT

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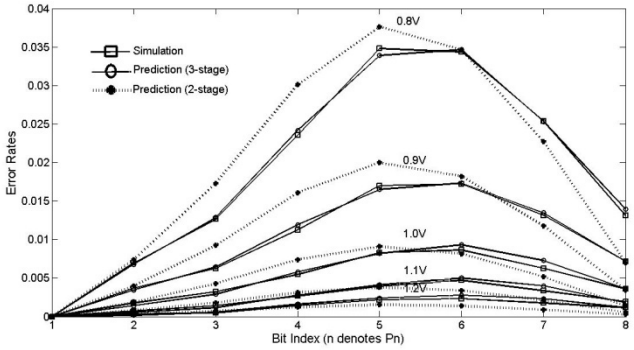

Figure 9. 4x4 WTM Error-Rates

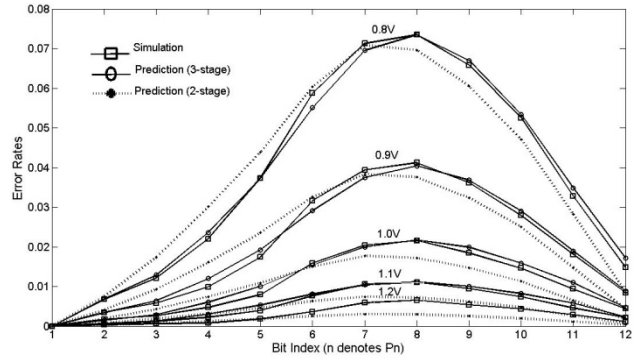

Figure 10. 6x6 WTM Error-Rates

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