On the Calculation of Noise in Multistage Amplifiers

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Abstract—**It is shown that it can be a fallacy that the noise figure of a multistage amplifier is primarily determined by the noise figure of the first stage if the available power gain of the first stage is sufficiently high. The expression for the equivalent input noise voltage of a multistage amplifier is derived, where each stage is represented by the $V_n - I_n$ amplifier noise model. It is shown that the noise contributed by stages following the first stage is lowest when the first stage has a high transconductance, an input resistance that is high compared to the source resistance, and a high open-circuit voltage gain. In addition, the second stage must have a low input current noise. Circuit topologies which meet these conditions are described.**

I. Introduction

The concept of noise figure (also called noise factor) was introduced in the 1940's as a method of specifying the noise performance of RF receivers [1], [2]. The noise figure F of a two-port network is defined by

$$F = \frac{N_{ao}}{N_{aos}} \tag{1}$$

where N_{ao} is the incremental available noise output power from the network and N_{aos} is that part of N_{ao} caused by the source which drives the network [3]. The units of N_{ao} and N_{aos} are W/Hz. The noise figure is often specified in decibels by the relation $10\log(N_{ao}/N_{aos})$.

The incremental available output power from any network is defined as the maximum value of the output power per unit bandwidth. This is the output power per unit bandwidth delivered to a load impedance equal to the complex conjugate of the output impedance of the network.

Fig. 1 illustrates the cascade connection of N two-port networks. Let the j-th stage have the noise figure F_j. The noise figure of the cascade connection is given by [3]

$$F = F_1 + \frac{F_2 - 1}{G_{a1}} + \frac{F_3 - 1}{G_{a1}G_{a2}} + \cdots + \frac{F_N - 1}{G_{a1}G_{a2}\cdots G_{a(N-1)}} \tag{2}$$

where G_{aj} is the available power gain of the j-th stage. The available power gain is defined by

$$G_a = \frac{P_{ao}}{P_{as}} \tag{3}$$

where P_{ao} is the incremental available output power in response to a specific source and P_{as} is the incremental available input power from that source. The units of P_{ao} and P_{as} are W/Hz.

If G_{a1} is sufficiently large, (2) seems to imply that the noise figure F is primarily determined by the noise figure F_1 of the first stage. This conclusion is often applied in the noise analysis of multistage amplifiers to justify neglecting the noise of all stages following the first stage [3]–[7]. However, this is not necessarily correct. For example, an increase in G_{a1} can cause an increase in F_2 so that the term $(F_2 - 1)/G_{a1}$ in (2) approaches a nonzero limit as $G_{a1} \to \infty$. In this case, the noise figure of the amplifier may not be primarily determined by the noise figure of the first stage.

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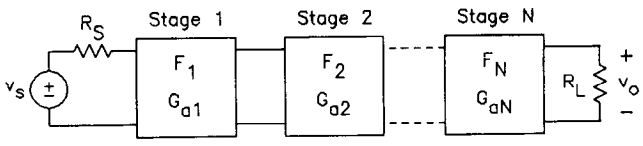

Fig. 1. N-stage amplifier, with each stage having a noise figure F and an available power gain G_a.

This paper investigates the noise analysis of multistage amplifiers. The analysis is directed toward low-frequency analog circuits so that frequency response effects can be neglected. The noise generated by each stage is modeled by a series input voltage and a shunt input current. Conditions are identified for which the noise generated by the stages following the first stage can be neglected. Possible circuit topologies which meet these conditions are identified.

II. A Noise Figure Fallacy

The noise generated by any amplifier can be modeled by two noise sources at its input. One is a series voltage source and the other is a shunt current source. Two noise sources are required in order for the sources to be independent of the output impedance of the network which drives the amplifier [8], [9]. In general, the correlation coefficient between the two sources is not zero. The model is called the $V_n - I_n$ amplifier noise model.

Fig. 2 illustrates a cascade connection of N amplifier stages, where each stage is modeled with the $V_n - I_n$ model. All sources represent instantaneous values. The voltage v_{ts} is the thermal noise generated by the source resistance R_S. For the j-th stage, v_{nj} is the series input noise voltage, i_{nj} is the shunt input noise current, R_{ij} is the input resistance, R_{oj} is the output resistance, and i_{oj} is the short-circuit output current. The latter can be written $i_{oj} = g_{mj}v_{ij}$, where g_{mj} is the transconductance and v_{ij} is the voltage across R_{ij}.

The noise figure of the amplifier is given by (2). Consider the case $N = 2$. It is straightforward to show that F_1, G_{a1}, and F_2 are given by

$$F_1 = 1 + \frac{\langle (v_{n1} + i_{n1}R_S)^2 \rangle}{\langle v_{ts}^2 \rangle} \tag{4}$$

$$G_{a1} = \left(\frac{R_{i1}}{R_S + R_{i1}}\right)^2 g_{m1}^2 R_S R_{o1} \tag{5}$$

$$F_2 = 1 + \frac{\langle (v_{n2} + i_{n2}R_{o1})^2 \rangle}{\langle v_{to1}^2 \rangle} \tag{6}$$

where the symbols $\langle\cdot\rangle$ represent the time average or mean value of the quantity enclosed. In (6), the term $\langle v_{to1}^2 \rangle$ represents the mean-square thermal noise voltage generated by a resistor of value R_{o1}, i.e., a resistor having a value equal to the source resistance seen by the second stage. This noise is not represented by a source in Fig. 2 because it is only used in the definition of F_2.

The mean-square thermal noise voltage generated by any resistor R is given by $\langle v_t^2 \rangle = 4kTR\Delta f$, where k is Boltzman's constant, T is the absolute temperature, and Δf is the bandwidth in Hz over which the noise is measured [3]. It follows that $\langle v_{to1}^2 \rangle$ in (6) can be written

$$\langle v_{to1}^2 \rangle = \frac{R_{o1}}{R_S} \times 4kTR_S\Delta f = \frac{R_{o1}}{R_S}\langle v_{ts}^2 \rangle \tag{7}$$

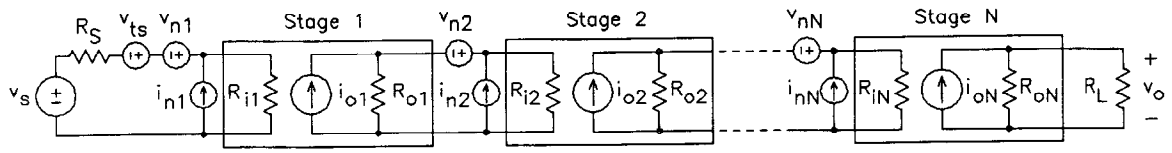

Fig. 2. N-stage amplifier with each stage modeled by the $V_n - I_n$ amplifier noise model.

where $\langle v_{ts}^2 \rangle = 4kTR_S\Delta f$. Thus an alternate expression for F_2 is

$$F_2 = 1 + \frac{R_S}{R_{o1}} \times \frac{\langle (v_{n2} + i_{n2}R_{o1})^2 \rangle}{\langle v_{ts}^2 \rangle} \tag{8}$$

For $R_{o1} \to \infty$, it follows from (5) and (8) that

$$\lim_{R_{o1}\to\infty} G_{a1} = \infty \tag{9}$$

$$\lim_{R_{o1}\to\infty} \frac{F_2 - 1}{G_{a1}} = \left(1 + \frac{R_S}{R_{i1}}\right) \frac{\langle i_{n2}^2 \rangle}{g_{m1}^2 \langle v_{ts}^2 \rangle}. \tag{10}$$

It is clear that $(F_2 - 1)/G_{a1}$ is not necessarily small compared to F_1 even though G_{a1} is infinite. It follows that the noise generated by the second stage cannot be neglected, in general, if the available power gain of the first stage is large. In RF circuit design, this fallacy may not arise when circuits are designed for a fixed output impedance. In analog circuit design, however, the output impedance of a stage can be very low to very high, depending on the topology. In this case, it can be a fallacy to assume that the noise generated by stages following the first stage can be neglected if the available power gain of the first stage is high.

III. Equivalent Noise Input Voltage

Let the open-circuit input voltage to the j-th stage in Fig. 2 be denoted by $v_{ij(oc)}$. This is the input voltage with R_{ij} open circuited. The short-circuit output current can be written

$$i_{oj} = G_{mj} v_{ij(oc)} \tag{11}$$

where G_{mj} is the transconductance gain defined by

$$G_{mj} = g_{mj} \frac{R_{ij}}{R_{o(j-1)} + R_{ij}} \tag{12}$$

and $R_{o(j-1)} = R_S$ for $j = 1$. The ratio of the open-circuit output voltage to the open-circuit input voltage is given by $G_{mj}R_{oj}$. It follows that the overall voltage gain of the amplifier is given by

$$A_v = \frac{v_o}{v_s} = G_{m1}R_{o1}G_{m2}R_{o2} \cdots G_{mN}(R_{oN} \| R_L). \tag{13}$$

With these definitions, the instantaneous amplifier output voltage can be written

$$v_o = A_v \Bigg[v_s + v_{ts} + v_{n1} + i_{n1}R_S + \frac{v_{n2} + i_{n2}R_{o1}}{G_{m1}R_{o1}} + \frac{v_{n3} + i_{n3}R_{o2}}{G_{m1}R_{o1}G_{m2}R_{o2}} + \cdots + \frac{v_{nN} + i_{nN}R_{o(N-1)}}{G_{m1}R_{o1}G_{m2}R_{o2} \cdots G_{m(N-1)}R_{o(N-1)}} \Bigg]. \tag{14}$$

Let v_{ni} be the instantaneous equivalent noise voltage in series with the input which generates the same noise at the output. It follows from (14) that this is given by

$$v_{ni} = v_{ts} + v_{n1} + \frac{v_{n2}}{G_{m1}R_{o1}} + \frac{v_{n3}}{G_{m1}R_{o1}G_{m2}R_{o2}} + \cdots + \frac{v_{nN}}{G_{m1}R_{o1}G_{m2}R_{o2} \cdots G_{m(N-1)}R_{o(N-1)}} + i_{n1}R_S + \frac{i_{n2}}{G_{m1}} + \frac{i_{n3}}{G_{m1}R_{o1}G_{m2}} + \cdots + \frac{i_{nN}}{G_{m1}R_{o1}G_{m2}R_{o2} \cdots G_{m(N-1)}}. \tag{15}$$

If G_{m1} is sufficiently large, it can be seen from this equation that v_{ni} is primarily determined by the noise of the first stage. It follows from (12), that G_{m1} cannot be large unless g_{m1} is large. This is a condition that can be difficult to achieve in practice.

A BJT biased at the collector current $I_C = 1$ mA has a transconductance $g_m = I_C/V_T = 0.0386$ S, where $V_T = 0.0259$ V is the thermal voltage at $T = 27^0$ C. The transconductance of a FET is smaller typically by a factor of 10 or more. It can be concluded that it can be difficult in general to design a multistage amplifier for which the noise is primarily determined by the first stage if the only requirement for that stage is a large g_m.

IV. Conditions For Minimum Noise

Examination of (15) shows that all noise terms due to the stages which follow the first stage, with the exception of the i_{n2} term, are inversely proportional to the first-stage open-circuit voltage gain $G_{m1}R_{o1}$. If this gain is sufficiently large, these noise terms can be neglected. To maximize the first-stage open-circuit voltage gain, the product $G_{m1}R_{o1}$ must be maximized. This can be achieved only if the stage has a high output resistance. That is, its output circuit should look like a high-resistance current source. For a BJT first stage, the highest small-signal output resistance is obtained with the common-emitter (CE) and common-base (CB) configurations. Similarly, for a FET first stage, the highest small-signal output resistance is obtained with the common-source (CS) and common-gate (CG) configurations.

To minimize the i_{n2} term in (15), G_{m1} must be maximized and the second stage must exhibit a low input current noise. It follows from (12) that G_{m1} is maximized when the input device has a high transconductance and an input resistance that is high compared to the source resistance. The current noise of the second stage is minimized by selecting a second stage device which exhibits a low input current noise. Because the FET exhibits essentially zero current noise, it is the preferred device for the second stage. Practical considerations demand that this stage be connected in the common-gate configuration. Otherwise, a shunt bias coupling network could be required between the two stages which would increase the noise. An additional advantage of the CG second stage is that its small-signal input resistance is low. This makes the loaded voltage gain of the first stage low, thus reducing the Miller effect and increasing the bandwidth.

Fig. 3 shows the topologies which minimize the noise contributed by the second stage. In Fig. 3(a), the first stage is a BJT stage. For

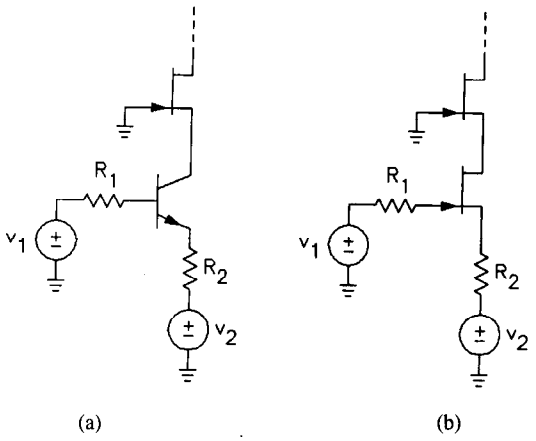

Fig. 3. Topologies for the first two stages of a multistage amplifier which minimize the noise contributed by stages following the first stage.

$v_2 = 0$, the BJT operates as a CE amplifier with a source resistance $R_S = R_1$. For $v_1 = 0$, it operates as a CB amplifier with a source resistance $R_S = R_2$. For both configurations, it can be shown that G_{m1} and $G_{m1}R_{o1}$ are approximately given by

$$G_{m1} = \left(\frac{R_1 + r_x}{\beta} + \frac{R_2}{\alpha} + \frac{V_T}{I_C}\right)^{-1} \tag{16}$$

$$G_{m1}R_{o1} = \frac{V_A + V_{CB}}{V_T + I_C(R_1 + r_x + R_2)/\beta} \tag{17}$$

where α and β are the BJT current gains, r_x is the base spreading resistance, I_C is the collector bias current, V_A is the early voltage, V_{CB} is the collector-to-base bias voltage, and V_T is the thermal voltage. Because $\beta \gg \alpha$, it follows from (16) that G_{m1} is maximized for the CE configuration with $R_2 = 0$. If the source resistance is zero, both configurations give the same values for G_{m1} provided the resistance in series with the unused input is zero. For both configurations, the value of $G_{m1}R_{o1}$ is maximized when the resistance in series with the unused input is zero. In addition, the BJT should have a large β and a large V_A.

In Fig. 3(b), the first stage is a FET stage. For $v_2 = 0$, the FET operates as a CS amplifier with a source resistance $R_S = R_1$. For $v_1 = 0$, it operates as a CG amplifier with a source resistance $R_S = R_2$. For both configurations, it can be shown that G_{m1} and $G_{m1}R_{o1}$ are approximately given by

$$G_{m1} = \left(R_2 + \frac{1}{2\sqrt{KI_D}}\right)^{-1} \tag{18}$$

$$G_{m1}R_{o1} = 2\sqrt{\frac{K}{I_D}}\left(\frac{1}{\lambda} + V_{DS}\right) \tag{19}$$

where K is the FET transconductance parameter, I_D is the drain bias current, λ is the channel length modulation parameter, and V_{DS} is the drain–to-source bias voltage. It follows from (18) that G_{m1} is maximized when the input stage is operated as a CS amplifier with $R_2 = 0$. In the case that the source resistance is zero, both configurations give the same values for G_{m1}. The value of $G_{m1}R_{o1}$ is the same for both configurations and is independent of the source resistance and the resistance in series with the unused input. It is maximized when the FET has a large K and a small λ.

V. Conclusions

If the available power gain of the first stage of a multistage amplifier is high, it can be a fallacy to assume that the noise generated in the following stages can be neglected. The equivalent input noise voltage of a multistage amplifier is primarily determined by the first stage when that stage has a high transconductance, an input resistance that is high compared to the source resistance, and a high open-circuit voltage gain. In addition, the second stage must have a low input current noise. Circuit topologies for the first two stages which minimize the noise contributed by stages following the first stage are a CE or CB BJT stage followed by a CG FET stage and a CS or CG FET stage followed by a CG FET stage. Unless the source resistance is very small, the CE and CS configurations for the first stage are preferred.

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An Optimized Compensation Strategy for Two-Stage CMOS OP AMPS

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***Abstract*—An optimized compensation strategy for two-stage Miller-compensated CMOS operational amplifiers is presented. The output conductance of the buffer which avoids the right half-plane zero is profitably used to achieve a pole-zero compensation. Indeed, thanks to a proper choice of the buffer transconductance, the compensation for the pole due to the load capacitor is reached, thus providing better frequency performance.**

I. Introduction

Two-stage transconductance operational amplifiers (op amps) are widely used in CMOS analog integrated circuits based on switched-capacitor circuits, because they provide good values for most of their electrical parameters. Indeed, the advantages of these amplifiers are

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