Amplifier Techniques for Combining Low Noise, Precision, and High-Speed Performance

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Abstract—A monolithic operational amplifier is presented which optimizes voltage noise both in the audio frequency band, and in the low frequency instrumentation range. In addition, the design demonstrates that the requirements for low noise do not necessitate compromising the specifications in other respects. Techniques are set forth for combining low noise with high-speed and precision performance for the first time in a monolithic amplifier.

Achieved results are: 3 nV/$\sqrt{\text{Hz}}$ white noise, 80 nV_{p-p} noise from 0.1 to 10 Hz, 17 V/μs slew rate, 63 MHz gain-bandwidth product, 10 μV offset voltage, 0.2 μV/°C drift with temperature, 0.2 μV/month drift with time, and a voltage gain of two million.

I. Introduction

THE constantly improving designs of analog circuits have reduced the error contribution of most parameters to the "noise level." In many applications, noise does become the limiting factor on performance. In the case of operational amplifiers, the error due to a specific parameter can always be controlled: temperature drift effects can be reduced by regulating the environment of the system, gain error terms can be minimized by cascading several amplifying stages, etc. Voltage noise, however, cannot be eliminated, and, therefore, it can be defined as the ultimate error source.

The major emphasis of the monolithic operational amplifier design presented here was to minimize voltage noise both in the audio frequency range and in the low frequency instrumentation range. Details of this effort are described in Section II. The precision characteristics of the design are discussed in Section III. Several examples illustrate how low noise and precision can be complementary requirements.

Section IV considers the high-speed aspects of the design; the combination of low noise and bandwidth broadening is discussed. Achieved performance is summarized in Section V.

II. Low Noise Design

The noise spectrum of a typical operational amplifier is shown in Fig. 1. In the audio region, noise is flat or white noise, and is characterized by a constant value over all frequencies of interest. The low frequency instrumentation range noise is usually called the $1/f$ region because

$$(\text{voltage noise})^2 \propto 1/f. \tag{1}$$

Fig. 1 depicts voltage noise, but current noise has the same form, i.e., it is completely characterized by its white noise value and the location of its $1/f$ corner frequency. The amplifier's noise contribution in a band from frequencies f_1 to f_2, $(N_{f_2-f_1})$, can be determined [1] from

$$N_{f_2-f_1} = N_0 \left[f_0 \ln \frac{f_2}{f_1} + (f_2 - f_1) \right]^{1/2} \tag{2}$$

where

$N_{f_2-f_1}$ can be either voltage or current noise,
N_0 is the white voltage or current noise density (usually specified in nV/$\sqrt{\text{Hz}}$ or pA/$\sqrt{\text{Hz}}$), and
f_0 is the corner frequency where the $1/f$ and white noise components intersect.

In the audio range noise is minimized by a simple reduction of white noise; in the instrumentation region the problem is more complicated. In addition to low white noise, the $1/f$ corner frequency f_0 has to be as low as possible. Reducing white noise and f_0 are two separate tasks; low white noise does not necessarily imply low instrumentation range noise, as illustrated in Fig. 2.

Here the noise spectra of three operational amplifiers are shown. The popular 741 has relatively high white noise and f_0; it cannot be classified as a low noise amplifier in any region. The audio op amp [2] has low white noise, but because its $1/f$ corner is high at 70 Hz, its low frequency noise is rather high. The amplifier being described here (type OP-27/37) has minimum white noise and a low f_0 of 2.7 Hz.

A. White Noise Reduction

The essential requirement for low noise is to minimize the number of components, transistors, or resistors, contributing to input noise. The voltage noise of the simple, resistively loaded differential input stage of Fig. 3 depends on input transistors $Q1$ and $Q2$ only, provided that the noise of the load resistors R_L, and the input referred noise of the second stage are negligible.

The white voltage noise (e_{N_0}) of a differential pair [3] is given by

$$e_{N_0}^2 = 8kT\left(\frac{kT}{2qI_c} + r_{bi} + r_{be}\right) \tag{3}$$

where

I_c is the collector current of the transistors,
r_{bi} is the intrinsic base resistance underneath the emitter, and

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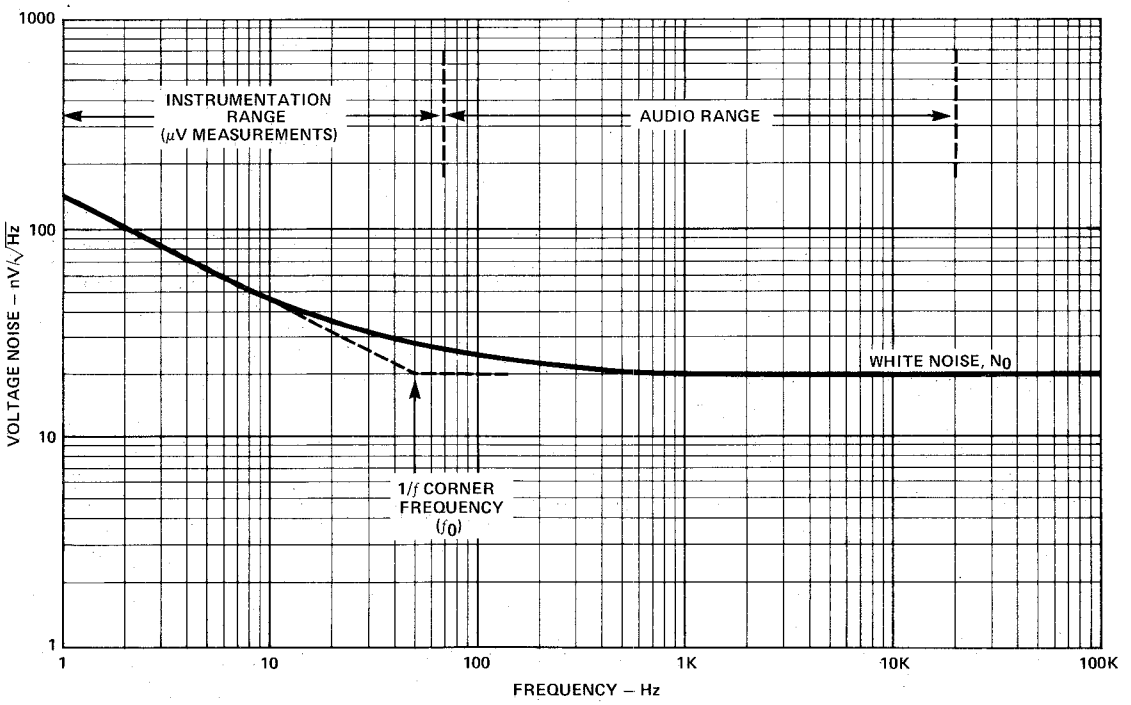

Fig. 1. Typical operational amplifier noise spectrum.

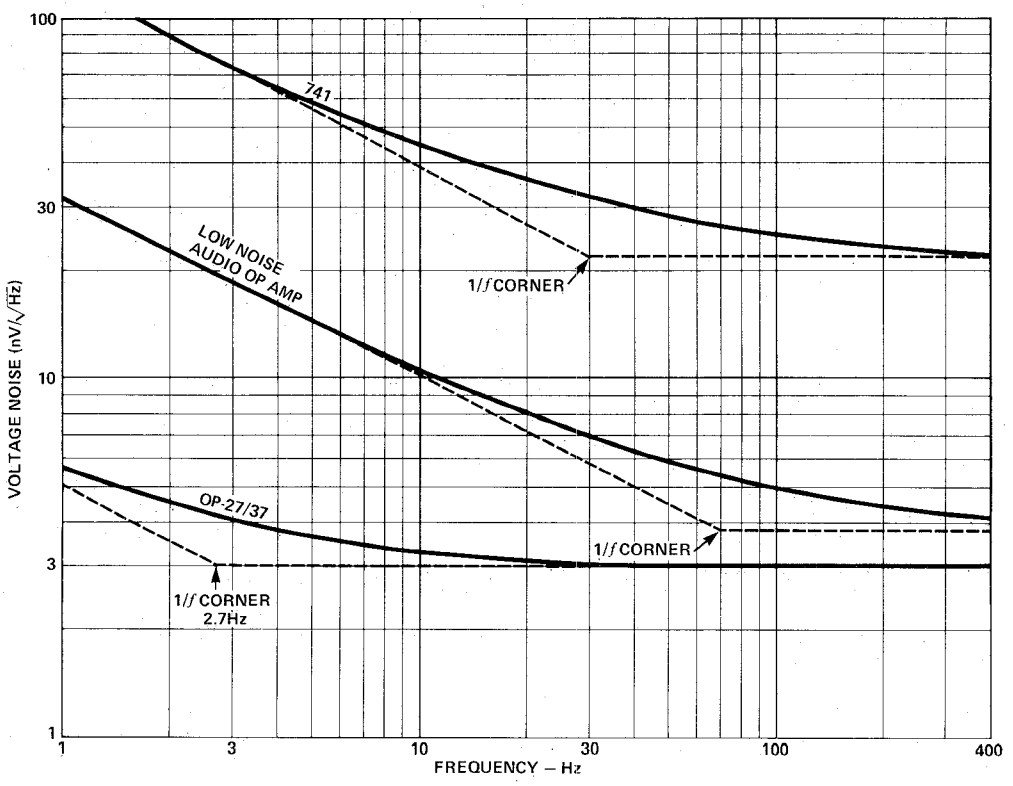

Fig. 2. Noise spectra of three operational amplifiers.

r_{be} is the extrinsic base resistance from the base contact to the edge of the emitter; it also includes base and emitter interconnection and contact resistances.

The design goal of the low noise op amp was to achieve a white noise of 3 nV/$\sqrt{\text{Hz}}$. This implies that the total resistance of the terms in parentheses of (3) is 260 Ω. The collector current dependent first term contributes 110 Ω by operating the input stage at 120 μA; r_{bi} and r_{be} are minimized by long and narrow input transistor emitters surrounded by base contacts.

Earlier, it was assumed that the second stage and load resistor noise contributions are, or at least can be made, negligible. The voltage gain A_{Vi} of the input stage is

$$A_{Vi} = g_m R_L = \frac{qI_c}{kT} R_L = \frac{120\,\mu\text{A}}{26\,\text{mV}} \times 22\,\text{k}\Omega \simeq 100. \quad (4)$$

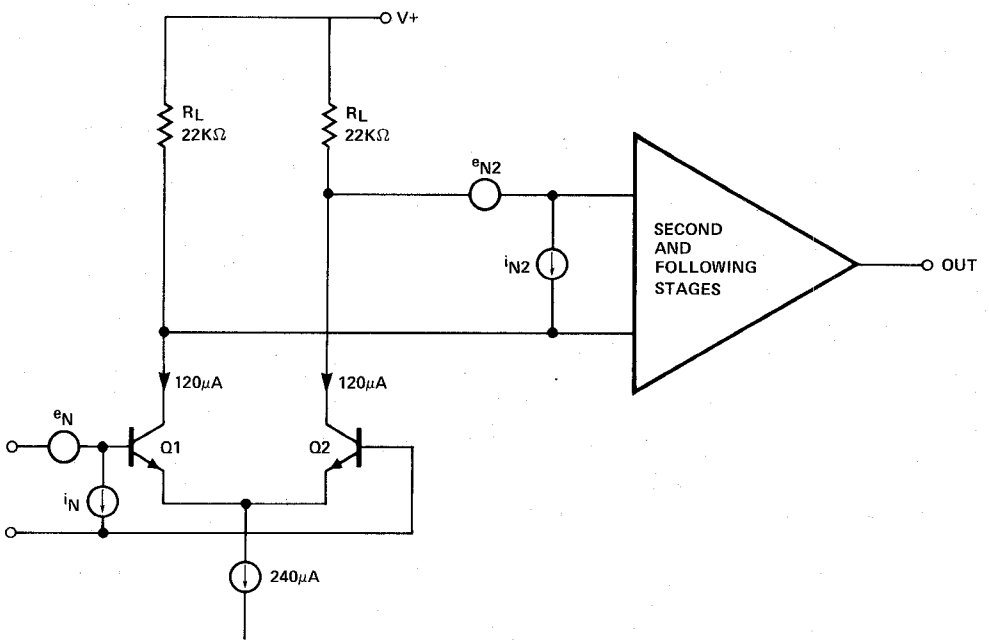

Fig. 3. Differential, resistively-loaded input stage with input and second-stage noise sources.

If the second stage voltage noise is less than 50 nV/$\sqrt{\text{Hz}}$, which is not a stringent condition, its input referred contribution will be less than 0.5 nV/$\sqrt{\text{Hz}}$, which increases input voltage noise by less than 1.4 percent when root sum squared with 3 nV/$\sqrt{\text{Hz}}$. Similarly, the load resistor noise [$=(2 \times 4kTR_L)^{1/2}$] referred to the input will be a negligible 0.27 nV/$\sqrt{\text{Hz}}$.

A general relationship can be developed between the input transistor noise (e_{N_0}) and the input referred resistor noise (N_R/A_{vi}) of the differential stage. From (3),

$$e_{N_0}^2 > \frac{4(kT)^2}{qI_c}. \tag{5}$$

Also,

$$\left(\frac{N_R}{A_{vi}}\right)^2 = \frac{2 \times 4kTR_L}{(g_m R_L)^2} = \frac{8(kT)^2}{qI_c A_{vi}}. \tag{6}$$

Therefore,

$$\frac{e_{N_0}}{N_R/A_{vi}} > \left(\frac{A_{vi}}{2}\right)^{1/2}. \tag{7}$$

From (7), if the differential gain is large, the resistor noise will be negligible. For example, if the gain is greater than 20, the resistor noise contribution will be less than 5 percent.

The current noise i_{N2} of the second stage flows through the load resistors, and thus creates an input referred voltage noise component $e_N(i_{N2})$:

$$e_N(i_{N2}) = 2i_{N2}R_L/A_{vi} = \frac{2i_{N2}}{g_m}. \tag{8}$$

The transimpedance of the input state is only 220 Ω. Therefore, as long as the white current noise of the second stage is less than 3 pA/Hz$^{1/2}$, its influence will be negligible. This again is not a stringent condition.

Fig. 4 illustrates three commonly used operational amplifier input stages. Fig. 4(a) is the 741 input stage [4] and Fig. 4(b) is used as an input on many precision amplifiers [5]. Both of these have active loads ($Qa5$, $Qa6$, $Qb3$, $Qb4$). Active loads, by their very nature, amplify their own internal noise. This current noise then flows through the input transistors, thereby degrading noise performance. A detailed noise analysis of active load stages can be found in [6].

Fig. 4(c) shows a resistively loaded input stage which is employed on the most popular three-gain-stage op amps [7], [8]. With its collector current at 8 μA, the voltage noise at 9 nV/(Hz)$^{1/2}$ is basically limited by the transistor noise of $Qc1$ and $Qc2$ and can be calculated from (3). When the collector current is increased to 120 μA, and the input device geometries are redesigned to minimize r_{bi} and r_{be}, the observed noise of Fig. 4(c) will be higher than predicted by (3). Secondary noise contributors which are negligible at the 9 nV/(Hz)$^{1/2}$ level suddenly become significant noise sources. For example, the input bias current cancellation scheme ($Qc3$-$Qc10$) adds about 2 nV/(Hz)$^{1/2}$ to the total voltage noise. Resistors $R1$ and $R2$ limit the current through the input protection diodes when large differential voltages are applied. However, the 1 kΩ total source resistance contributes 4.1 nV/(Hz)$^{1/2}$ of noise.

On the present design, the limiting resistors are eliminated, and the bias current cancellation network is removed from the signal path—to be discussed later—resulting in the simple input stage of Fig. 3.

B. Current Noise

Voltage noise is inversely proportional to the square root of collector current as shown by (3). Current noise, however, is directly proportional to the same function. Therefore, an inevitable byproduct of reduced voltage noise is increased current noise. The amplifier's current noise is shown in Fig. 5; it has the form described by (2), and the critical parameters

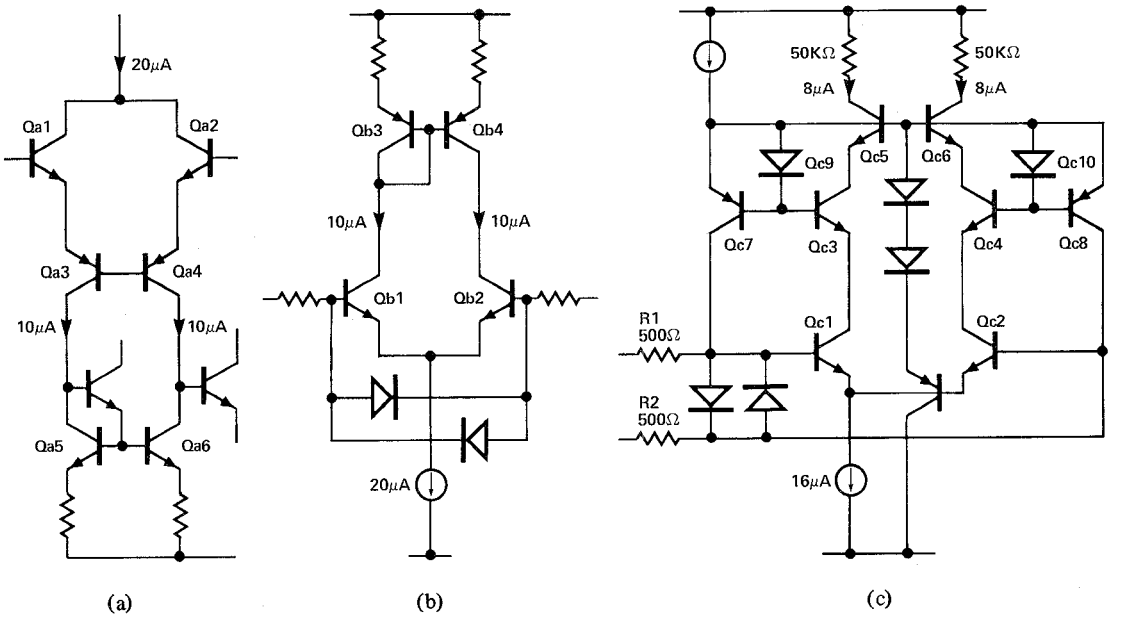

Fig. 4. Three op amp input stages. (a) 741—active load. (b) n-p-n input—active load. (c) Resistive load with bias current cancellation.

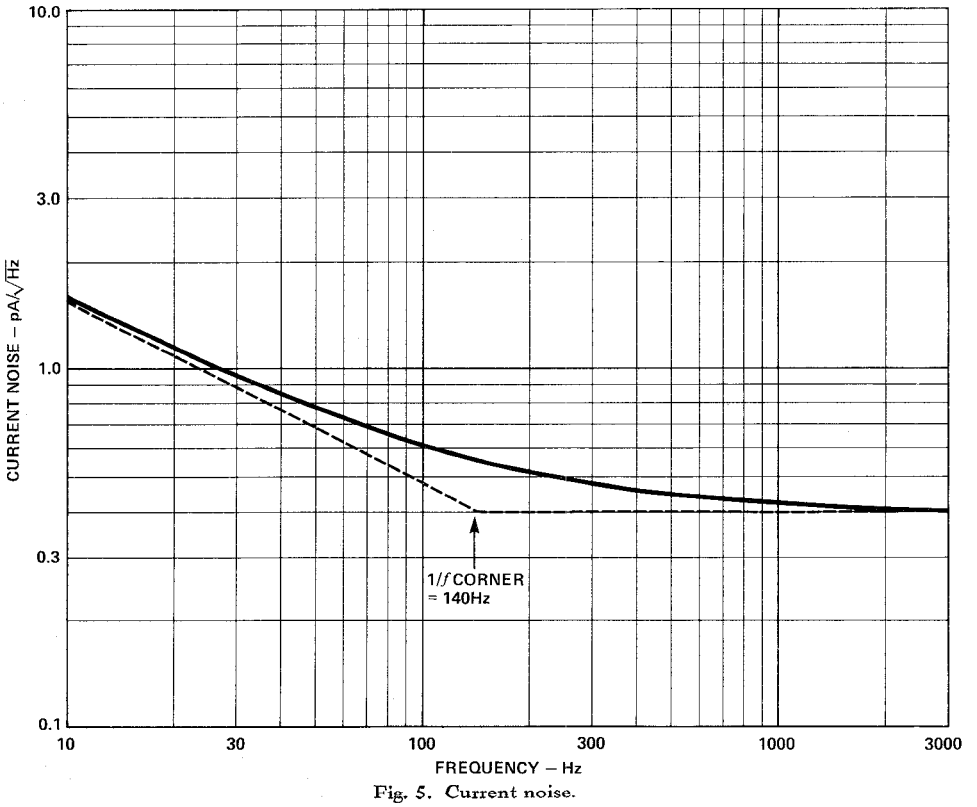

Fig. 5. Current noise.

again are the magnitude of the white noise and the location of the $1/f$ corner frequency.

The total observed noise of an op amp is

$$(\text{total noise})^2 = (\text{voltage noise})^2 + (\text{source resistor noise})^2 + (\text{current noise} \times \text{source resistor})^2. \quad (9)$$

The obvious contribution of current noise is the last term of (9). In addition, voltage noise will have current noise dependent components, e.g., the current noise flowing through r_{bi} and r_{be} of the input transistors. Furthermore, internal current noise sources create voltage noise, as shown earlier in (8).

White current noise is seldom a problem when total noise is considered. Although white noise is relatively high, it still does not limit performance. Fig. 6 plots total noise as a function of source resistance. 1000 Hz noise is dominated by resistor noise when source resistance is in excess of 1 kΩ.

The key parameter in considering current noise is the location of the $1/f$ corner frequency. A survey of op amp data sheets indicates corner frequencies of 200 Hz–2 kHz, typi-

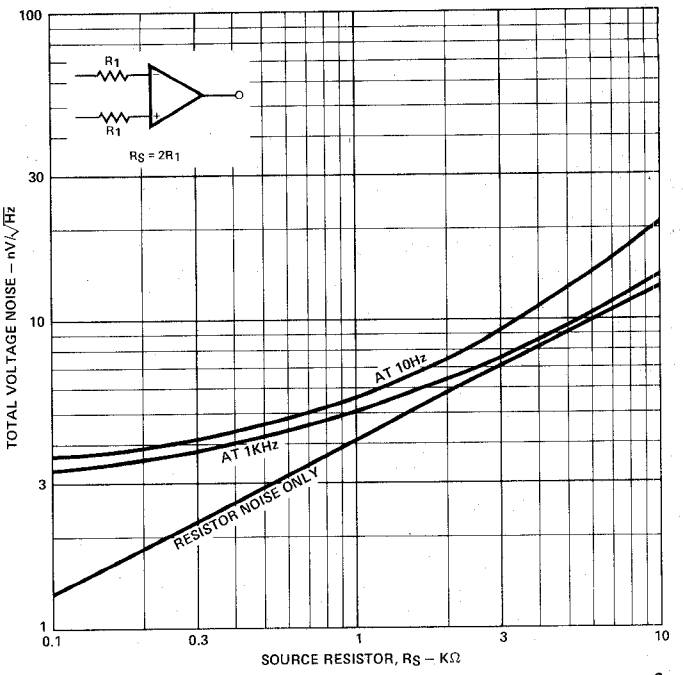

Fig. 6. Total voltage noise versus source resistance; total noise = $[e_N^2 + (i_N R_S)^2 + 4kTR_s]^{1/2}$.

cally an order of magnitude higher than the f_0 of voltage noise. The current noise f_0 is strictly process dependent, it can be as high as 10 MHz for some digital processes [6]. For this device, the $1/f$ corner is low at 140 Hz (Fig. 5), partially due to the silicon nitride passivation used, which acts as an additional gettering step.

When low frequency (10 Hz) total noise is plotted in Fig. 6, the resistor noise is unchanged, but current noise is enlarged four fold. Voltage noise is only slightly increased (Fig. 2). With source resistors in excess of 5 kΩ, current noise starts to dominate. The total noise at this point, however, is four times higher than voltage noise. The optimized voltage noise of the device is completely wasted, not because of current noise, but because source resistor noise exceeds voltage noise even at 1 kΩ.

C. Minimizing Low Frequency Noise

The $1/f$ region of voltage noise is basically a current noise-caused phenomenon. It occurs because current noise at some internal node in the circuit flows through a relatively large resistor, creating voltage noise. As shown earlier, in the white current noise region, the problem is insignificant. However, because of the relatively high $1/f$ corner of current noise, at low frequencies the current noise-caused voltage noise can easily increase by an order of magnitude.

A reduction of instrumentation range voltage noise therefore requires a low $1/f$-corner current noise process (which has been achieved here), and a systematic evaluation of the internal nodes of the circuit. Buffering with emitter followers should be used when either the current noise or the impedance is high at a given node.

An example of this is shown in the simplified schematic of the operational amplifier (Fig. 7). With an n-p-n input stage a lateral p-n-p second stage is always necessary for level shifting. In many designs the bases of the lateral p-n-p transistors ($Q23$, $Q24$) are tied directly to the input stage. However, the low frequency current noise of these p-n-p's is very high for several reasons. They operate at high emitter currents (240 μA) where their current gains have already fallen off to a low value. In addition, the lateral p-n-p being a surface device, its $1/f$ corner frequency is significantly higher than that of the n-p-n transistors. In this particular example, the white current noise of $Q23$, $Q24$ is 2.5 pA/Hz$^{1/2}$, its $1/f$ corner occurs at 500 Hz. Converting this second stage current noise to input referred voltage noise using (8), gives 3 nV/$\sqrt{\text{Hz}}$ at about 70 Hz. In other words, loading the input stage directly with lateral p-n-p's $Q23$, $Q24$ would move the $1/f$ voltage noise corner of the amplifier from 2.7 to 70 Hz.

The insertion of emitter followers $Q21$ and $Q22$ completely eliminates this problem. The current noise of $Q21$ and $Q22$ is actually $\sqrt{2}$ times less than the input current noise because of the lower operating current. The current noise of $Q23$ and $Q24$ flows through two 1 kΩ resistors (the output impedance of the emitter followers and the base resistance of the lateral p-n-p's) rather than the 22 kΩ load resistors. The input referred voltage noise contribution of the $Q23$, $Q24$ current noise at 2.7 Hz is only 0.7 nV/Hz$^{1/2}$, while the $Q21$, $Q22$ current noise translates to 0.9 nV/Hz$^{1/2}$.

The $1/f$ corner is at 2.7 Hz because at that frequency the root sum squared of all the frequency dependent noise sources equals the white noise of 3 nV/Hz$^{1/2}$. The dominant terms are the input current noise (which is 3.1 pA/Hz$^{1/2}$ at 2.7 Hz) flowing through the equivalent input resistance of 520 Ω, as given by (3), and the input referred voltage noise of the second stage. The second stage noise is about 160 nV/Hz$^{1/2}$ at 2.7 Hz, or twice the noise of a 741 amplifier (80 nV/Hz$^{1/2}$ at 2.7 Hz as shown in Fig. 2).

The 0.1–10 Hz peak to peak noise of the op amp is 80 nV,

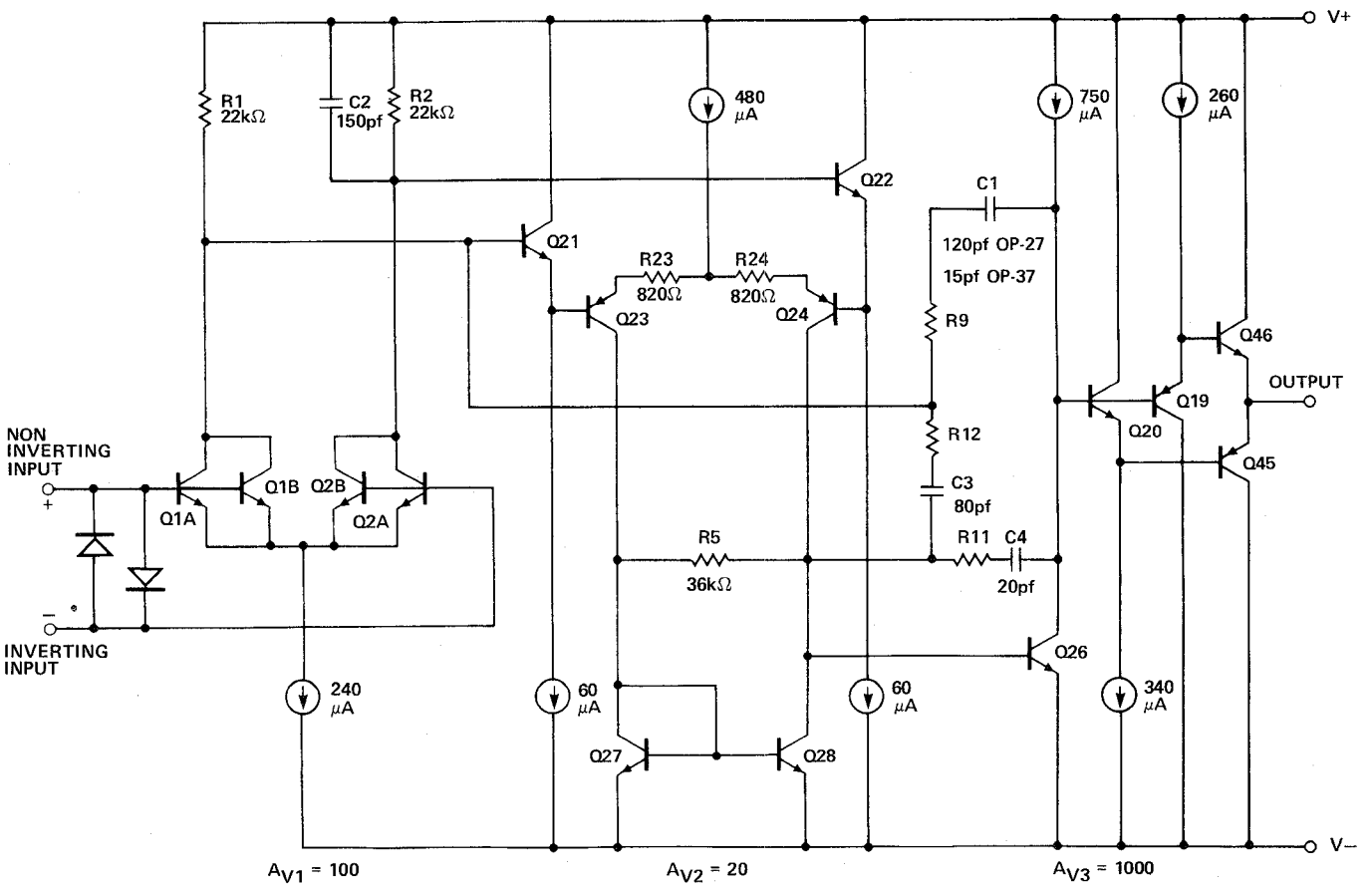

Fig. 7. Low noise op amp simplified schematic.

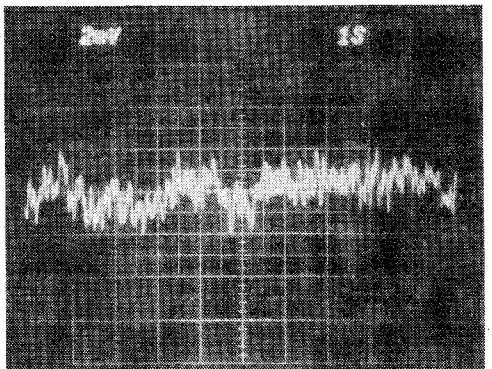

Fig. 8. Low frequency noise: 0.1–10 Hz peak to peak. 40 nV/div referred to input (closed-loop gain = 50 000).

as illustrated by the oscilloscope photograph of Fig. 8. The rms noise in this frequency band is 14.2 nV as calculated from (2).

III. Precision Design

The circuit employs all the well-established design techniques for achieving precision performance. The simple resistively loaded input stage has been demonstrated in the past to be the best for low offset voltage and drift with time and temperature [9]. In addition, the load resistors are ideal for on wafer Zener-zap adjustment of offset voltage to a few microvolts [8], which is also used on this circuit. And, as demonstrated in the previous section, resistive loading optimizes noise.

The quad-connection of input transistors [9] is another design tool which enhances both precision and low noise performance. The transistors making up the differential input pair are formed from cross connected segments of a quad of transistors ($Q1A$, $Q1B$, $Q2A$, $Q2B$ of Fig. 7). This has the well-known benefits of cancelling thermal gradients and variations in the epi and diffusions. As far as noise is concerned, the quad connection also helps because it effectively halves r_{bi} and r_{be} by the use of transistors in parallel.

Because the input stage operates at a collector current which is an order of magnitude higher than the typical 10 μA of most op amps, input bias current (I_B) can be a significant error contributor. Super β input transistors cannot be used to reduce I_B, because the intrinsic resistance of super β transistors underneath the emitter [r_{bi} of (1)] is inherently high. Therefore, the noise performance of a super β transistor is considerably worse than that of the equivalent n-p-n transistor (i.e., same device geometry and operating at the same current).

The bias current cancellation circuit of Fig. 9 provides the best compromise. As implied in Section II, it is removed from the signal path and therefore does not contribute to voltage noise or to input offset voltage. $Q11$ and $Q12$ are identical to the input transistors, and operate at the same current density and approximately the same collector-base voltage as $Q1$ and $Q2$. Therefore, the base current of $Q11$, $Q12$ precisely matches

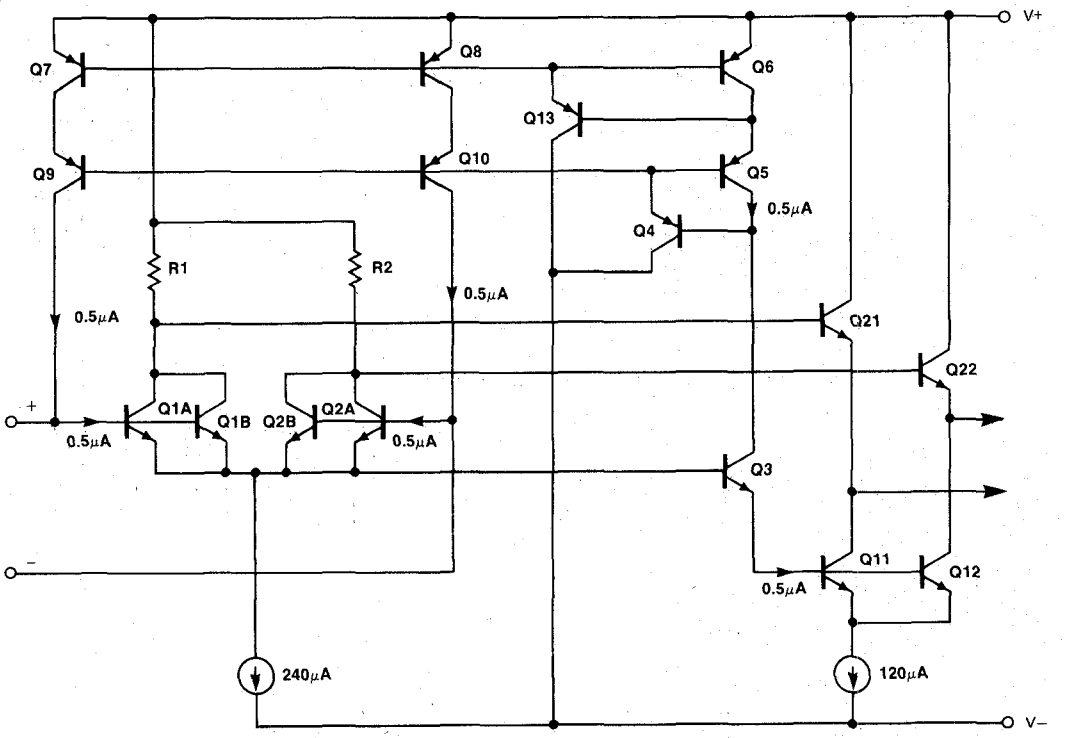

Fig. 9. Input bias current cancellation circuit.

the uncompensated input current of $Q1$ and $Q2$. The output of the precision current mirror of $Q5$-$Q10$ is fed back to the bases of the input transistors, cancelling the base currents. This scheme is successful in removing 98 percent of the input bias current and has a 3 GΩ common-mode input resistance.

Bias current compensation schemes, as a rule, increase input current noise by a factor of $\sqrt{2}$ because the cancelling current noise is uncorrelated to the input transistor current noise. This is the case of the bias current cancellation network used on the OP-07 amplifier [8] [Fig. 4(c)], where the noise currents of $Qc1$ and $Qc3$ are uncorrelated. In the circuit of Fig. 9, however, the noise currents of both $Q9$ and $Q10$ originate from the same source: the base current of $Q11$ and $Q12$, and thus correlate [10]. With balanced source resistors the cancellation noise currents represent a common-mode component and, therefore, do not add to the input current noise.

A necessary condition of precision performance is high voltage gain, preferably in excess of a million. This gain should be maintained even under heavy load conditions. Both thermal and electrical effects can prevent the realization of such high gain under load. The double-buffered output stage, shown on the simplified schematic of Fig. 7, isolates the load by a β^2 factor from the high impedance (approximately 80 kΩ) gain node at the collector of $Q26$. For positive swings the current gains of $Q46$ and $Q19$ are multiplied, for negative swings the β product of $Q45$ and $Q20$ applies. This β^2 multiplier is at least 5000, even when 10 mA is delivered to a 1 kΩ load, i.e., the reflected impedance at the collector of $Q26$ is more than 5 MΩ, or the electrical gain degradation is less than 2 percent.

Thermal feedback—the effect of output power dissipation

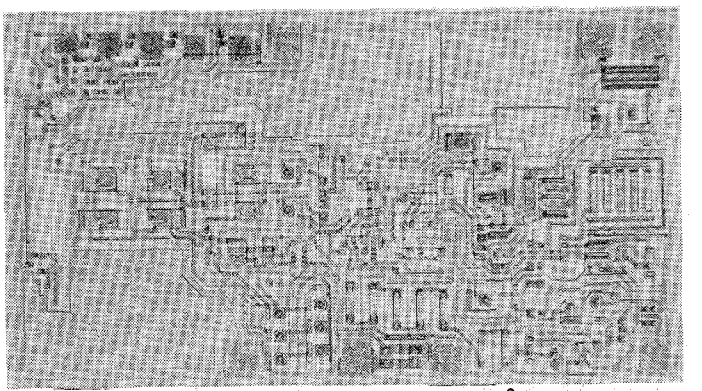

Fig. 10. Photomicrograph of the 96 × 54 mil^2 chip.

changes on the input transistors—is less than 1 μV. This is accomplished by a thermally symmetrical layout [9], which, by now, is a common technique of all precision amplifier designs, and can be observed on the chip photograph of Fig. 10. Fig. 11 shows the voltage gain with 1 kΩ load as measured on a Tektronix 178 tester. The straightness of this line illustrates the absence of thermal feedback, even as 10 mA is delivered to the load.

IV. High-Speed Design

The relatively high operating current of the input stage (120 μA), which is necessary for low voltage noise, also provides an opportunity for increasing bandwidth. The typical three stage op amp's first stage gain is limited to 20 because of its 10 μA collector currents, and maximum practical load resistors of 50 kΩ. Here the input differential gain is 100. This "excess" gain allows the design of a wider band, less

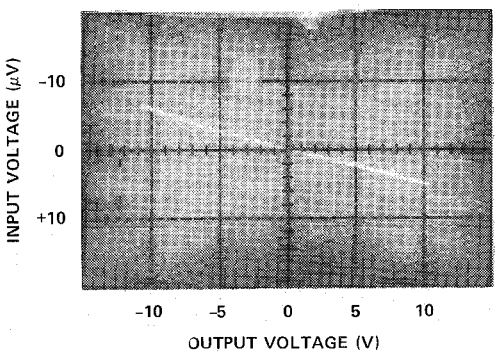

Fig. 11. Voltage gain, R_L = 1 kΩ (measured on Tektronix 178 linear tester).

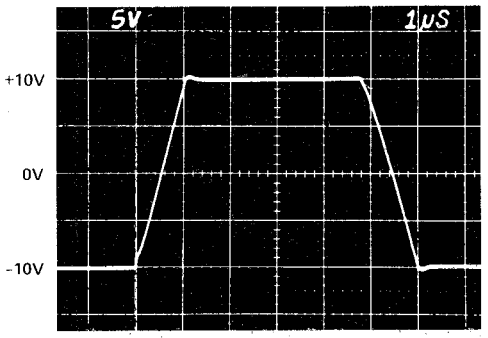

Fig. 12. Large signal transient response.

accurate second stage without adversely influencing input accuracy. The usually slow lateral p-n-p level-shift amplifier is broadbanded with degenerating resistors $R23$ and $R24$ (Fig. 7) [11] and a low, controlled gain of 20. The frequency characteristics of the second stage are mainly determined by $R5$, $R23$, and $R24$, and to a reduced extent, by the lateral p-n-p's, $Q23$ and $Q24$. As a result, feed-forward capacitor $C3$ can bypass the second stage at a significantly higher frequency than in previous three stage precision op amp designs.

Capacitor $C1$ sets the dominant pole. $C2$ makes the high frequency signal single-ended, i.e., it rolls off the gain of the input stage on the side which is not fed forward. The use of resistors $R9$, $R11$, and $R12$ allows shaping of the frequency response with appropriately placed zeros to cancel poles occurring in the 5–20 MHz range.

On the unity gain compensated version of the design (type OP-27) $C1$ is 120 pF, the bandwidth is 8 MHz with 70° phase margin. $C1$ is reduced to 15 pF on the decompensated model (type OP-37) which is stable in closed loop gains of five or more. On this device slew rate is 17 V/μs (Fig. 12), voltage gain at 10 kHz is still 6300.

Wider bandwidth has beneficial effects as far as precision performance is considered, specifically, gain error at low frequencies. A typical precision op amp may have a dc gain of two million, with a bandwidth of 600 kHz. Since the gain rolls off with frequency at a 20 dB/decade rate, the full voltage gain of the amplifier can only be realized at frequencies below the dominant pole of 0.3 Hz. Many low frequency instrumentation applications, of course, have to process signals which change at a faster rate. The OP-27's dominant pole occurs at 7 Hz, the OP-37's at 30 Hz.

TABLE I
TYPICAL AND GUARANTEED SPECIFICATIONS OF THE LOW NOISE, PRECISION, HIGH-SPEED OP AMP AT $V_s = \pm 15$ V, $T_A = 25°C$

	Typ	Min/Max	Units
Noise Specifications			
Voltage noise: 0.1–10 Hz	80	180	nV_{p-p}
f_0 = 10 Hz	3.5	5.5	$nV/\sqrt{Hz}$
f_0 = 1 kHz	3.0	3.8	$nV/\sqrt{Hz}$
Current noise: f_0 = 10 Hz	1.6	4.0	$pA/\sqrt{Hz}$
f_0 = 1 kHz	0.4	0.6	$pA/\sqrt{Hz}$
Precision Specifications			
Offset voltage	10	25	μV
drift with temperature	0.2	0.6	μV/°C
drift with time	0.2	1.0	μV/mo
Input bias current	10	40	nA
Input offset current	7	35	nA
Voltage gain	2000	1000	V/mV
CMRR	126	114	dB
Speed Specifications			
Slew rate, $A_{VCL} \geq 1$ (OP-27)	2.8	1.7	V/μs
Slew rate, $A_{VCL} \geq 5$ (OP-37)	17	11	V/μs
Gain at 10 kHz (OP-37)	6.3	4.5	V/mV
Unity gain bandwidth (OP-27)	8.0	5.0	MHz
Other Specifications			
Power consumption	90	140	mW
Output voltage swing, $R_L \geq 600\ \Omega$	11.5	10	V
Capacitive load capability	2000	–	pF

V. PERFORMANCE

The achieved specifications of the circuit are listed in Table I. The significance of most parameters has already been discussed. The device has been in high volume production since December 1980; thus, the validity of the specifications has been demonstrated by more than just a few developmental units.

VI. CONCLUSIONS

The amplifier described advances the state of the art by a significant reduction of noise simultaneously with enhanced precision and high-speed performance.

ACKNOWLEDGMENT

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A Low-Voltage BiMOS Op Amp

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Abstract—**This paper describes the development of a threshold-implanted BiMOS amplifier IC optimized for 2-5 V operation at a supply current of 300 μA. A nonlinear operational transconductance amplifier (OTA) buffer having on-chip feedback provides a low-impedance rail-to-rail output, and a bulk-modulated PMOS input pair extends the common-mode range. Protective-network bootstrapping makes possible subpicoampere input-bias currents below 85°C, and improved offset stability is achieved by the choice of threshold-level stage currents. Amplifier design is straightforward and readily applied from "micropower" to "broad-band" operating ranges. The combination of these features has produced a unique high-performance integrated circuit.**

I. Introduction

THE monolithic operational amplifier continues to evolve in new and improved forms. Part of this change appears to be the result of the influence of more sophisticated systems in which approaches such as "autozeroing" permit performance improvements. Another factor is the trend toward lower-voltage single-supply operation for microprocessor, automotive, portable, and remote applications. In addition, the appearance of linear CMOS products provides a broader perspective and challenge for op amp design in a high-density inexpensive process.

For small to moderately sized silicon chips—perhaps up to 10 000–15 000 mils^2—process cost may permit the designer a choice of bipolar, CMOS or "mixed-technology" (BiMOS, BiFET) approaches. Performance requirements have usually dictated that choice: bipolar for its accuracy potential [1], [2] and mixed-technology amplifiers for their combination of speed, bandwidth, and input impedance [3], [4], with analog CMOS fast assuming an important posture [5], [6].

More specifically, recent developments in op amp design have stressed extended-range operation and improved input and output swings at lower supply voltages. At ISSCC '78, it was shown that low-voltage bipolar amplifiers can deliver substantial drive currents [7]. In order to accomplish this goal at a supply of 1.1 V, however, the amplifier design and its compensation can become quite complex. CMOS op amps described at Electro '79 show excellent input-voltage range and low-voltage micropower capability [8], but sacrifice gain under load and low output resistance in order to achieve rail-to-rail output swing. Similar shortcomings exist when CMOS inverters are used as an output stage [4], the inverters requiring a large class A current in order to drive even modest load capacitance without excessive phase shift.

A new design approach described in this paper circumvents most of these limitations. A BiMOS process makes possible a large common-mode input range, exceptionally low input-bias currents, and a rail-to-rail low-impedance output, while remaining economically competitive. Operation at supply potentials down to 2 V is readily achieved with simple circuitry, and tightened threshold control would appear to make the same approach practical for high-performance 1 V operation.

II. A Design Approach

This section treats amplifier design in general terms; a more detailed description of new aspects follows in a subsequent section. Fig. 1 shows the amplifier in block form. A gain stage having a PMOS input drives a second buffer amplifier having substantial feedback. Bias is generated by a bandgap-type loop, which permits relatively good control of buffer idling currents. A pair of unity-gain amplifiers bootstrap the input protective networks (shown here simply as diodes) to

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