The JFET

Device Equations

The circuit symbols for the junction FET or JFET are shown in Fig. 1. There are two types of devices, the n-channel and the p-channel. Each device has gate (G), drain (D), and source (S) terminals. The drain and source connect through a semiconductor channel. A diode junction separates the gate from the channel. For proper operation as an amplifying device, this junction must be reverse biased. This requires $v_{GS} < 0$ for the n-channel device and $v_{GS} > 0$ for the p-channel device.

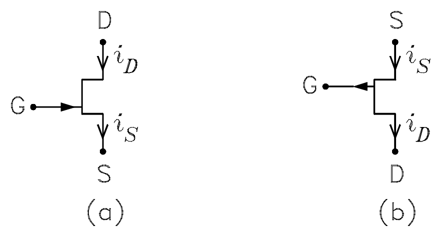

Figure 1: JFET circuit symbols. (a) N channel. (b) P channel.

The discussion here applies to the n-channel JFET. The equations apply to the p-channel device if the subscripts for the voltage between any two of the device terminals are reversed, e.g. v_{GS} becomes v_{SG}. The JFET must be biased with the gate-source junction reverse biased to prevent the flow of gate current, i.e. $v_{GS} < 0$ for the n-channel device and $v_{GS} > 0$ for the p-channel device. The gate current is then equal to the reverse saturation current of the junction. This current is very small and is usually neglected in bias and small-signal calculations. However, its effect is included in the noise model given here. The JFET is biased in the active mode or the saturation region when $v_{DS} \geq v_{GS} - V_{TO}$, where V_{TO} is the threshold or pinch-off voltage, which is negative.

In the saturation region, the drain current is given by

$$\begin{aligned} i_D &= \beta\left(v_{GS} - V_{TO}\right)^2 \qquad \text{for } v_{GS} \geq V_P \\ &= 0 \qquad \text{for } v_{GS} < V_{TO} \end{aligned} \tag{1}$$

where β is the transconductance coefficient given by

$$\beta = \beta_0\left(1 + \lambda v_{DS}\right) \tag{2}$$

In this equation, β_0 is the zero-bias value of β, i.e. the value with $v_{DS} = 0$, and λ is the channel-length modulation parameter which accounts for the change in β with drain-source voltage. Because $i_G \simeq 0$ in the pinch-off region, the source current is equal to the drain current, i.e. $i_S = i_D$.

A second way of writing the JFET current is

$$\begin{aligned} i_D &= I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 \qquad \text{for } v_{GS} \geq V_P \\ &= 0 \qquad \text{for } v_{GS} < V_P \end{aligned} \tag{3}$$

where I_{DSS} is the drain-source saturation current, i.e. the value of i_D with $v_{GS} = 0$. It is given by

$$I_{DSS} = \beta V_{TO}^2 = \beta_0 (1 + \lambda v_{DS}) V_{TO}^2 \tag{4}$$

Typical device parameters are $\beta_0 = 2 \times 10^{-4}$ A/V^2, $V_{TO} = -4$ V, and $\lambda = 0.01$ V^{-1}.

Figure 2 shows the typical variation of the drain current i_D with gate-to-source voltage v_{GS} for $V_{TO} \le v_{GS} \le 0$. The slope of the curve is the small-signal transconductance g_m. For $v_{GS} < V_{TO}$, the drain current is zero. For $v_{GS} > 0$, gate current flows. Fig. 2 shows the typical variation of drain current i_D with drain-to-source voltage v_{DS} for eight values of V_{GS} in the range $V_{TO} < V_{GS} \le 0$. The dashed line separates the linear or triode region from the active or saturation region. In the saturation region, the slope of the curves is the reciprocal of the small-signal drain-source resistance r_0.

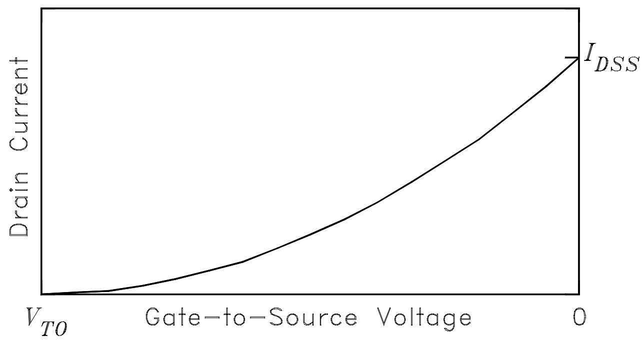

Figure 2: Plot of I_D versus V_{GS} for constant V_{DS}.

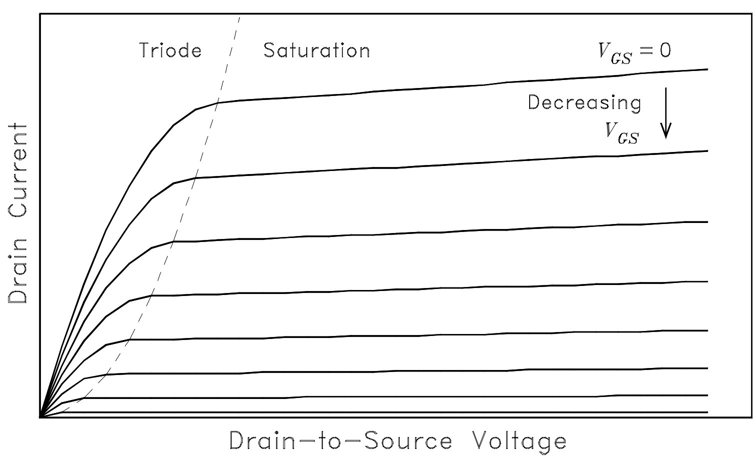

Figure 3: Plot of I_D versus V_{DS} for eight values of V_{GS}.

Bias Equation

Figure 4 shows the JFET with the external circuits represented by Thévenin dc circuits. If the JFET is in the pinch-off region, the following equations for I_D hold:

$$I_D = \beta (V_{GS} - V_{TO})^2 \tag{5}$$

$$V_{GS} = V_{GG} - (V_{SS} + I_D R_{SS}) \tag{6}$$

$$\beta = \beta_0 (1 + \lambda V_{DS}) \tag{7}$$

$$V_{DS} = (V_{DD} - I_D R_{DD}) - (V_{SS} + I_D R_{SS}) \tag{8}$$

Because this is a set of nonlinear equations, a closed form solution for I_D cannot be easily written unless it is assumed that β is not a function of V_{DS}. This assumption requires the condition $\lambda V_{DS} \ll 1$. In this case, the equations can be solved for I_D to obtain

$$I_D = \frac{1}{4\beta R_{SS}^2} \left[\sqrt{1 + 4\beta R_{SS} (V_{GG} - V_{SS} - V_{TO})} - 1 \right]^2 \tag{9}$$

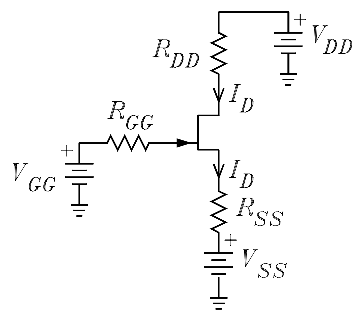

Figure 4: JFET dc bias circuit.

Unless $\lambda V_{DS} \ll 1$, Eq. (9) is only an approximate solution. A numerical procedure for obtaining a more accurate solution is to first calculate I_D with $\beta = \beta_0$. Then calculate V_{DS} and the new value of β from which a new value for I_D can be calculated. The procedure can be repeated until the solution for I_D converges. Alternately, computer tools can be used to obtain a numerical solution to the set of nonlinear equations.

Small-Signal Models

There are two small-signal circuit models which are commonly used to analyze JFET circuits. These are the hybrid-π model and the T model. The two models are equivalent and give identical results. They are described below.

Hybrid-π Model

Let the drain current and each voltage be written as the sum of a dc component and a small-signal ac component as follows:

$$i_D = I_D + i_d \tag{10}$$

$$v_{GS} = V_{GS} + v_{gs} \tag{11}$$

$$v_{DS} = V_{DS} + v_{ds} \tag{12}$$

If the ac components are sufficiently small, we can write

$$i_d = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} \tag{13}$$

where the derivatives are evaluated at the dc bias values. Let us define

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2\beta \left(V_{GS} - V_{TO}\right) = 2\sqrt{\beta I_D} \tag{14}$$

$$r_0 = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1} = \left[\beta_0 \lambda \left(V_{GS} - V_{TO}\right)^2\right]^{-1} = \frac{V_{DS} + 1/\lambda}{I_D} \tag{15}$$

The drain current can thus be written

$$i_d = i_d' + \frac{v_{ds}}{r_0} \tag{16}$$

where

$$i_d' = i_s' = g_m v_{gs} \tag{17}$$

The gate current is given by $i_g = i_s' - i_d' = 0$. The small-signal circuit which models these equations is given in Fig. 5(a). This is called the hybrid-π model. The resistor r_d is the parasitic resistance in series with the drain contact. It has a typical value of 50 to 100 Ω. Often it is neglected in calculations. This is done in the following. It is simple to account for r_d in any equation by adding it to the external drain load resistance.

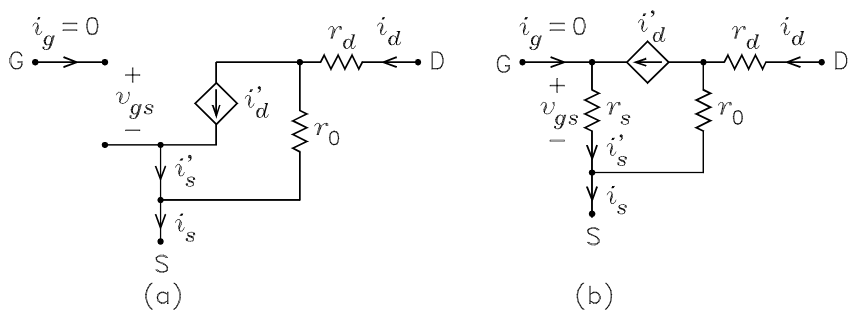

Figure 5: (a) JFET hybrid-π model. (b) T model.

T Model

The T model of the JFET is shown in Fig. 5(b). The resistor r_0 is given by Eq. (15). The resistor r_s is given by

$$r_s = \frac{1}{g_m} \tag{18}$$

where g_m is the transconductance defined in Eq. (14). The currents are given by

$$i_d = i_d' + \frac{v_{ds}}{r_0} \tag{19}$$

$$i_d' = i_s' = \frac{v_{gs}}{r_s} = g_m v_{gs} \tag{20}$$

$$i_g = i_s' - i_d' = 0 \tag{21}$$

The currents are the same as for the hybrid-π model. Therefore, the two models are equivalent.

Small-Signal Equivalent Circuits

Several equivalent circuits are derived below which facilitate writing small-signal low-frequency equations for the JFET. We assume that the circuits external to the device can be represented by Thévenin equivalent circuits. The Norton eqivalent circuit seen looking into the drain and the Thévenin equivalent circuit seen looking into the source are derived. Several examples are given which illustrate use of the equivalent circuits.

Simplified T Model

Figure 6(a) shows the JFET T model with a Thévenin source in series with the gate. We wish to solve for the equivalent circuit in which the source i'_d connects from the drain node to ground rather than from the drain node to the gate node. We call this the simplified T model. Aside for the subscripts, the T model in Fig. 5(b) is identical to the T model for the BJT with $r_x = 0$. Therefore, the simplified T model for the JFET must be of the same form as the simplified T model for the BJT. Because $i_g = 0$, the effective current gains of the JFET are $\alpha = 1$ and $\beta = \infty$. The simplified T model is shown in Fig. 6(b), where i'_d and r_s are given by

$$i'_d = i'_s \tag{22}$$

$$r_s = \frac{1}{g_m} \tag{23}$$

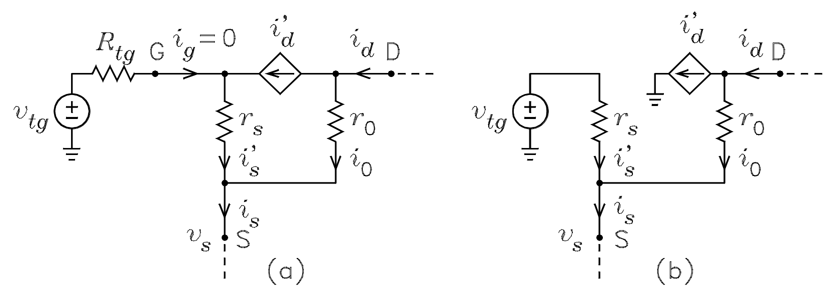

Figure 6: (a) JFET T model with Thévenin source connected to the gate. (b) Simplified T model.

Norton Drain Circuit

The Norton equivalent circuit seen looking into the drain can be used to solve for the response of the common-source and common-gate stages. Fig. 7(a) shows the JFET with Thévenin sources connected to its gate and source. The Norton drain circuit follows directly from the BJT Norton collector circuit with appropriate changes in subscripts and the substitutions $\alpha = 1$, and $\beta = \infty$, and $r_x = 0$. The circuit is given in Fig. 7(b), where $i_{d(sc)}$ and r_{id} are given by

$$i_{d(sc)} = G_{mg} v_{tg} - G_{ms} v_{ts} \tag{24}$$

$$r_{id} = \frac{r_0 + r_s \| R_{ts}}{1 - R_{ts} / (r_s + R_{ts})} = r_0 \left(1 + \frac{R_{ts}}{r_s}\right) + R_{ts} \tag{25}$$

The two transconductances G_{mg} and G_{ms} are given by

$$G_{mg} = \frac{1}{r_s + R_{ts} \| r_0} \frac{r_0}{r_0 + R_{ts}} \tag{26}$$

$$G_{ms} = \frac{1}{R_{ts} + r_s \| r_0} \tag{27}$$

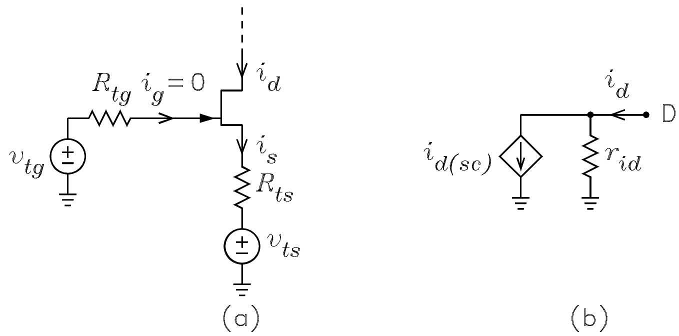

Figure 7: (a) JFET with Thévenin sources connected to the gate and the source. (b) Norton drain circuit.

For the case $r_0 \gg R_{ts}$ and $r_0 \gg r_s$, we can write

$$i_{d(sc)} = G_m (v_{tg} - v_{ts}) \tag{28}$$

where

$$G_m = \frac{1}{r_s + R_{ts}} \tag{29}$$

The value of $i_{d(sc)}$ calculated with this approximation is simply the value of i'_s calculated with r_0 considered to be an open circuit. The term "r_0 approximations" is used in the following when r_0 is neglected in calculating $i_{d(sc)}$ but not neglected in calculating r_{id}.

Thévenin Source Circuit

The Thévenin equivalent circuit seen looking into the source is useful in calculating the response of common-drain stages. Fig. 8(a) shows the JFET symbol with a Thévenin source connected to the gate. The resistor R_{td} represents the external load resistance in series with the drain. The Thévenin source seen looking into the source follows directly from the Thévenin emitter circuit for the BJT with appropriate subscript changes and the substitutions $\alpha = 1$, $\beta = \infty$, and $r_x = 0$. The circuit is shown in Fig. 8(b), where $v_{s(oc)}$ and r_{is} are given by

$$v_{s(oc)} = v_{tg} \frac{r_0}{r_s + r_0} \tag{30}$$

$$r_{is} = \frac{r_s (r_0 + R_{td})}{r_s + r_0} \tag{31}$$

When $R_{td} = 0$, note that $r_{is} = r_s \| r_0$.

Summary of Models

Figure 9 summarizes the four equivalent circuits derived above.

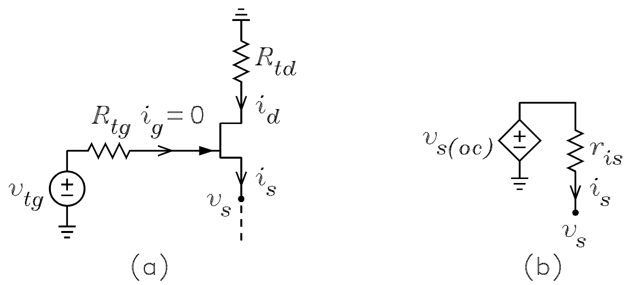

Figure 8: (a) JFET with Thévenin source connected to the gate. (b) Thévenin equivalent circuit seen looking into the source.

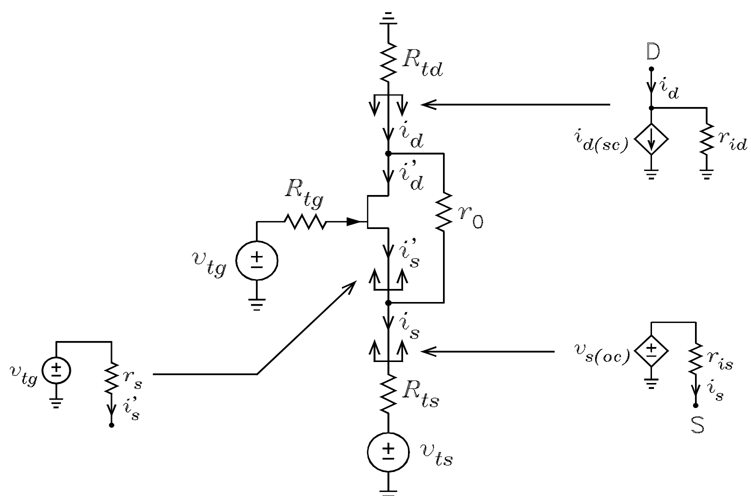

Figure 9: Summary of the small-signal equivalent circuits.

Example Amplifier Circuits

The Common-Source Amplifier

Figure 10(a) shows the ac signal circuit of a JFET common-source amplifier. We assume that the bias solution and the small-signal resistances r_s and r_0 are known. The output voltage and output resistance can be calculated by replacing the circuit seen looking into the drain by the Norton equivalent circuit given in Fig. 10(b). These are given by

$$v_o = -i_{d(sc)} (r_{id} \| R_{td}) = -G_{mg} (r_{id} \| R_{td}) v_{tg} \tag{32}$$

$$r_{out} = r_{id} \| R_{td} \tag{33}$$

where G_{mg} and r_{id}, respectively, are given by Eqs. (26) and (25). Because the gate current is zero, the input resistance is infinite.

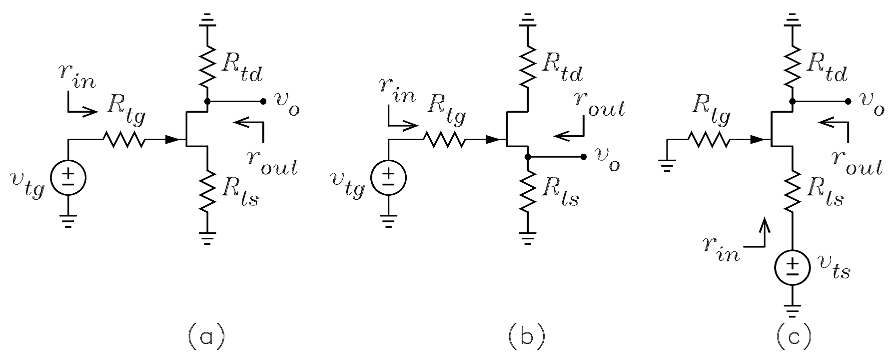

Figure 10: (a) Common-source amplifier. (b) Common-drain amplifier. (c) Common-gate amplifier.

The Common-Drain Amplifier

Figure 10(b) shows the ac signal circuit of a JFET common-drain amplifier. We assume that the bias solution and the small-signal resistances r_s and r_0 are known. The output voltage and output resistance can be calculated by replacing the circuit seen looking into the source by the Thévenin equivalent circuit given in Fig. 8(b). These are given by

$$v_o = v_{s(oc)} \frac{R_{ts}}{r_{is} + R_{ts}} = \frac{r_0}{r_s + r_0} \frac{R_{ts}}{r_{is} + R_{ts}} v_{tg} \tag{34}$$

$$r_{out} = r_{is} \| R_{ts} \tag{35}$$

where $v_{s(oc)}$ and r_{is}, respectively, are given by Eqs. (30) and (31). Because the gate current is zero, the input resistance is infinite.

The Common-Gate Amplifier

Figure 10(c) shows the ac signal circuit of a JFET common-gate amplifier. We assume that the bias solution and the small-signal parameters r_s and r_0 are known. The output voltage and output resistance can be calculated by replacing the circuit seen looking into the drain by the Norton equivalent circuit given in Fig. 7(b). The input resistance can be calculated by replacing the circuit seen looking into the source by the Thévenin equivalent circuit given in Fig. 8 with $v_{s(oc)} = 0$. These are given by

$$v_o = -i_{d(sc)} (r_{id} \| R_{td}) = G_{ms} (r_{id} \| R_{td}) v_{tg} \tag{36}$$

$$r_{out} = r_{id} \| R_{td} \tag{37}$$

$$r_{in} = R_{ts} + r_{is} \tag{38}$$

where G_{ms}, r_{id}, and r_{is}, respectively, are given by Eqs. (27), (25), and (31).

Small-Signal High-Frequency Models

Figure 11 shows the hybrid-π and T models for the JFET with the gate-source capacitance c_{gs} and the gate-drain capacitance c_{gd} added. The capacitor c_{gss} is the gate-substrate capacitance which in present in integrated-circuit devices but is omitted in discrete devices. These capacitors model charge storage in the device which affect its high-frequency performance. They are given by

$$c_{gs} = \frac{c_{gs0}}{(1 + V_{SG}/\psi_0)^{1/3}} \tag{39}$$

$$c_{gd} = \frac{c_{gd0}}{(1 + V_{DG}/\psi_0)^{1/3}} \tag{40}$$

$$c_{gss} = \frac{c_{gss0}}{(1 + V_{SSG}/\psi_0)^{1/2}} \tag{41}$$

where V_{SG}, V_{DG}, and V_{SSG} are dc bias voltages; c_{gs0}, c_{gd0}, and c_{gss0} are the zero-bias values; and ψ_0 is the built-in potential. The voltage V_{SSG} is the gate to substrate voltage.

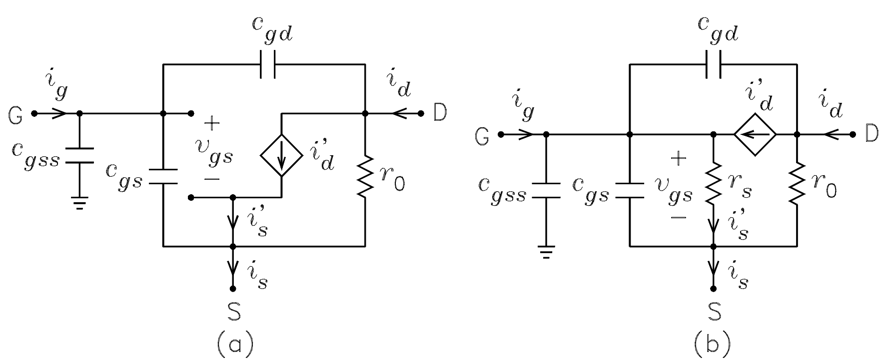

Figure 11: Small-signal high-frequency models of the JFET. (a) Hybrid-π model. (b) T model.