ECE 4894

Introduction and Course Overview
Outline

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Definitions

Computer-Aided Design

– Design where a significant portion of the decisions are automated via an algorithm

VLSI

– Any CMOS chip design over 10,000 transistors (basically, any digital chip design)

Not of interest

– Custom VLSI design, e.g., specialized memories or unique adders and multipliers
– Any specialized circuit technique which is done most by hand (by designer’s intuition and knowledge)

In summary…

– This course covers the vanilla, chocolate and strawberry of ice cream, **not** the toppings or other special flavors!!!
Course Content: Lecture Topics

“SYNTHESIS”
- Introduction to Logic Synthesis
- Logic synthesis and two-level logic optimization
- Multilevel Logic Synthesis
- Algebraic Methods
- Boolean Methods
- Timing Issues in Multi-Level Synthesis
- Library Binding
- Introduction to High-level Synthesis
- Architectural Synthesis
- Scheduling

“LAYOUT”
- Review of Design and Fabrication of VLSI Devices
- Partitioning
- Clustering
- Floorplanning
- Placement
- Steiner Routing
- Multi-net Routing

“TEST”
- Introduction to Test Issues and Concepts
- Fault Models: Stuck-at and Timing Failures
- Test Synthesis and Scheduling for Embedded IP Cores
- Built-in Self Test for Memory and Logic
- Design for Testability and Boundary Scan
Die size: 9.3mm x 9.3mm
Process: 65nm LP
Supply voltage: 1.2V (internal), 1.8/2.5/3.3V (I/O)
# of TRs, gates, memory:
307M TRs (28.2M Gates, 30.7Mb-RAM, 6.4Mb-ROM)
CPUs: ARM926EJ-S, 166MHz [modem control];
ARM1176JZF-S, 500MHz [application]; SH-X2, 500MHz [multimedia]
2G/3G modem:
WCDMA/HSDPA category 8,
GSM/GPRS/EDGE
Multimedia hardware:
VPU(MPEG4/H.264/VC-1 D1 size), VIO (Camera interface 12M pixels), 3D/2D Graphics, GPS, LCDC, Sound Processing Unit(SPU),
512KByte MediaRAM(MERAM)
I/O: 617 pins

A 65nm dual-mode baseband and multimedia application processor SoC with advanced power and memory management, Kamei et al., ASP-DAC 2009, pp. 535-539.
Lab Plan

Each student will “champion” a particular lab
  – will work with me directly on the lab
  – will produce a web page overview and instructions
  – will do the assignment and turn it in to me
  – grading will not be competitive but instead will be based on completeness
  – the goal is to make students “jack-of-all-CAD-tools”

Tentative list: three synthesis labs, three place and route labs and three test labs
The Complex Systems Problem

Exploding Complexity + Accelerating Rate-of-Change of the Technology Base + Static Design Technology = Big Trouble

AP/TP Abstraction Hierarchy + Abstractions Support Evolving H/W and System-S/W + IC CAD Model of Success = Leveraged Pivot Position: • Systems Eng. • S/W Eng. • IC CAD

Best Chance Solution Path

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Enabling Technologies

IC CAD

- Behavior
- Register
- Gate
- Mask

Candidate for Complex Systems

System Specification

- Application
  - Detect / Class
  - Track / Localize

- Target-Platform
  - Data Base / Security
  - Real-time Network

Architecture

- Beamforming
- Signal Processing

- Network Topology
  - DSP/GP/Mem/IO

Component

- FFT / Wavelet
- Spectral Analysis
- Signature Match

- I860 / ATM / VME
- RTOS / CORBA

Physical

- Application SW
  - Task / TP Binding
  - Application Routing & Scheduling

- System Software
  - Configuration
  - Physical HW Layout

Functions to be Performed

Identify Components & Interconnections

Task & Component Specifications

Code & Physical

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Increasing Cost of Chip Design*

Example: Design with 80 M transistors in 100 nm technology

Cost and risk continue rising

Top cost drivers

- Verification (40%)
- Architecture Design (23%)
- Embedded Software Design
  - 1400 man months (SW)
  - 1150 man months (HW)
- HW/SW integration

12 – 18 months


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Comments on the Semiconductor Market

Disclaimer: these numbers are from Professor Mooney’s memory over the past decade and thus their accuracy is not guaranteed

Global Sales of Semiconductors is ~$300B
In the 1970’s, there were approx. 5,000 chip designers worldwide; in the 1990’s, the number was ~50,000
By 2000, there were ~12,000 new chip design starts, but by the mid 2000’s, half that number (i.e., 6,000) with the same market size: clearly, design teams are much larger
The CAD market is approximately $3B with most of the revenue recorded by the “big three” of Cadence, Mentor Graphics and Synopsys
Fabless Semiconductor startups are currently quite rare
A Comment on Textbooks and Lecture Notes

This is an undergraduate course based on three graduate courses: ECE 6132, ECE 6133 and ECE 6140. The required text is related to ECE 6140.

ECE 6132 is based on *Synthesis and Optimization of Digital Circuits* by Giovanni De Micheli.

ECE 6132 is based on *Practical Problems in VLSI Physical Design Automation* by Sung-Kyu Lim.

Lecture notes will be mostly taken from the accompanying lecture slides provided for the course text and the above two textbooks.

Advice: follow the lecture notes closely!!!