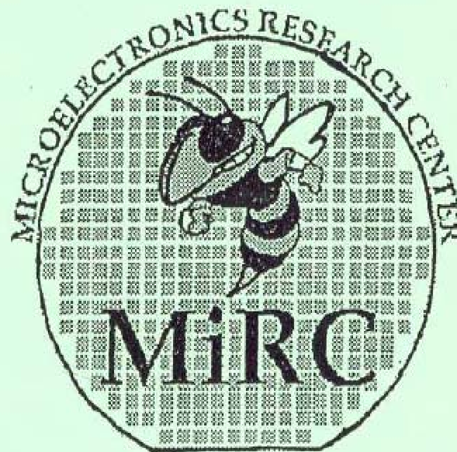
GEORGIA
INSTITUTE OF TECHNOLOGY

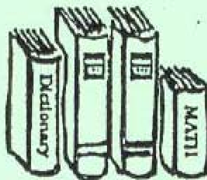
MICROELECTRONICS RESEARCH CENTER

"REDEFINING THE LEADING EDGE"

CLASS HANDBOOK

Course EE / ChE 4752
Microelectronics Processing Laboratory





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GEORGIA INSTITUTE OF TECHNOLOGY
Schools of Electrical and Computer Engineering / Chemical Engineering

COURSE TITLE: "Microelectronics Processing Laboratory"

INSTRUCTORS: Professor Paul A. Kohl (Chemical Engineering)
Professor Ajeet Rohatgi (Electrical & Computer Engineering)
Mrs. Laureen Rose (Laboratory Instructor)

REQUIRED TEXT: Vol. V Introduction to Microelectronic Fabrication Second Edition
Richard C. Jaeger, 2002, 1998 by Prentice Hall
Modular Series on Solid State Devices

COURSES POLICIES:

1. In the laboratory, <u>SAFETY</u> is of utmost concern. Although all lab procedures are safe if Done properly, improper procedures can result in severe injuries. Disregard for safety Procedures will be grounds for expulsion from the course with a grade of "D".

2. There will be a short homework assignment handed out each week to be completed by the following lecture. Also, laboratory notebooks may be inspected prior to each session to insure that the session's instructions have been recorded.

3. For the laboratory, you will be divided into groups of two or three. The lab report will be a Group effort (i.e. – only one report is due from each group). ALL other requirements for the course will be INDIVIDUAL efforts.

4. Since we are on a rigid schedule, and because unsupervised independent work in the laboratory cannot be allowed due to safety reasons, it is extremely important that students attend EVERY lab session. If you or your partner cannot attend a session, please notify your instructor ASAP. In these cases, the laboratory instructor can be "hired" to process your wafer at a "cost" of a 10% reduction in your non-exam points for the course per occurrence, except as described below.

5. There may be scheduled *"catch-up"* sessions in the proposed lab schedule throughout the semester. In these cases, if you can convince the laboratory instructor to open the lab, you can make up work without the above penalty if YOU do the processing.

GRADING:

There will be one midterm exam and one final exam. The remainder of the grade will be determined from the homework, laboratory notebook and the laboratory report.

Midterm Exam = 20%
Final Exam =20%
Homework =10%

Laboratory Notebook = 20%
Laboratory Report = 30%

The notebook and report are described in more detail elsewhere.

LECTURES AND LABS:

Lectures will be held on Thursday morning (9:30 – 11:00 Room 102A). Labs will be held Monday through Friday. Occasionally, lab time may be used for lecture if necessary. Some lab sessions may not take the entire three hours, but others may take every available minute. Therefore, all lab sessions will begin PROMPLTLY.

EXAM DATES:

The midterm and final exams will both be of the same weight and length (1. 5 hours). The midterm will be closed book and notes, but the final will be open book and notes.

OFFICE HOURS:

Dr. Kohl: Microelectronics Research Center (Pettit Bldg.) Room 119
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EE / ChE 4752 Microelectronics Processing Laboratory

Laboratory Instructor: Ms. Laureen Rose

Location to Laboratory: MiRC / Pettit Bldg. Room 150

Note: The Pettit Building is the Microelectronics Research Center, which is adjacent to the Van Leer Building (791 Atlantic Drive).

Class Rules and Regulations:

1. In the lecture sessions, please note: there is no eating, drinking, or smoking.

2. In the laboratory sessions, please note: "*SAFETY*" is of the utmost concern in this class. Although all procedures in this laboratory are safe if done properly, improper procedures can result in severe injuries. Therefore, repeated or intentional disregard for the safety procedures of this course will be grounds for expulsion from the course and a grade of "D", regardless of past performance in the course.

3. If anyone in this course is graduating this quarter, you are exempt from the final examination. However, you must still hand in a laboratory notebook and a laboratory report.

4. There is no formal homework required for this course. However, your laboratory notebooks may be inspected prior to each laboratory session to make sure that you have recorded that session's instructions in your notebook.

5. For this laboratory course, you may be divided up into groups of two. If so, the laboratory report will be a group effort (i.e., I expect to receive one laboratory report from each group). ALL other requirements for the course are to be INDIVIDUAL efforts. If you have any questions regarding when your fellow students can help you and when they can't, please see your instructor.

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Microelectronics Research Center
Microelectronics Processing Laboratory

LABORATORY NOTEBOOK

This handout outlines what is expected in your laboratory notebook and laboratory report.

Your laboratory notebook should contain everything that you have done in the laboratory, including results of tests and device performance. Since everyone has been bringing their laboratory notebook to every lab, your notebook should have in it (among other things) condensed versions of the procedures used, any observations, anomalous or otherwise, you observed during the processing, intermediate characterizations such as oxide thickness', sheet resistivities, and calculated junction depths, and the results of testing your transistors and resistors.

The following criteria (in order of importance) will be used in grading your laboratory notebook;

(1) COMPLETENESS – is everything there?
(2) AUTHENTICITY – did you actually record things 'as they happened' (good) or did you copy things in later (not as good)? Are pages of your notebook dated? Your observations can be recorded on the sheets that have comments / notes. If you used these instead of your notebook, are these dated and taped (or stapled) into your notebook?
(3) NEATNESS – The notebook is a handwritten item, so I don't expect it to be as neat as your report. However, I do expect to be able to read and follow it without too much effort deciphering either handwriting or logic.

Each individual student should hand in a laboratory notebook. The laboratory notebook is 20% of your grade.

LABORATORY REPORT

Your laboratory report should be a condensed version of the laboratory experiments, with some additional explanations, observations and calculations. The report will be divided into sections (called "sections" below) which will generally correspond to specific processing step in the fabrication of the CMOS FETs, in the order you performed them (e.g. characterization, field oxidation, etc.).
Each section should contain:

A. Summary of the theory or concept behind the processing step. If the processing step is repeated more than once (e.g. oxidation), the theory or summary need only appear once, in the first section. This should take less than one to two typed pages.

B. Results, the results of the laboratory should be presented in a logical, easily read form.

C. Comment on Sections A, and B above. Compare what actually happened to what was supposed to happen. For example, in an oxidation step you could compare the actual oxide thickness to the calculated one.

D. Specific calculations or questions will be required for each section. They will be distributed in lecture.

The individual sections of the report will be handed in soon after that processing step is performed. You will be asked to answer specific questions for each section. The individual sections will be graded and

returned to you for the final report, you should combine sections 1 – 6. Correcting errors in previous sections prior to final submission will improve your overall grade.

Remember, the laboratory report must be TYPED. If there are complex equations which you wish to include, and cannot easily render them on your typewriter or word processor, it is OK to write them in NEATLY by hand.

SECTIONS:

1. Characterization and Field Oxidation
2. Photolithography
3. Boron Diffusion
4. Gate Oxidation and drive-in (calculations and discussion only)
5. Metallization
6. Device Characterization / Final Report

GRADING:

Your grade will depend on a midterm exam (20%), a final exam (20%). Your laboratory notebook will be (20%) and your laboratory report (30%). The remainder of the grade will be determined from the homework (10%), which is more detailed in accompanying handouts.

EXAMS:

The exam will be designed to be completed in an hour, and you will have the full class time to work on it. The final exam will be the same weight and length. The format of the midterm exam and final exam will be open book and notes. Partial credit will be given on all exams. Please note that academic honesty is of paramount importance to insure that the class and grading is fair to all students. Academic dishonesty will not be tolerated. If you have any questions regarding what is and is not allowed, please see your instructor prior to the exam.

There will be no make-up exams for this course. A grade of zero will be given for any missed exam for which there have been no arrangements made beforehand, unless you have written medical excuse.

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LABORATORY HANDOUTS:

The following set of handouts contains material which will be needed for the laboratory sessions.

They include:

- A. Laboratory Safety and Clean Room Procedures.
- B. Laboratory Sessions and Description.
- C. Equipment Operating Procedures.

The Laboratory Safety and Clean Room Procedures handouts should be read prior to first entering the lab, and referred to throughout the quarter. Familiarity with the material included will be expected at all times when you are in the lab. Safety and cleanliness are of the utmost importance.

The processing sequence has been divided into several Laboratory Sessions. The handouts for each session will serve as a detailed description of the procedures for each day in lab. The procedures you will follow in your Laboratory Session should be recorded in your laboratory notebook prior to the beginning of the lab session.

Your Laboratory Notebook should be a bound volume of pages, which are numbered in ascending order and cannot be detached from the notebook. Record in this notebook all laboratory procedures as well as any and all observations, measurements, and results which you obtain. Neatness, logical order, but above all, completeness is of the utmost concern. If you make a mistake in your notebook, *DO NOT* erase it, but cross it out lightly so that it can still be read. In addition to your notebook, a typed Laboratory Report will be collected at the end of the course.

Bring to each lab period:

All past Sessions — as they will be referred to

The present Session

The next Session — in the unlikely event that we get slightly ahead

Before each laboratory period read the Lab Session notes to be used that day, and record them into your Laboratory Notebook.

Finally, there are a number of Equipment Procedures written for specific pieces of equipment to be used in the course. These Procedures will be referenced in the Laboratory Session whenever they are applicable. Be sure to have read all Procedures for any given day's Laboratory Session in preparation for the lab period.

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LABORATORY SAFETY:

The chemicals and equipment used in this laboratory are not toy. They are of research level and quality, and must be used with intelligence and respect. Instruction sheets for the operation of major pieces of equipment have been provided. Refer to these handouts as necessary when using the equipment. Any machines that are not used by the course should not be handled by unqualified users.

Chemical safety is also very important. The majority of this handout is dedicated to chemical conerns. Depending on your background, these notes will either be a reminder of past concerns, or new material which you may have never seen before. In either case, read them carefully, such that you fully understand them. If you have any questions, please ask your instructor.

The lab facility is small for the number of users. Therefore, it is important to respect other's workspace in the lab. As there will be up to six or more students in each lab group, the class must be especially concerned. The course shares the lab space with advanced undergraduate and graduate student researchers. Remember that your actions in the lab could affect someone else's work, so it is important to follow instructions, both written and oral.

Safety as well as cleanliness requires the use of protective clothing. These should be *worn at all times* while in the laboratory:

Lab Coat

Bouffant Cap

Shoe Covering (booties)

Safety glasses --- Prescription eyeglasses are acceptable. Wearing of contact lenses is discouraged. Contact lenses greatly increase the likelihood of permanent eye damage should a chemical splash contact the eye, as the chemical can become trapped between the lens and the eye. If you do wear contact lenses, be sure to notify your instructor, so that proper care can be given if necessary.

A supplemental handout describes the safety guidelines in the *"research"* clean room downstairs. Be sure that you review that document as well as these handouts, as many of the safety guidelines and concerns are similar.

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SAFETY GUIDELINES:

1. NO OPEN-TOE SANDALS, BARE FEET, or SHORTS allowed in the lab.

2. All work with acids and solvents must be done under an exhaust hood. This includes opening of bottles.

3. Never pour excess chemicals back into the original bottle. Discard any excess acid into the sinks with the tap running, and discard organic solvents into the solvent waste bottle under the fume hood.

4. Persons handling chemicals should wash hands after use.

5. Food or beverages are not allowed inside the laboratory.

6. Never use laboratory glassware as drinking glasses.

7. Clean up your work area during and after use. DO NOT leave hazards for others.

8. Material Safety Data Sheets are available in the lab for all chemicals used. The instructor will be familiar with these, in case of accidental contact. You should be familiar with safety procedures in case of a spill of a particular chemical.

9. Familiarize yourself with the location of chemical showers and eye washes.

10. Emergency procedures are posted near the telephone in the lab. To reach CAMPUS POLICE DIAL 4-2500.

11. Report ALL safety violations and hazards to your instructor.

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ACID HANDLING:

1. In case of accidental contact with any acid, flush immediately with copious quantities of running water. All burns must be report to your instructor immediately.

2. When mixing solutions containing acids, always pour acid into water, ***NEVER*** the reverse. Begin pouring acids slowly. Excessively violent reactions may occur if mixed incorrectly. This is especially true when mixing Sulfuric Acid (H2S04).

3. After mixing acid solutions, allow solutions to cool thoroughly before capping. Heat is generated after mixing which can cause pressure in a capped bottle.

4. After use, always cap acid bottles tightly.

5. All chemicals poured into a sink will mix in the piping --- please run lots of water between chemicals, and always before and after dumping any chemical into the sink.

6. Keep in mind that while other chemical fumes are strong irritants or corrosive, hydrofluoric acid (including buffered oxide etch, BOE) is lethal if inhaled.

DANGER --- HYDROFLUORIC ACID (HF)

Hydrofluoric acid does not produce overt tissue burns like most acids. However, HF does diffuse through tissue and will dissolve bone. Whereas other acids, bases, and solvents are strong irritants, cumulative poisons, or carcinogenic, HF fumes can be *fatal.*

For these reasons, particular caution should be exercised when handling HF.

Immediately report any possible contact to your instructor.

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SOLVENT HANDLING:

1. Organic solvents, such as acetone and trichloroethylene, will react with acids or other strong oxidizing materials such as hydrogen peroxide. DO NOT MIX THEM. A mixture of nitric acid and acetone, for example, is highly explosive.

2. Solvents should be poured into the waste solvent bottle located in the fume hood.

3. Most solvents present some degree of toxic hazards when their fumes are inhaled over a prolonged period. Always work with solvents in an exhausted hood.

4. Avoid getting solvents onto the skin. Solvents are readily absorbed through the skin and into the bloodstream. Some solvents, such as trichloroethylene, are carcinogenic.

5. Solvents are generally quite flammable. Though there are few ignition sources in the lab, always be cautious of solvents near any source of a spark.

6. Photoresist contains organic solvents as part of its makeup. These solvents can be as hazardous or more so than the other solvents used in the laboratory. Avoid skin contact or breathing the fumes of photoresist.

DANGER — MERCURY VAPORS AT ROOM TEMPERATURE

Mercury evaporates at room temperature, and is highly toxic. Notify your instructor if you break a thermometer or spill mercury.

UV light sources (present in the mask aligners) are normally quite safe. However, when these lamps approach their useful end, they can overheat and explode. This releases toxic mercury fumes into the room. Should this happen, immediately leave the area and notify your instructor.

After turning off a normal UV lamp, it must cool for 30 minutes before restarting. Failure to do this may result in a bulb explosion.

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CLEANROOM PROCEDURES:

In order to preserve the integrity of work in a semiconductor processing facility, a number of 'clean' practices must be followed. Dirt, dust, fingerprints, perfume, hair sprays, sneezes, etc. are the scourge of the semiconductor industry. Steps must be taken to protect your devices from contamination, or fabricated devices will not function as desired. It is important to keep wafers covered except when processing. Also, keep your tweezers and other objects used for handling wafers clean. Follow all cleaning procedures carefully, and once cleaned, transfer wafers without delay to the next process. The written procedures are designed to minimize contaminants if followed.

1. Always wear all of your protective clothing.
2. Do not bring pencils into clean room.
3. Remain in clean areas only when processing. No visitors without permission.
4. NEVER put your head in laminar flow, especially over wafers.
5. Move hands slowly in and out of laminar flow.
6. Avoid tapping feet or running in clean areas.
7. Never touch wafer holders without gloves.
8. Always use complete cleaning procedures.
9. Never handle wafers with metal tweezers after an RCA clean.
10. NEVER touch metal tweezers to quartz furnace boats.
11. Do not allow furnace pushrods and thermocouples to touch anything except designated furnace tubes, boats and holders.

SAFETY QUIZ

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CHE 4752 / EE 4752 Microelectronics Processing Laboratory

NAME: ______________________________

1. Should you add acid to water or water to acid, why?

   ____

2. If someone is not following the safety procedures, give two possible actions you could take? 1.) ______________________________

   2.) ____

3. Name 3 pieces of safety clothing for this lab:

   1) ____
   2) ____
   3) ____

4. Give two reasons why HF is dangerous:

   1) ____
   2) ____

5. Give two reasons why solvents should be used in a hood:

   1) ____
   2) ____

6. You are about to use the mask aligner and someone turned it off, what should you do before restarting it? ________________________

   ____

7. What do you do if someone spills acid on their clothes?

   ____

   ____

8. What do you do if someone spills acid on their face?

   ____

   ____

9. Why should you not mix acids and solvents?

   ____

   ____

10. What is the emergency phone number? ________________________

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SUBSTRATE CHARACTERIZATION PROCEDURE:

It is necessary to characterize the starting material in a semiconductor process, as the material dopant type and amount must be correct for a certain process to work as designed. This lab process requires wafers of the following characteristics:

- N-type (Phosphorous dopant)
- 10^{14}-10^{15} cm^{-3} Dopant concentration
- <100> Crystal Orientation
- 5-20 Ω-cm Wafer Resistivity

The first set of measurements is to verify that the starting material has these necessary characteristics. The tests are destructive, so the control wafer used here is not processed.

1. On control wafer, C1, determine the carrier type (n or p) using the hot probe.

2. Measure the wafer thickness with the micrometer.

3. Measure the wafer sheet resistivity in Ω / square, using the 4-pt probe. Multiplying by the thickness will yield the bulk resistivity. Given that the mobility of electrons is 1800 cm^2 / Vs, what is the dopant concentration?

4. Check location of wafer flats to verify crystal orientation. The secondary flat opposite the primary flat, signifies n-type < 100 >. Other dopant types and orientations have different locations for the secondary flat.

5. Using a diamond scribe, or sharp tweezers, it is possible to break a wafer cleanly along the orientation plane. After other characterizing measurements have been taken, break up the wafer in order to observe the single-crystal nature of the substrates.

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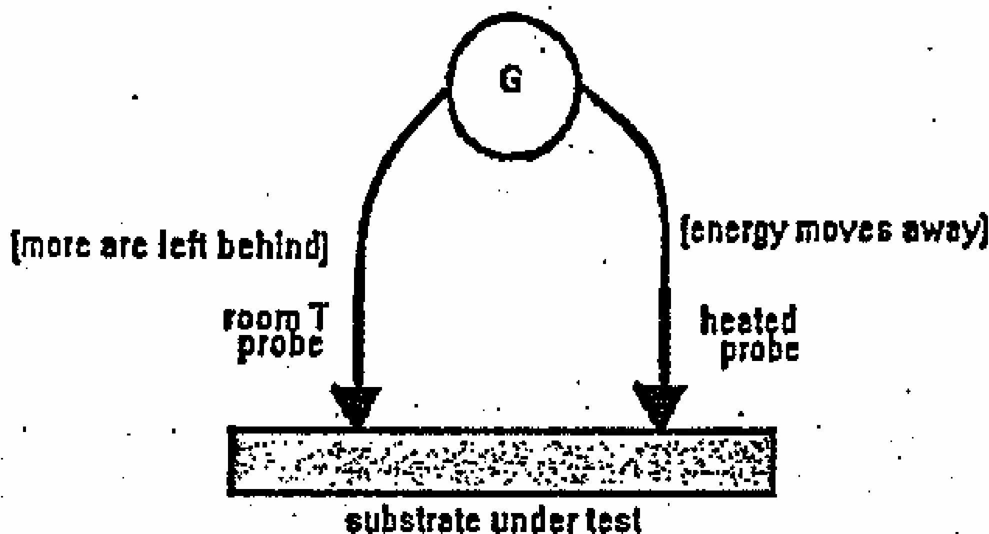
HOT PROBE DETERMINATION OF CARRIER TYPE:

A hot probe may be used to determine the majority carrier type of a semiconductor with resistivity less than 1000Ω-cm. Two sharply-pointed metal probes are used to contact the sample. One of the probes is heated while the other remains at room temperature. A galvanometer is used to detect rthe direction of current flow between the two probes:



The majority carriers under the heated probe have greater thermal energy than those in the cooler portions of the wafer. These higher energy carriers diffuse away from the probe leaving a net fixed charge at the hop probe with polarity opposite to majority carrier type. An electric field is then established in the semiconductor between the majority carrier type. An electric field is then established in the semiconductor between the majority carriers diffusing away from the hot probe and the fixed charges left behind.

The potential thus generated is detectable at the probes using an electrometer. Alternately, the flux of majority carriers can be measured using an ammeter. A positive potential implies *n-type* material while a negative potential implies *p-type* material.

(SHOULD BE DONE IN ORDER)

R C A CLEANING PROCEDURE

ORGANIC CLEAN ---------------------------------- 80 oC ------------ 15 min.

BUBBLER RINSE ---------------------------------- 5 min.

H.F. DIP -- 15 sec.

BUBBLER RINSE ---------------------------------- 30 sec.

IONIC CLEAN ------------------------------------ 80 oC ------------ 15 min.

BUBBLER RINSE ---------------------------------- 15 min.

N2 DRY -- CLEAN

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RCA PROCEDURE:

This is cleaning procedure that should be done of wafers that will go in any of the high temperature furnaces. Wafers to be cleaned should have a *Si*, SiO_2 or Si_3N_4 surface, and not have gone through a metallization step. Any other substrate should use different glassware and cleaning facilities. This handout is intended to serve only as a guideline; ***all users MUST be given explicit permission by the laboratory instructor*** to use the cleaning station. If you wish to deviate from this procedure, or have any questions, consult with your laboratory instructor.

NOTES

- Wear poly gloves while working in clean station
- Due to safety reasons, keep hood sash down when not in use.
- Use the white Teflon wafer carrier for the clean.
- Use fresh chemicals for each clean.
- Chemicals should not be brought to a boil, as this causes rapid decomposition of H_2O_2.
- When measuring chemicals, use the appropriate (i.e., organic or ionic) beaker, graduated cylinder, and heating bath. DO NOT MIX THEM UP.
- Always place carrier handle and TEFLON tweezers in solutions and rinses with carrier and wafers.

A. Start-Up

1. Turn on DI water flow to the rinse station. The knob is located in the front of the station . Take care that the knob is not opened too far, as this could cause overflowing of the station. Consult your laboratory instructor if you are unfamiliar with the setup.

2. Turn on N_2 flow knob to the rinse station. This is done by adjusting the regulator knob located next to the DI knob in front of the sink. When correctly adjusted, there should be a gentle bubbling of nitrogen through the rinse station.

3. All cleaning solution should be made at the same time to minimize delay in processing. Thus, as soon as the organic removal solution has been made and is heating, start on the ionic solution.

B. ORGANIC CLEAN

1. Prepare solution for organic clean

   In quartz tank marked (O),

   Add: 1000 ml DI (H_20)

   200 ml H_2O_2

   200 ml NH_4OH

2. Turn left hot plate switch ON and adjust the hot plate temperature to 350. The solution should heat for 15 minutes, in order to reach 80°C.

3. Submerge wafers into the warming solution as soon as possible.

4. During heating time, prepare solutions for Oxide Stripping and Ionic Removal (see below).

5. When the organic solution begins to bubble, immerse the wafer carrier with your wafers for 15 minutes.

6. Remove carrier and wafers from left tank, and immediately place in the bubblier rinse tank for 5 minutes.

7. Turn off hot plate and allow solution to cool to room temperature.

C. OXIDE STRIPPING

1. *To be done during step #4 above:*

   The following HF solution will be prepared *by the laboratory instructor:*

   In the left polypropylene vat marked HF TANK, a 50:1 HF dip as follows:

   Add: 4500 ml DI H_20 (tank is marked to the required level)

   50 ml HF

2. Remove the carrier and wafers from the bubblier rinse, and carefully submerge it into the "50:1" HF solution agitating in the direction of the wafers for 15 sec.

3. Transfer the carrier to the bubblier for 30 seconds. (This should not be any longer, as to avoid reformation of a hydrous oxide film).

4. Immediately transfer to Hot Ionic Clean (right quartz vat).

D. IONIC CLEAN

1. *To be done during step #4 of Organic Clean:*
   Prepare solution for ionic clean in quartz marked (I),
   Add: 1000 ml DI (H_20)
   200 ml H_20_2
   200 ml HCl

2. *To be done during step #4 of Organic Clean:*
   Turn left hot plate switch ON and adjust the hot plate temperature to 350. The solution should heat for 15 minutes, in order to reach 80°C.

3. Submerge the still wet wafers from the HF Rinse into the Hot Ionic Cleaning solution.

4. Maintain wafers in 80°C solution for 15 minutes.

5. After 15 minutes has elapsed, transfer wafers directly to the bubblier rinse.

6. Turn *off* hot plate and let solution cool to room temperature.

E. FINAL RINSE AND DRY

1. Rinse the wafers in the bubblier rinse tank for 15 minutes.

2. After wafers have rinsed for 15 minutes, remove from bubblier rinse and place wafer carrier in black box, transfer to wafer dryer using standard procedure.

3. Turn off DI water and N_2 flow to rinse tank.

4. After completing drying cycle, carefully remove wafer carrier back into the black box replace cover, transfer to furnace boat loading area, and immediately load wafers into the furnace.

5. After hot solutions have cooled to room temperature, empty and rinse the cleaning tanks with DI water.

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FIELD OXIDATION PROCEDURE:

This process will thermally oxidize the silicon substrate. The oxide grown will be a thick field oxide to isolate the devices and define the source and drain regions for subsequent diffusion.

1. RCA clean device wafers and control wafer C2. Refer to RCA Clean handout for procedure in substrate cleaning station. During the cleaning, continue with the next three items, preparing the oxidation furnace.

2. Verify that the gases flowing through the furnaces are in the IDLE CONFIGURATION:

   Note that in the idle configuration, nitrogen gas is flowing through all three furnaces.

3. Turn on the oxidation furnace and adjust it to 900° C. This is accomplished by adjusting the furnace controller in the back of the furnace clean hood.

4. Fill bubble flask with DI water and turn the controller dial to 50, then immediately back to 25. This will start heating the water in the bubblier to a temperature between 90 and 100° C.

5. At the completion of the RCA clean, remove the quartz boat from the furnace using appropriate push rod and quartz boat loader. *Always wear poly gloves and / or high temperature gloves when handling quartz ware.* DO NOT hold push rod in front of mark on rod. Keep the boat in the boat loader and set the boat loader down in front of the furnace tubes, taking care that holder and boat remain in laminar flow.

6. Place the RCA – cleaned wafers, still in their carrier, into the carrier box, and transport them to the furnace loading station. Load wafers onto quartz boat using Teflon or Teflon – tipped tweezers. Avoid passing arms or head over cleaned wafers.

7. With boat loader, return wafers on boat to oxidation furnace. Slowly push boat into the mouth of the furnace with push rod, to avoid wafer fracturing due to thermal stress. Push the quartz rod in just to the point where the mark on the push rod is even with the metal door to the furnace. This will place the center of the boat at the center of the furnace.

   The field oxidation process is to be carried out at 1100° C. The process is:

   a. Load in N_2 (Idle gas)
   b. Dry O_2 5 minutes
   c. Wet O_2 120 minutes
   d. Dry O_2 5 minutes
   e. Unload in N_2 (Idle gas)

8. Ramp the furnace controller up to the oxidation temperature of 1100° C.
Lock in ramp mode. Wait until the temperature has stabilized (about 10 minutes).

9. Begin dry oxygen flow through the tube.

>> turn oxide furnace valve to O_2
>> valve to Dry or Wet should be facing Dry

Dry oxygen is now flowing through the tube ADJUST the flow rate to 94.70 sccm, (standard cubic centimeter minute).

10. When 5 minutes have elapsed, begin WET oxygen flow through the tube.

>> turn valve from DRY to WET

Wet oxygen (i.e., a combination of oxygen and steam) is not flowing through the tube. Note that oxygen is flowing through the bubblier mounted in the back of the furnace.

11. When 120 minutes have elapsed, start DRY oxygen flowing through the tube.

>> turn valve from WET to DRY

12. Turn OFF HEATER to the wet oxidation bubblier.

13. When 5 minutes have elapsed, start nitrogen flowing through the tube, i.e., return the gas delivery system to its IDLE CONFIGURATION:

>> turn oxide furnace valve to N_2

14. Set furnace to 900° C, lock in ramp mode and wait 10 minutes for it to cool to approximately 900° C.

15. Pull wafer boat slowly to the mouth of the furnace with push / pull rod. Let wafers cool briefly before completely removing boat from furnace. Make sure that the wafers stay in laminar flow hood at all times.

16. Allow wafers to cool completely in boat before removing and storing in N_2 dry box.

17. With boat loader, return boat to oxidation furnace. Slowly push boat into furnace with push rod, approximately ¼ of the way into the furnace tube. Loosely replace end cap and store boat holder inside the metal furnace door.

18. Estimate the thickness of the grown oxide using the color charts as well as your calculation of approximately how thick the grown oxide should be.

19. Measure grown oxide thickness of control wafer using Ellipsometer, referring to Ellipsometer procedure (this may be deferred to later lab for time reasons).

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LAYER THICKNESS MEASUREMENTS

Color:

Both silicon dioxide and silicon nitride layers exhibit different colors on the wafer. We know that silicon dioxide is transparent (glass is silicon dioxide), yet it has a color on a wafer. The color is actually the result of an *interference phenomenon,* the same phenomenon that creates the colors of rainbows.

The silicon dioxide layer on a silicon wafer is actually a thin transparent film on a reflecting substrate. Some of the light rays impinging on the wafer surface reflect off of the oxide while others pass through the transparent oxide and reflect off of the mirrored wafer surface. When the light rays exit the film, they combine with the surface-reflected ray, resulting in a color.

The exact color is f function of three factors. One, which is a property of the transparent film material, is the *Index of Refraction.* A second factor is the viewing angle (rotate an oxidized wafer and the surface color will change). The third factor is the thickness of the film.

The color of a thin transparent film becomes an indication of the thickness when the nature of the viewing light is specified (i.e. daylight, fluorescent), along with the viewing angle. The classic color vs. thickness chart is a regular feature at oxidation and diffusion stations. Color alone is not an exact indication of thickness, due to the consequences of the interference phenomenon.

As the film gets thicker the color changes in a specific sequence and then repeats itself. Each repetition of the color is called an *order.* To determine the exact film thickness, a knowledge of the color order is necessary. A principle use of color charts is for process control.

Each oxidation or silicon nitride process is designed to produce a specified thickness. Naturally the thickness will vary run to run. Operators quickly become sensitive to the usual color. When a variation occurs, a quick check of the chart will indicate if the film thickness is out of specification. Rarely is a process so far off that the film thickness is a whole order (same color, different thickness) out of specification. The accuracy of color chart thickness determination is limited to the accurate perception of the colors (what exactly is red-orange). A typical chart is accurate to < or > 300 angstroms.

Ellipsometers:

Ellipsometers are film thickness instruments that use a laser light source. The laser light source is polarized. The effect of polarization is to create a wave that is traveling in only one plane. Polarization can be imagined by considering looking into the beam of a flashlight. In an ordinary beam light rays come to your eyes in many planes, like an arrow with many feathers. A polarized beam has all of the light in only one plane, or an arrow with only one feather.

In the ellipsometer the polarized beam is directed to the oxide covered wafer at an angle. The beam enters the transparent film and reflects off of the reflective wafer surface. During its passage through the film the angle of the beam plane is rotated. The amount of rotation of the beam is a function of the thickness and index of refraction of the film. A detector in the instrument measures the amount of rotation and an on-board computer calculates the thickness and index of refraction.

Ellipsometers are used to measure thin oxides (50 to 1200 angstroms). Their accuracy in this range is unequalled by other techniques.

Table 7.4 Color Chart for Thermally Grown SiO_2 Films Observed Perpendicularly Under Daylight Fluorescent Lighting*

Film Thickness (μm)	Color and Comments
0.05	Tan
0.07	Brown
0.10	Dark violet to red violet
0.12	Royal blue
0.15	Light blue to metallic blue
0.17	Metallic to very light yellow green
0.20	Light gold or yellow—slightly metallic
0.22	Gold with slight yellow orange
0.25	Orange to melon
0.27	Red violet
0.30	Blue to violet blue
0.31	Blue
0.32	Blue to blue green
0.34	Light green
0.35	Green to yellow green
0.36	Yellow green
0.37	Green yellow
0.39	Yellow
0.41	Light orange
0.42	Carnation pink
0.44	Violet red
0.46	Red violet
0.47	Violet
0.48	Blue violet
0.49	Blue
0.50	Blue green
0.52	Green (broad)
0.54	Yellow green
0.56	Green yellow
0.57	Yellow to "yellowish" (not yellow but is in the position where yellow is to be expected. At times it appears to be light creamy gray or metallic)
0.58	Light orange or yellow to pink borderline
0.60	Carnation pink
0.63	Violet red
0.68	"Bluish" (Not blue but borderline between violet and blue green. It appears more like a mixture between violet red and blue green and looks grayish)
0.72	Blue green to green (quite broad)
0.77	"Yellowish"
0.80	Orange (rather broad for orange)
0.82	Salmon
0.85	Dull, light red violet
0.86	Violet
0.87	Blue violet
0.89	Blue
0.92	Blue green
0.95	Dull yellow green
0.97	Yellow to "yellowish"
0.99	Orange
1.00	Carnation pink
1.02	Violet red
1.05	Red violet
1.06	Violet
1.07	Blue violet
1.10	Green
1.11	Yellow green
1.12	Green
1.18	Violet
1.19	Red violet
1.21	Violet red
1.24	Carnation pink to salmon
1.25	Orange
1.28	"Yellowish"
1.32	Sky blue to green blue
1.40	Orange
1.45	Violet
1.46	Blue violet
1.50	Blue
1.54	Dull yellow green

* See reference 57.

Table 1 Rate constants for wet oxidation of silicon

Oxidation temperature (°C)	A (μm)	Parabolic rate constant B (μm²/h)	Linear rate constant B/A (μm/h)	τ (h)
1200	0.05	0.720	14.40	0
1100	0.11	0.510	4.64	0
1000	0.226	0.287	1.27	0
920	0.50	0.203	0.406	0

value of τ as defined in Eq. 14 must be used. Table 2 lists the values of rate constants for dry oxidation of silicon.[4]

Examination of Eq. 14b reveals that B is expected to be proportional to C^*, which, according to Henry's law, is proportional to the partial pressure of the oxidizing species. However, A should be independent of the partial pressure. This has indeed been confirmed experimentally for both wet and dry oxidations[4,8] in the temperature range between 1000 and 1200°C and between 0.1 and 1 atm. The pressure independence of A means that the linear rate constant B/A has the same linear pressure dependence as B.

Figure 3a shows the effect of temperature[4] on the parabolic rate constant B for both dry and wet oxygen at 640 Torr and for wet oxygen normalized to 760 Torr using the linear pressure dependence. As might be expected from Eq. 14, the temperature dependence of B is similar to that of D, that is, B increases exponentially with temperature. For dry oxygen the activation energy for B is 1.24 eV, which is comparable to the value of 1.17 eV for the diffusivity of oxygen through fused silica (similar in structure to thermal SiO_2). The wet oxygen activation energy (0.71 eV) also compares favorably with the activation energy for the diffusivity of water in fused silicon (0.80 eV).

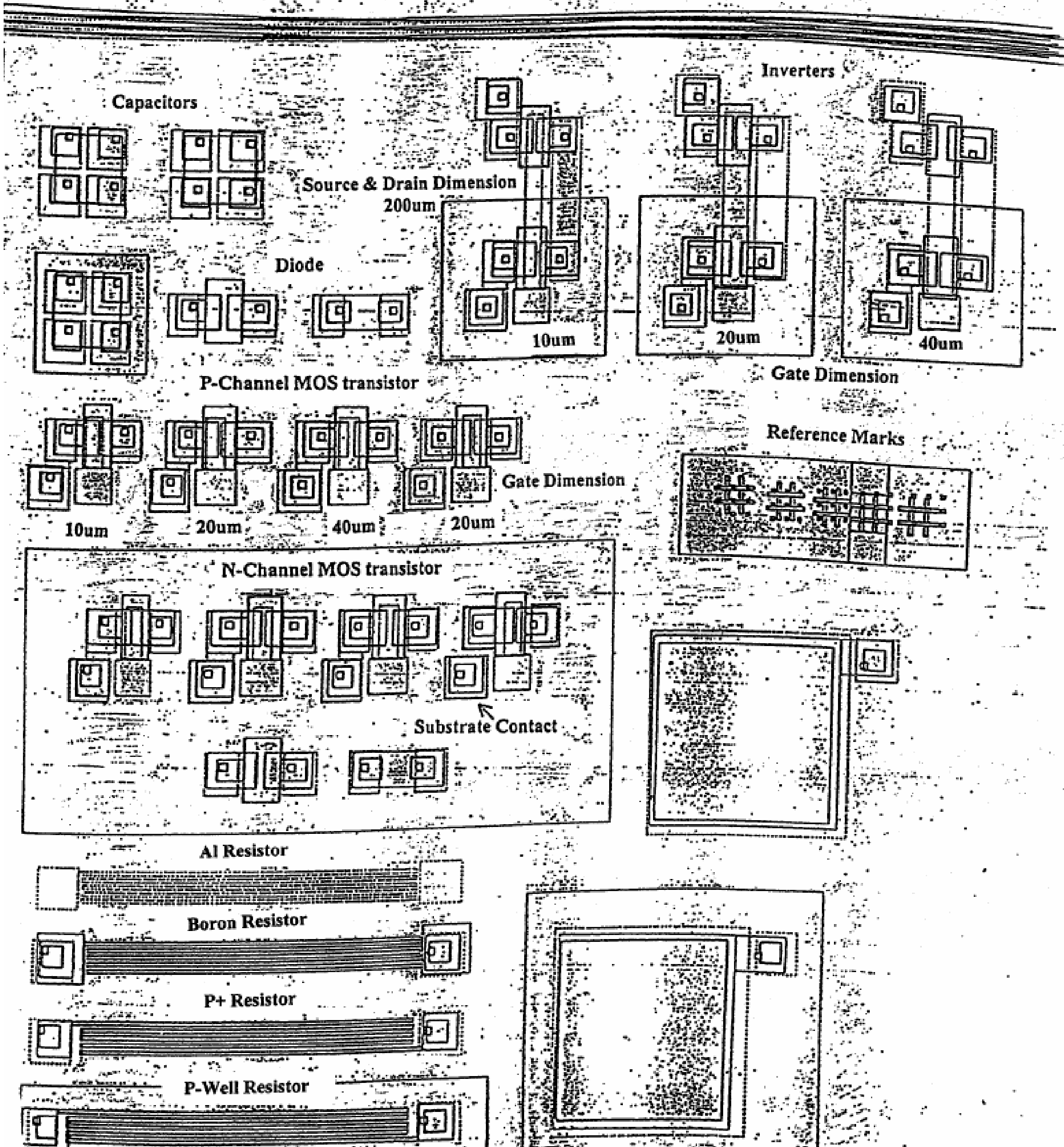
Figure 3b shows the temperature dependence of the linear rate constant B/A for both dry and wet oxygen at 640 Torr and for wet oxygen normalized to 760 Torr. Once again an exponential dependence is observed with activation energies 1.96 and 2.0 eV for wet and dry oxidation, respectively. Deal and Grove[4] show that these

Table 2 Rate constants for dry oxidation of silicon

Oxidation temperature (°C)	A (μm)	Parabolic rate constant B (μm²/h)	Linear rate constant B/A (μ/h)	τ (h)
1200	0.040	0.045	1.12	0.027
1100	0.090	0.027	0.30	0.076
1000	0.165	0.0117	0.071	0.37
920	0.235	0.0049	0.0208	1.40
800	0.370	0.0011	0.0030	9.0
700	...	...	0.00026	81.0

CMOS Fabrication Process 6 Mask Design

1) Mask # 1 P-Well
2) Mask # 2 P^+ source/drain
3) Mask # 3 N^+ source/drain
4) Mask # 4 gate/contact
5) Mask # 5 contact
6) Mask # 6 reverse field



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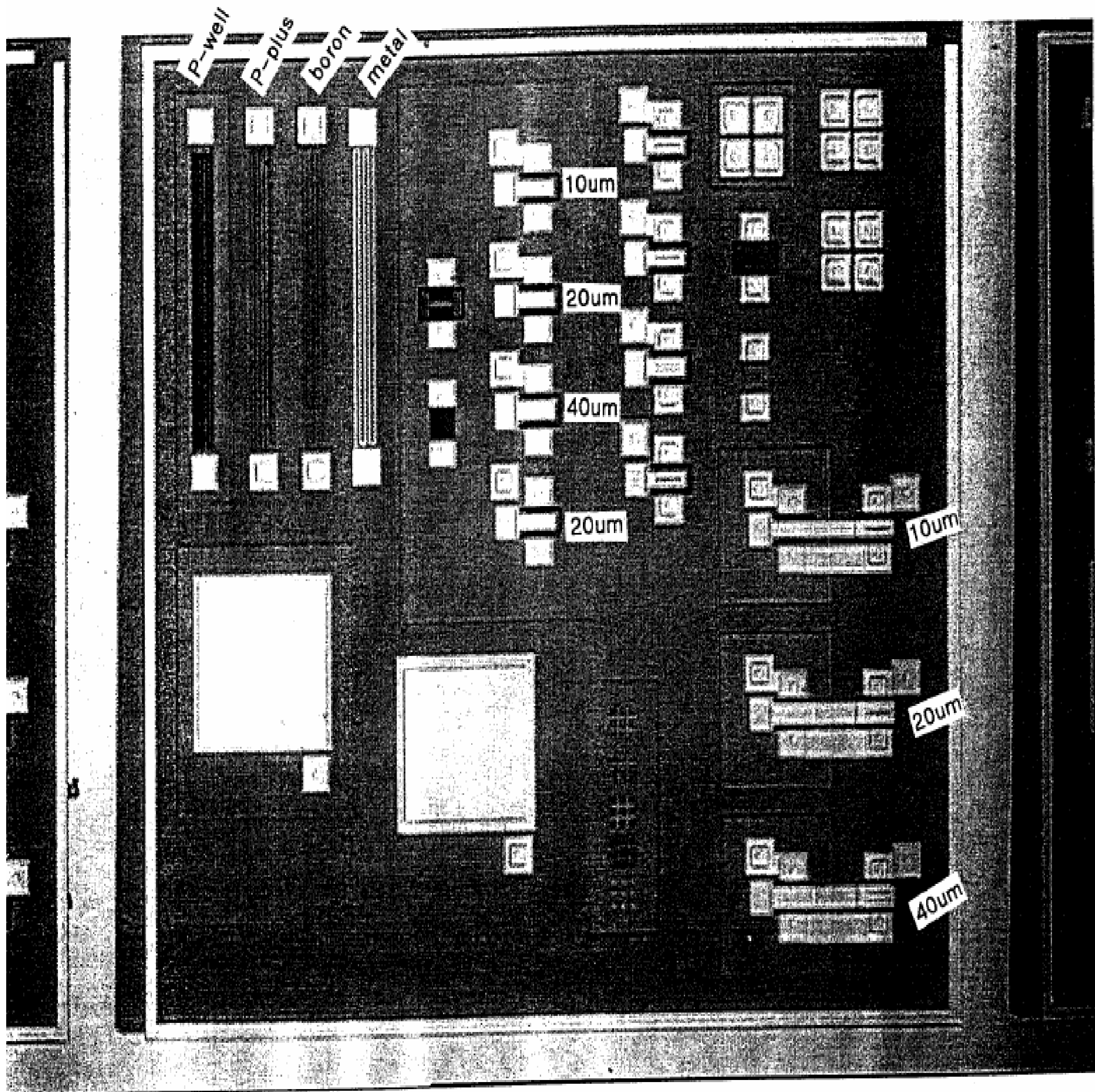
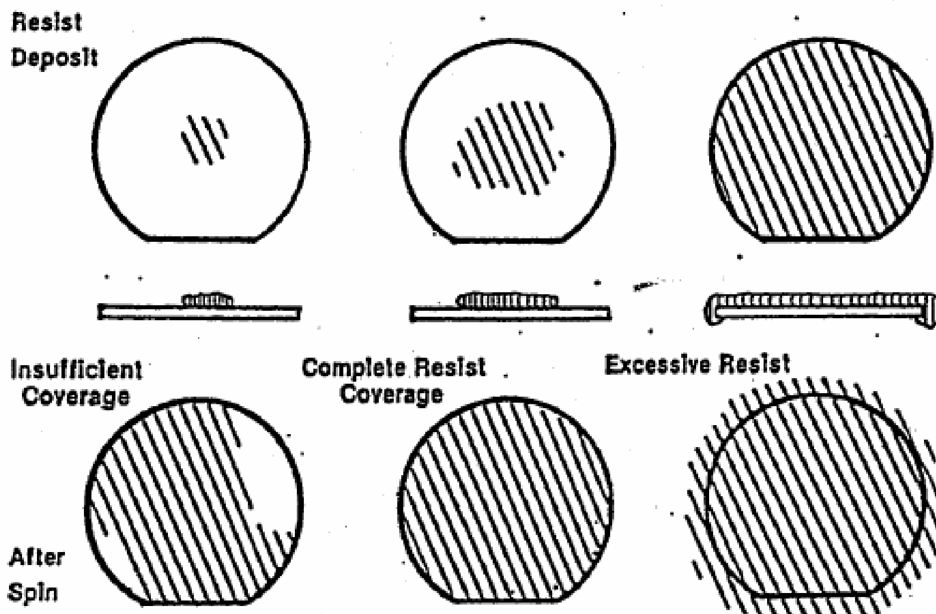


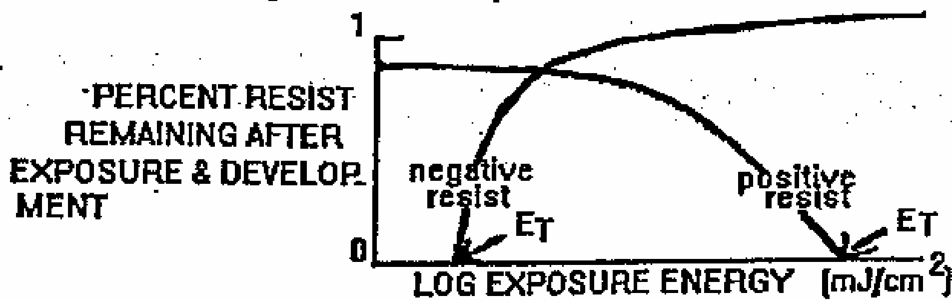
PHOTORESIST THICKNESS:

THE PHOTORESIST THICKNESS IS ACTUALLY DETERMINED BY SEVERAL RESIST-RELATED FACTORS AND TWO SPINNER-RELATED FACTORS. THE PHOTORESIST FACTORS, INCLUDING SURFACE TENSION, SOLIDS CONTENT AND VISCOSITY GOVERN THE DEGREE OF "SPREAD" OF THE RESIST PUDDLE AS THE WAFER IS ACCELERATED TO HIGH SPEED. SURFACE TENSION AND SOLIDS CONTENT ARE CONSTANT FOR A GIVEN RESIST, WHILE THE VISCOSITY IS THE PROCESS VARIABLE. ACCELERATION AND FINAL SPIN SPEED ARE THE TWO SPINNER FACTORS. GENERALLY, THE SPINNER ACCELERATION IS SET AT A CONSTANT, REACHING 5000 RPM IN ABOUT 1.5 SECONDS. PHOTORESIST THICKNESS CAN ALSO BE INFLUENCED BY THE AMOUNT OF PHOTORESIST APPLIED AND THE TIME OF THE SPIN, BUT ONLY IF THESE FACTORS VARY IN THE EXTREME. FORTUNATELY, BOTH OF THESE FACTORS HAVE WIDE RANGES AND ARE NOT NORMAL PROCESS VARIABLES IN DETERMINING RESIST THICKNESS. FOR A GIVEN VISCOSITY, THE FILM THICKNESS WILL DECREASE WITH INCREASING SPIN SPEED. INCREASING THE VISCOSITY FOR THE SAME SPIN SPEED WILL INCREASE THE FILM THICKNESS. THE COMBINATION OF ALL THREE FACTORS RESULTS IN A FAMILY OF CURVES AS ILLUSTRATED;

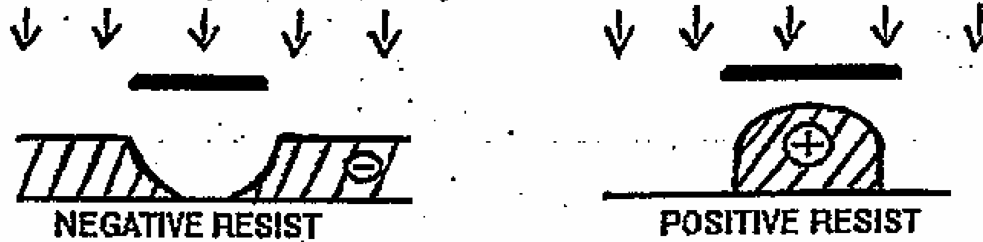


Example of Resist Coverage

(a) Positive & negative resist exposure characteristics



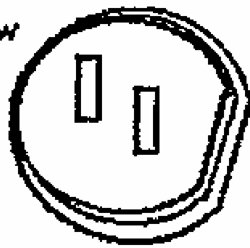
(b) Resist images after development

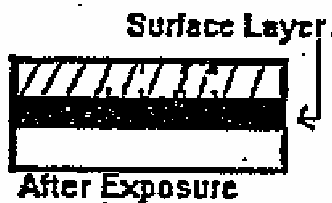


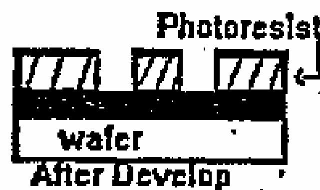
EXPOSURE RADIATION

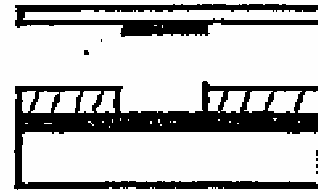
RESIST:

Resists may be either negative or positive. Negative resists becomes less soluble in developer when they are exposed to radiation, and positive resists become more soluble after exposure. The typical negative and positive resist exposure response curves. At low-exposure energies the negative resist remains completely soluble in the developer solution. As the exposure is increased above a threshold energy E_T, more of the resist film remains after development. At exposures two or three times the threshold energy, very little of the resist film is dissolved. For positive resists, the resist solubility in its developer is finite even at zero-exposure energy. The solubility gradually increases until, at some threshold, it becomes completely soluble. Response curves such as these are affected by all the resist-processing variables: initial resist thickness, spectral distribution of the exposure radiation, prebake conditions, developer chemistry, developing time, and so on. These curves can therefore be used to characterize the complete photoresist process. Positive resists usually require more exposure energy (longer exposure times) than negative resists to form resist images. Exposure tool throughput is therefore less when positive resists are used.









Photoresist development Process and Problems;

After the wafer completes the alignment and exposure step, the device or circuit pattern is coded in the photoresist as regions of exposed and unexposed resist. The pattern is "developed" in the resist by the chemical dissolution of the unpolymerized resist regions. Development techniques are designed to leave in the resist layer an exact copy of the pattern that was on the mask or reticle. Problems resulting from a poor developing process are underdevelopment, which leaves the hole incompletely developed to the correct dimensions, or a coved sidewall. In some cases, the development will not be long enough (incomplete) and will leave a layer of resist in the hole. The third problem is overdevelopment, which removes too much resist from the image edge or top surface. Negative and positive resists have different developing characteristics and require different chemicals and processes.

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EXPOSURE, ALIGNMENT, AND DEVELOPMENT PROCEDURE

This procedure outlines the operation of the Karl Suss Mask Aligner. Wafers to be exposed in the aligner should have the resist properly softbaked, to prevent damage to the aligner. *All users MUST have explicit permission to use the aligner.*

SAFETY NOTE:
The aligner uses a mercury arc lamp. Follow proper procedures, to avoid possible explosion and exposure to mercury vapors. Once lamp is on, do not turn off until the end of the day. If it is turned off, it must cool for 30 minutes before restarting.

A. START UP

Note: The aligner may already be on when you come into the lab. If so, proceed directly to part B.

1. Turn on the toggle valve located on the gas control panel. Verify proper flows on gauges, reading 4 bar, 2 bar, and 1 bar from left to right. These values are noted just below each gauge.

2. Flip toggle on bulb power supply ON. Allow power supply to warm up a few minutes.

3. Press button labeled 'start' to start Hg arc lamp. It will take 10 – 15 minutes for the bulb to come up to its final reading of approximately 200 watts.

4. Turn on power to aligner itself by pressing the red button marked 'power' on the aligner panel. Verify that the 'soft contact' and 'ST' lights are lit.

B. LOADING MASK

1. Remove mask holder from location in aligner by loosening thumb screws and sliding out to the left.

2. Place mask pattern (emulsion or chrome) side up on underside of mask frame. Center mask over vacuum groove, aligning it square with the frame.

Hint: The mask is square and can therefore go into the mask holder in any one of four orientations. Always put the mask onto the holder in the same orientation (i.g., words on mask pointing 'north'); this will save you an enormous amount of grief when aligning subsequent masks.

3. Push 'Vacuum Mask' button and verify that the mask is held in place.

4. Turning mask frame over, reload into aligner sliding it all the way to the right. The mask should be underneath, with the pattern side now facing down. Tighten thumbscrews lightly, holding mask frame and mask in place.

5. To view mask, and eventually wafer, the microscope light must be turned on. The control for this light is located on a small box to the left of the aligner. To manipulate the microscope objective as needed, use the handle (joystick) that hangs from the left of the aligner. It has two buttons on it, which when depressed release air brakes that hold the microscope head fixed in position. One releases the x direction, the other the y direction.

C. WAFER LOADING

1. Place wafer on chuck. If the wafer is whole, place it such that primary flat of wafer is pointing in one preferred direction (e.g., to the left). Be consistent; see 'hint' in section B above.

2. Depress the small silver button on the stage, drawing a vacuum on the wafer. Hold button while sliding stage into aligner. Slide it just until it stops; there is no need to force it.

3. On the left side of the aligner there are two levers.

   (a) Separation Lever
   This lower one slides forward and back in a plane parallel to the table. This lever is for bringing the wafer just out of contact with the mask in order to perform any necessary alignment.

   (b) Contact Lever
   The lever on top has a range of motion through 180° in a plane parallel to the side of the aligner. The function of this lever is to bring the wafer chuck up into contact from the lowered position it occupies when first entering aligner.

4. Using the Contact Lever, move it through 180° counterclockwise, raising wafer into contact. Looking through the microscope, shadows should appear, then disappear, as the wafer comes into contact with the mask. This contact should occur with the lever having passed through ¾ of its motion. Any adjustment to this height is made with the variable thickness control on the lower front of the aligner (if such adjustment is necessary, alert your laboratory instructor).

5. If this is the first mask step, and no alignment is necessary, continue with Exposure procedure section E below. Otherwise, continue with Part D.

D. ALIGNMENT

Alignment is probably one of the most difficult jobs that you will do in this lab. It takes a few tries to become 'expert'; don't get discouraged.

1. With the wafer in contact, focus the microscope on the mask and wafer. Use a low power objective.

2. Put the wafer into the separation position, by moving the Separation Lever all the way towards the front of the machine. The contact light will go out.

3. Rotate one of the alignment micrometers to verify freedom of motion of the wafer. This will be difficult if there is no wafer pattern in view. It is possible that the wafer will not move freely due to a spot of resist or some other reason. If this is the case, put it back into contact, then drop wafer out of contact with Contact Lever, slightly lower stage with variable thickness adjustment, and return wafer to contact. Remember to alert your instructor before you use the variable thickness adjustment.

4. To perform alignment, find alignment marks near the center of the mask. Then move microscope, searching wafer underneath for alignment marks. Once found, use the x and y manipulators to bring alignment marks together. Each micrometer has both a course and a fine adjustment. The course (which should primarily be used), is the smaller knot in the middle of each micrometer.

5. Now that alignment marks on both wafer and mask are visible together, adjust Θ as necessary. Do the best you can to align this one set of marks.

6. Move microscope objective to one side of the wafer, releasing it in only the x direction. Observe alignment at this end. Do not expect it to be great. Now:

   a. Move wafer ½ way in to alignment using y manipulator.
   b. Use Θ manipulator to adjust alignment as well as possible in the y direction.
   c. Adjust x manipulator to achieve 'perfect' alignment.

7. Move objective to opposite side of wafer. Again check alignment, and repeat previous sequence of steps.

8. Iterate back and forth until satisfactory alignment is achieved. It may take many iterations, depending on the amount of care taken at each step.

9. Move Separation Lever to its rear position, relighting the contact light.

10. The alignment can now be checked using a higher power objective if desired. If it is unsatisfactory, return to Separation, and twiddle alignment more.

E. EXPOSURE

<u>WARNING!!!</u> During exposure, ultraviolet light floods the wafer surface. Invariable, some light will escape. As ultraviolet light is damaging to your eyes, <u>DO NOT LOOK AT THE LIGHT DURING EXPOSURE</u>

1. Set exposure timer to correct value for your application (in seconds).

2. Verify that bulb power supply is reading approximately 200 W.

3. On bulb power supply, switch to CI by depressing button. The display should now switch to zero, indicating the UV exposure energy at the surface of the wafer.

4. Before exposing, check:

   a. Wafer is in contact, as displayed by light.
   b. Timer is set correctly.

5. Move head away from microscope, and depress EXPOSURE button. The bulb readout should read approximately calibrated mW per square centimeter. While resist is being exposed, DO NOT LOOK AT LIGHT.

6. When exposure is complete, unload the wafer by rotating the Contact Lever 180° clockwise to the front. Slide the transport slide carefully to the right, and remove wafer from the chuck.

F. DEVELOPMENT

Note: Wafer development is to be done in the fume hood.

1. Pour 500 ml of Developer 354 into a first clean beaker.

2. Pour 600 ml of deionized water into a second clean beaker.

3. Place exposed wafer into a wafer holder and agitate lightly in the developer for 30 seconds.

4. Remove from developer and quickly place wafer in deionized water for 30 seconds. Agitate lightly.

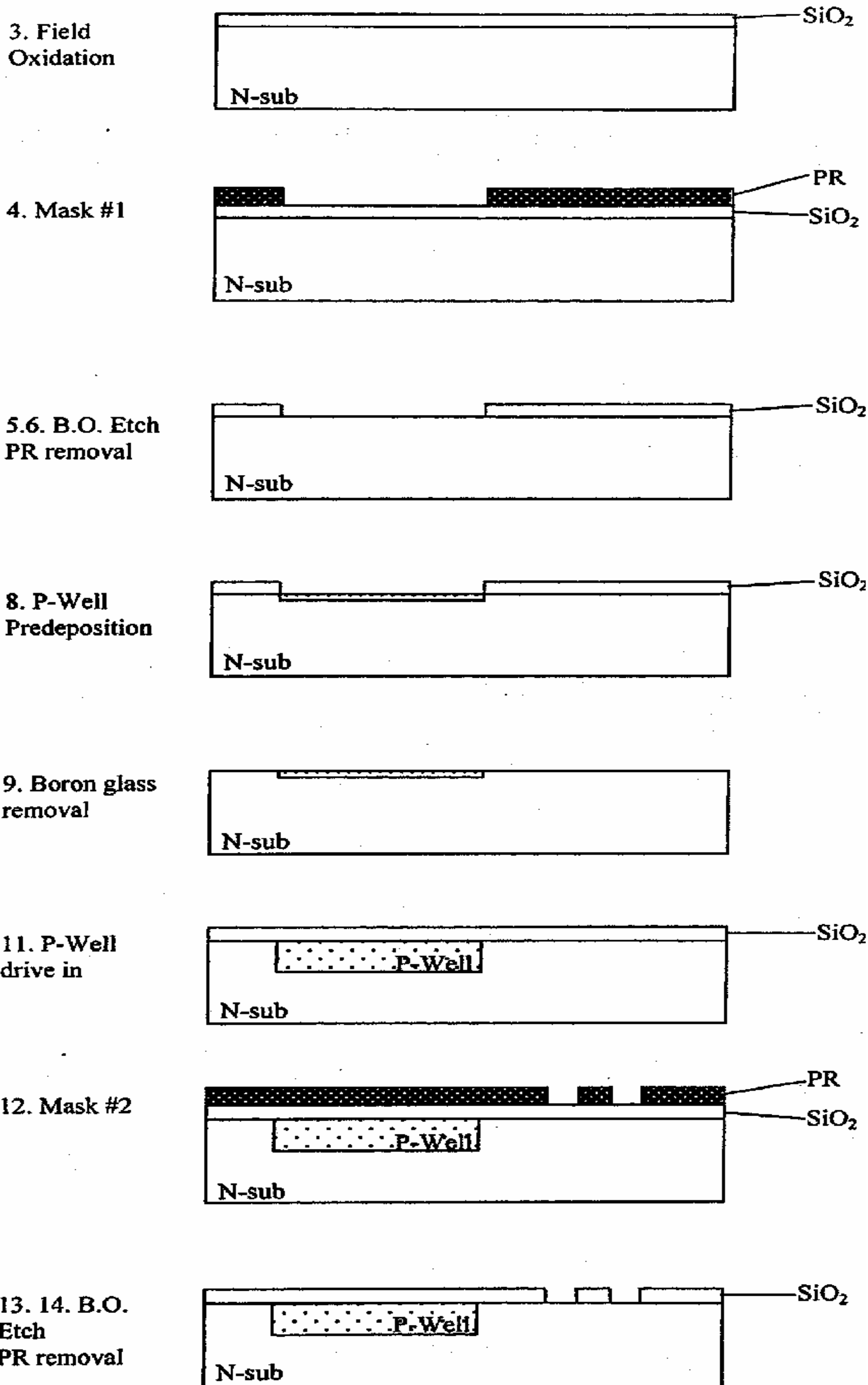
5. Hold wafer over sink and lightly spray with deionized water from the water gun for 30 seconds.

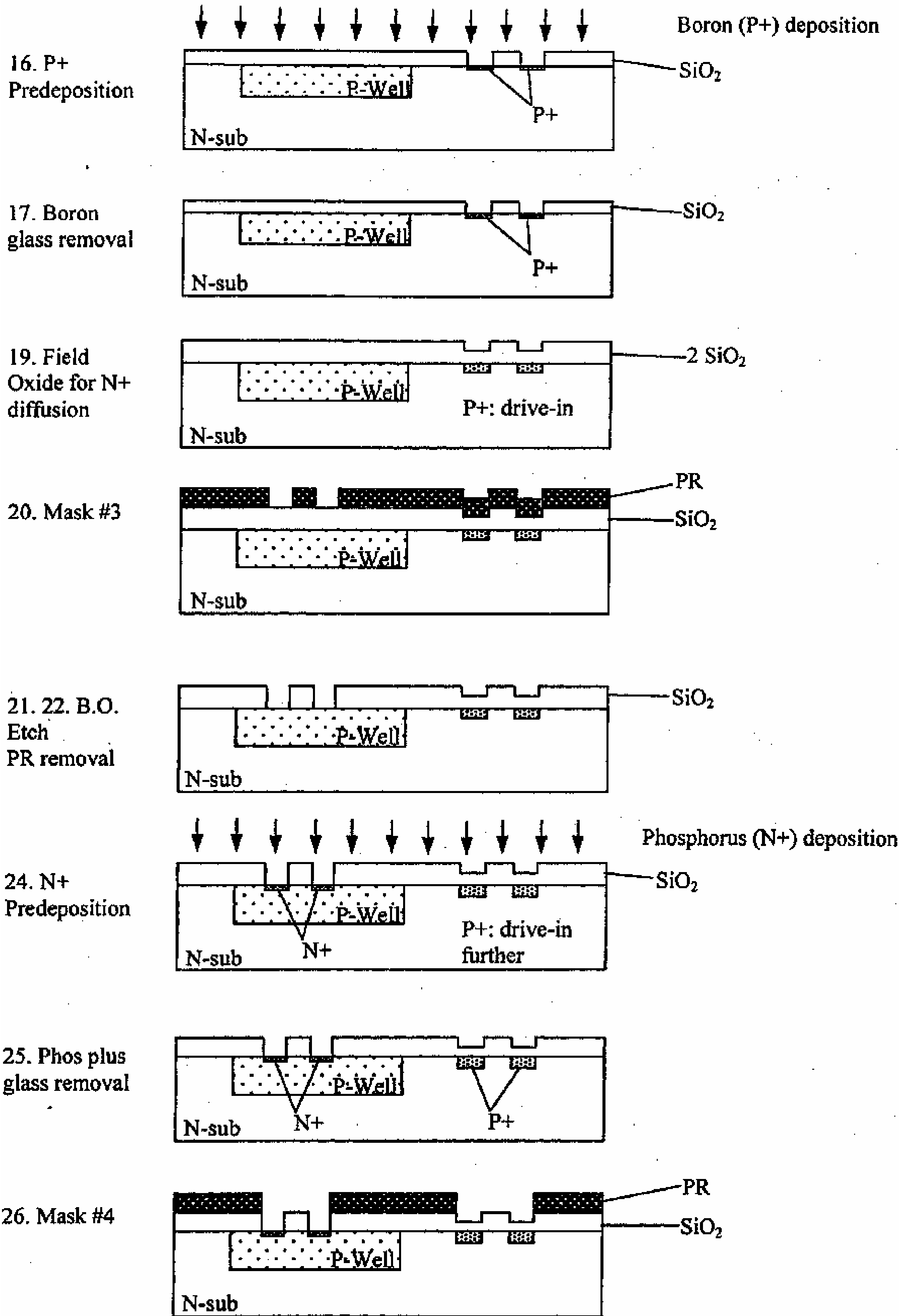
6. Dry wafer using nitrogen gun.

7. Inspect under microscope to determine how successful the photolithographic process has been. If the patterns do not come out, you may have to start all over again (see photoresist application procedure).

8. If patterns are well defined, postbake the wafers for 30 minutes at 120° C.

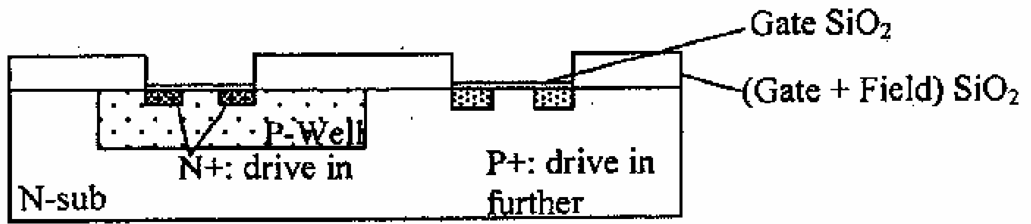
CMOS process cross-section view schematic



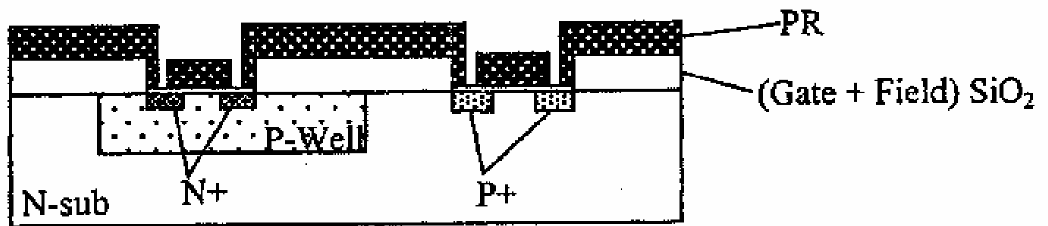

16. P+ Predeposition
Boron (P+) deposition
SiO2
P-Well
P+
N-sub
17. Boron glass removal
SiO2
P-Well
P+
N-sub
19. Field Oxide for N+ diffusion
2 SiO2
P-Well
P+: drive-in
N-sub
20. Mask #3
PR
SiO2
P-Well
N-sub
21. 22. B.O. Etch
PR removal
SiO2
P-Well
N-sub
24. N+ Predeposition
Phosphorus (N+) deposition
SiO2
P-Well
P+: drive-in further
N-sub
N+
25. Phos plus glass removal
P-Well
N-sub
N+
P+
26. Mask #4
PR
SiO2
P-Well
N-sub

27. B.O. Etch
PR removal

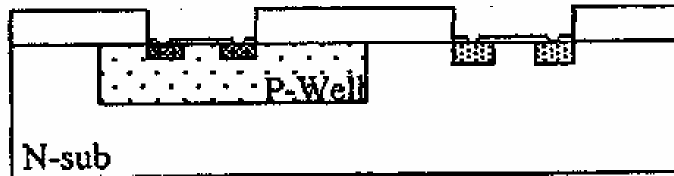
30. Gate
Oxidation



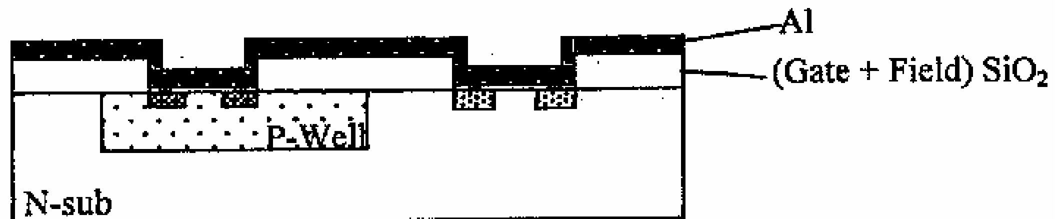
31. Mask #5



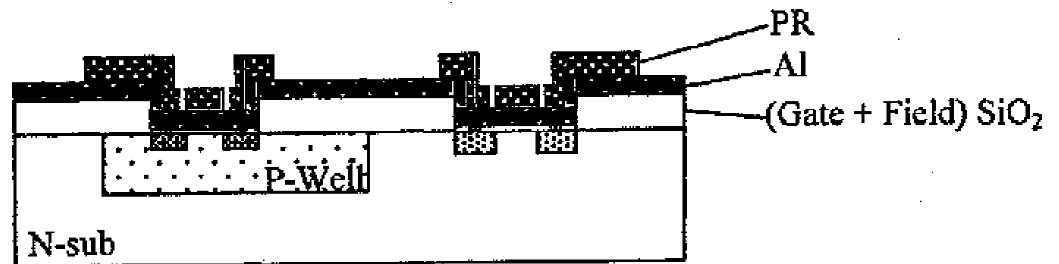
32. 33. B.O.
Etch
PR romoval



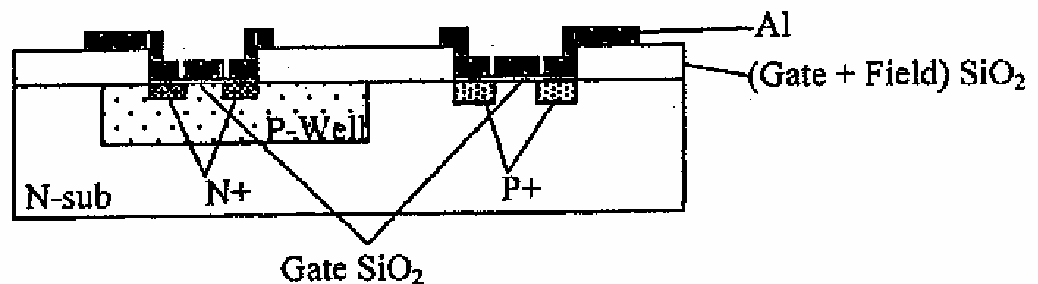
35. Metallization



36. Mask #6



37. B.O. Etch
PR removal
~40.



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BORON DIFFUSION PROCEDURE:

This lab introduces the solid-source method for dopant diffusion. In this case, a Boron (p-type) diffusion will dope the source / drain regions which are defined by gaps in the field oxide. Methods for evaluation of the diffused layer will be performed later. The boron source is a ceramic wafer of boron nitride (BN), which has been oxidized in a 1000° C 25% 0_2 atmosphere resulting in a surface layer of B203 glass.

During this infinite – source or pre-deposition step, this glass slowly evaporates from the BN wafer and condenses on the silicon wafer. This thin layer of B203 provides elemental boron for diffusion into the silicon via the reaction:

$$2\,B203 + Si \rightarrow 4\,B + 3\,Si0_2$$

After the desired amount of boron is deposited on the silicon wafer, the BN source wafers are removed the boron is diffused into the silicon wafer during a high temperature drive-in step. In our process, the drive-in will occur during the subsequent GATE OXIDATION STEP.

1. RCA Clean device and control wafers (refer to RCA clean handout). Check that the boron diffusion tube is idling at 600° C with nitrogen flowing through the tube. Before or during the clean, the instructor will prepare source wafers as necessary suing the following procedure.

    Oxidize BN wafers at 900° C in 25% 0_2 for approximately six hours. This is not necessary for every use, as the source are compromised if oxidized too frequently.

    After oxidation, the BN wafers need to be stabilized in N2 in the furnace for at least 30 minutes. The source wafers should then be stored at the mouth of furnace tube, to avoid hydration.

2. At completion of RCA clean, load wafers into boat with sources. The wafers should be inserted such that the device side of each is facing a BN source wafer. There are two wafer slots between sources, allowing for a device wafer facing out to both sides.

3. Load the boat into the mouth of the furnace for the pre-deposition diffusion

4. Check that the gas system is in the IDLE CONFIGURATION:

    >> Oxide Furnace valve is facing N_2

    Note that in the idle configuration, nitrogen gas is flowing through all three furnaces.

5. Turn the furnace controller up to the deposition temperature of 935° C. Wait until the temperature has stabilized (about 10 – 15 minutes)

6. Begin appropriate nitrogen flow through the tube.

   >> Adjust the flow rate to 87.11 sccm (1000 / standard cubic centimeter per min).

7. Wafers should be loaded in the wafer boat, between each solid source of boron and placed in the mouth of the furnace tube.

8. Push the wafers into the center of the tube at a continues movement until you reach center zone using the pushrod.

9. When 30 minutes have elapsed, boron deposition is completed.

10. Using pushrod return wafers back to the mouth of the furnace using the same procedure as in step 8.

11. Turn the temperature controller down to 600° C.

12. Allow the wafers to cool down in the mouth of the tube for a least 5 minutes before removing

13. Remove the boat from the furnace and allow the wafers to continue to cool before removing them from the wafer carrier.

14. The wafers are now covered with borosilicate glass, which served to dope the exposed source / drain regions and the polysilicon. Other areas of the wafer surface were masked from diffusion by the field oxide.

15. When wafers are cool, place them in the RCA wafer carrier and dip them back into the HF bath for 15 seconds and rinse for 2 minutes. This is to remove outer boron film from surface that is no longer needed.

NOTE: The sheet resistance will increase when the Boron is removed from the surface because the boron doping tends to increase conductivity (and therefore reduce resistivity). When this boron is removed, the conductivity decreases and the resistivity (as well as sheet resistance) goes up.

PHOS PLUS

High Purity Planar Dopant Sources

PhosPlus Planar Dopant Sources Have Widespread Uses.

PhosPlus planar diffusion sources represent a significant advancement in the field of phosphorus dopant materials. Their ability to easily and uniformly dope large-diameter silicon wafers in a safe manner accounts for their increasing popularity in the semiconductor industry. In general, PhosPlus sources offer all the advantages traditionally associated with planar sources plus they possess a number of additional improvements which make them the most desired phosphorus source available to the diffusion engineer.

Three PhosPlus Sources Provide Versatility.

Three PhosPlus sources are available to meet the many silicon processing requirements of the semiconductor industry. The following temperature ranges are normally recommended for their use:

Source Type	Recommended Temperature Range	Approximate Sheet Resistivity
TP-470	975-1150°C	<1-7 ohm/sq
*TP-360	900-1025°C	5-25 ohm/sq
TP-250	800-925°C	5-100 ohm/sq

*** The TP360 PhosPlus source has been discontinued as of Jan 1, 1997.**

Each type of PhosPlus source contains P_2O_5 and the extremely stable oxides of Ta_2O_5, Al_2O_3 and/or Ln_2O_3(rare earth oxide). The sources are manufactured in such a way that the P_2O_5 is combined with Al_2O_3 or Ln_2O_3, and it only evolves when the sources are heated to the doping temperatures through one of the following decomposition reactions:

TP-360 and TP-470

$Al(PO_3)_3 \dashrightarrow AlPO_4 + P_2O_5 \uparrow$

TP-250

$LnP_5O_{14} \dashrightarrow LnP_3O_9 + P_2O_5 \uparrow$

Several thin radial slots are cut into the sources to ensure that they will not fracture when rapidly heated in the diffusion furnace. The slots have no effect on the uniformity of the doped silicon wafer. The TP-360 and TP-470 sources also contain Ta_2O_5 to adjust their thermal expansion coefficients and make them extremely resistant to thermal shock.

Are Safe to Use.

PHOS PLUS

High Purity Planar Dopant Sources

PhosPlus Sources Show Long Lifetimes.

Industrial experience has shown that PhosPlus sources normally exhibit lifetimes in the range of 300-500 use hours. The actual lifetimes of PhosPlus sources used in typical plant production, however, depend upon many factors, such as temperature of use, care in handling, device being manufactured, the sensitivity of the process to the eventual decrease in the P_2O_5 evolution rate, etc.

The potential lifetime of a PhosPlus source can be estimated by periodically doping a silicon wafer with the source being held in diffusion furnace and observing how the resulting sheet resistivity varies with time. Figure 1 shows the average sheet resistivity obtained on the silicon wafers doped for 60 minutes at 1020°C with TP-470 sources when used in a typical production environment. Little change in sheet resistivity was observed for the first 600 hours of use. The sheet resistivity then began to slowly increase as the P_2O_5 evolution rates was gradually decreasing.

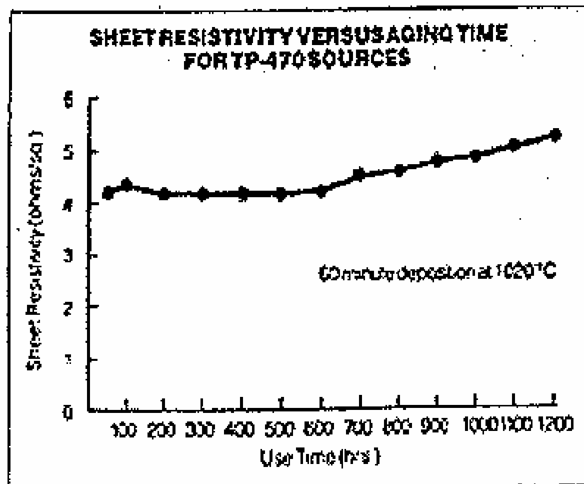


Figure 1

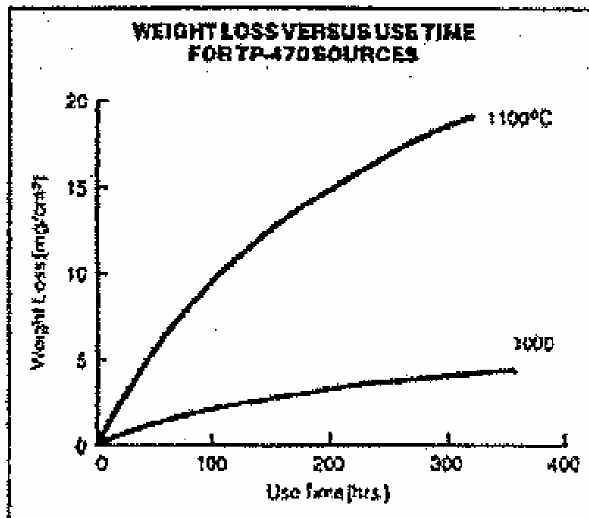


Figure 2

A second method of estimating the lifetime of a source is to measure the amount of weight a source loses at a use temperature as the P_2O_5 evolves. Weight loss data for the TP-470 sources (Figure 2) indicates a continuing process of P_2O_5 evolution over hundreds of use hours.

Figures 3 and 4 show similar sheet resistivity and weight loss date for the TP-250 sources. This data also indicates that hundreds of hours of use can be obtained from a set of TP-250 PhosPlus sources.

PHOS PLUS

High Purity Planar Dopant Sources

Doping Properties of PhosPlus Sources.

Single Crystal Silicon: Typical sheet resistivity versus deposition time curves for the three PhosPlus sources are plotted in Figures 5,6 and 7. The curves are different for each source because the sheet resistivity of the silicon wafer for a given deposition cycle depends somewhat upon the thickness of the deposited glassy film. The thicker the glassy film, the lower the sheet resistivity. Figure 8 shows how the deposited film thickness varies with the type of source being used.

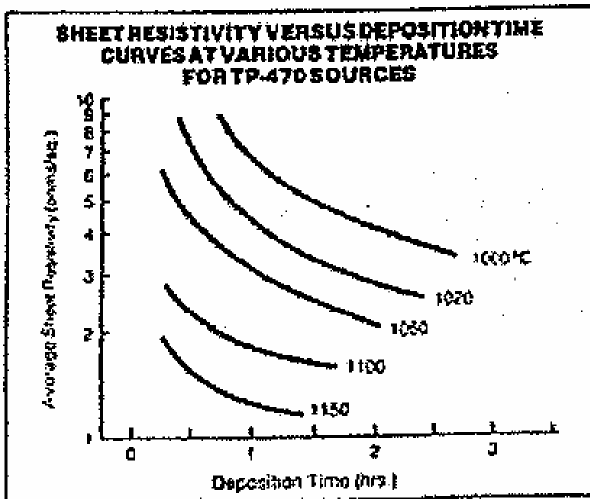


Figure 5

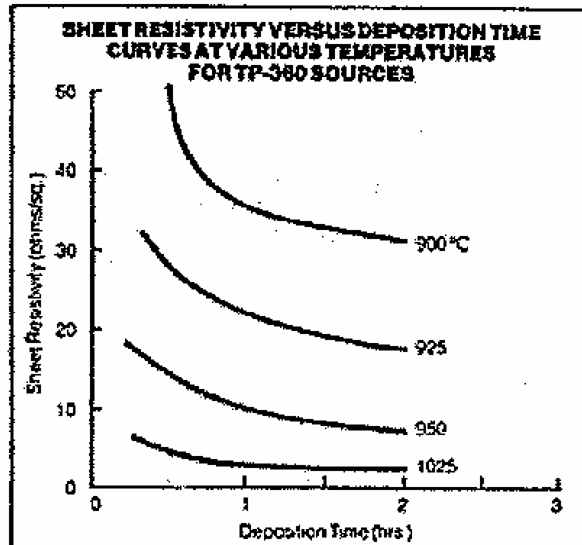


Figure 6

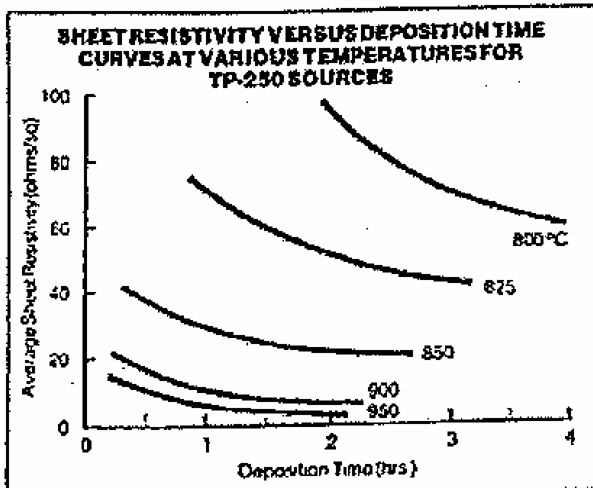
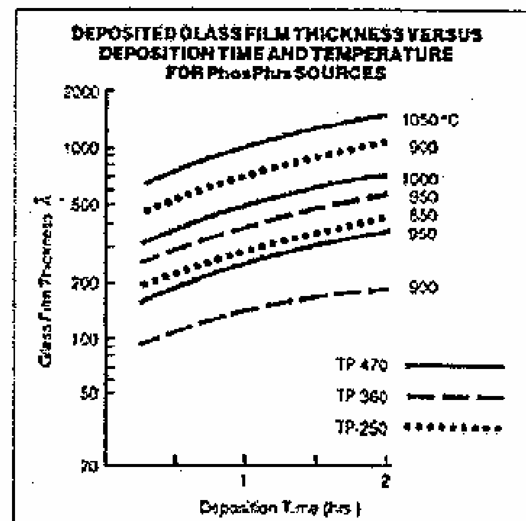


Figure 7



A typical deposition time for a solid-source diffusion system is about 45 minutes. This time is usually long enough for the sources to uniformly dope the silicon wafers. At the same time, it is short enough to be compatible with most semiconductor process parameters. Figure 9 shows the sheet resistivity and junction depth that is obtained from a 45-minute deposition with the TP-470 PhosPlus sources at various deposition temperatures.

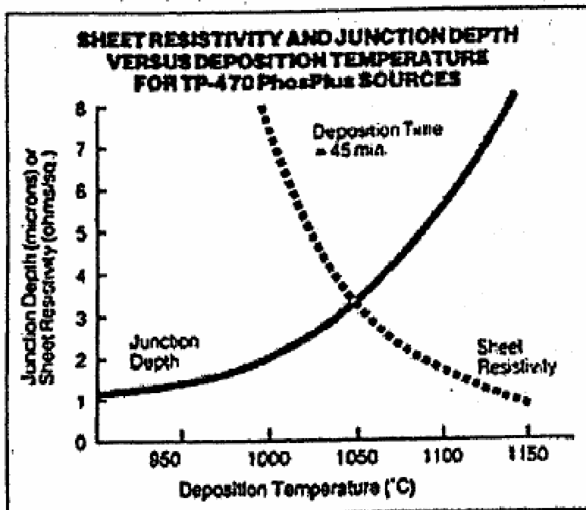


Figure 9

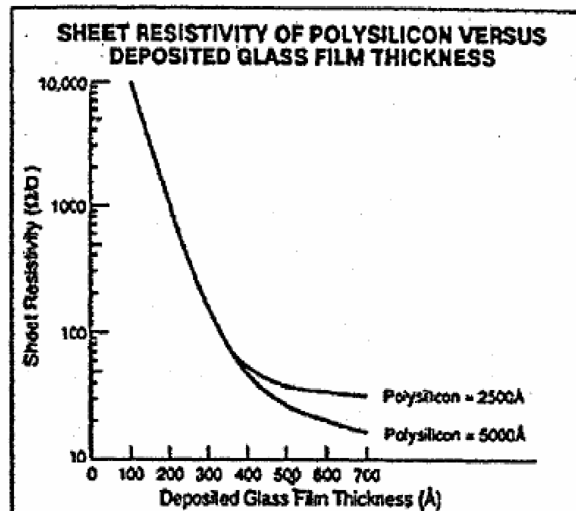


Figure 10

Polysilicon: The minimum sheet resistivity that can be obtained from polysilicon wafers that are saturated with phosphorus partially depends upon the thickness of the polysilicon layer. These sheet resistivities are about 12ohm/sq for 5000A of polysilicon and about 32ohm/sq for 2500A, and they occur when the deposited phosphorus glassy film exceeds about 500 to 600A.

Glassy films that are less than 500A can also be uniformly deposited on the polysilicon wafers from the PhosPlus sources to produce higher sheet resistivities for special applications. Figure 10 can be used as a guide to determine the approximate thickness that is required for different sheet resistivities.

Sheet resistivities at or above the saturation of phosphorus in polysilicon can be obtained from any of the three phosphorus sources. The appropriate deposition cycle can be selected from the curves shown in Figures 11, 12 and 13.

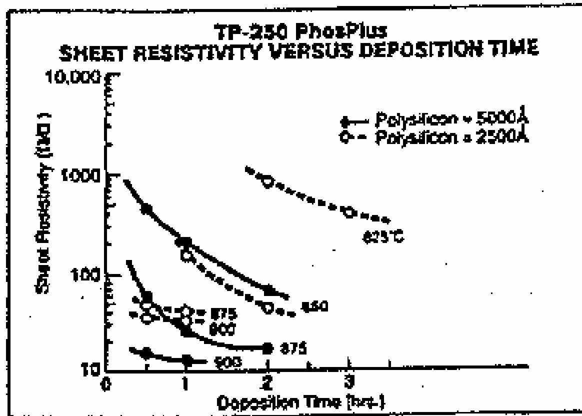


Figure 11

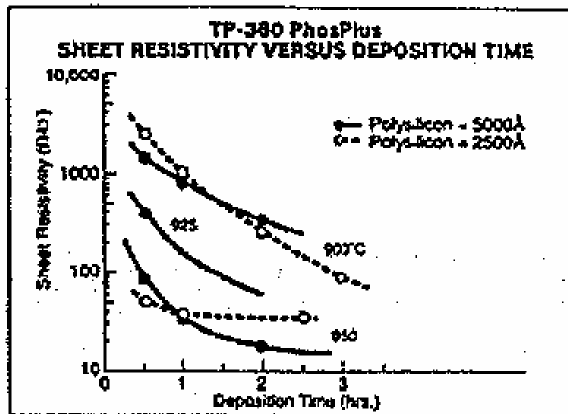


Figure 12

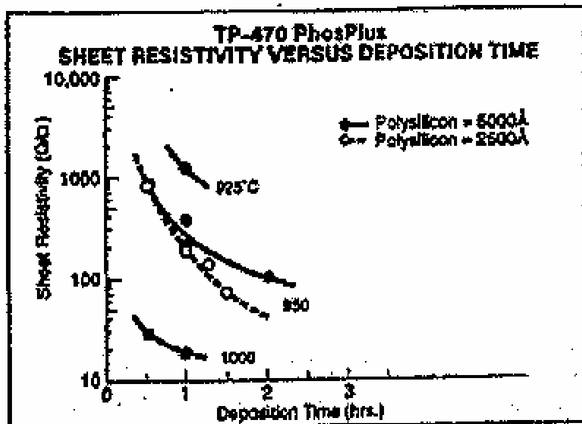


Figure 13

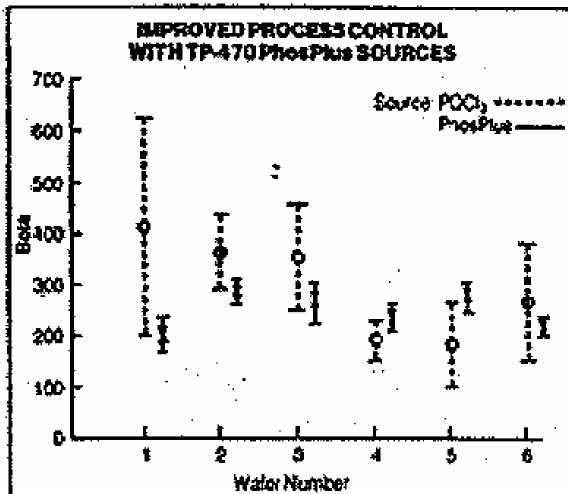


Figure 14

Uniformities: When the various processing conditions are optimized, uniformities of 2% across the silicon, 3% across the boat and 4% run-to-run or better can generally be obtained on single-crystal silicon. A total variation of about 3% can be achieved on high-quality polysilicon wafers doped to their minimum sheet resistivities (saturation with phosphorus).

These uniformities are quite typical of the planar diffusion system and tend to be independent of the diameter of the wafer and the number of silicon wafers being processed during a run. This independence can result in an increase in silicon throughput compared to the number of silicon wafers often processed in gas system. It can also significantly increase production yields by improving process control as demonstrated by the decrease in beta variation when TP-470 PhosPlus sources are used for an emitter diffusion instead of POCl3 (Figure 14).

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DRY OXIDATION PROCEDURE: (GATE REGION)

This process step will thermally oxidize the silicon substrate. The oxide grown will be a thin gate oxide, approximately 1000A.

1. RCA clean device wafers and control wafer. Refer to RCA Clean Handout for procedure in substrate cleaning station. During the cleaning, continue with the next three items, preparing the oxidation furnace.

2. Verify that the gases flowing through the furnaces are in the IDLE CONFIGURATION:

   Note that in the idle configuration, nitrogen gas is flowing through all four furnaces.

3. Ramp oxidation furnace and set it to 900° C. This is accomplished by adjusting the furnace controller in the side of the furnaces.

4. At the completion of the RCA clean, remove the quartz boat from the furnace using the appropriate push rod and quartz boat loader. Always wear poly gloves and / or high temperature gloves when handling quartz ware. DO NOT hold push rod in front of mark on rod. Keep the boat in the boat loader and set the boat loader down in front of the furnace tubes, taking care that holder and boat remain in laminar flow.

5. Place the RCA – clean wafers, still in their carrier, into the carrier box, and transport them to the furnace loading station. Load wafers into quartz boat using Teflon or Teflon-tipped tweezers. Avoid passing arms or head over clean wafers.

6. With boat loader, return wafers on boat to the mouth of the oxidation furnace. Slowly push boat into the mouth of the furnace with push rod, to avoid wafer fracturing due to thermal stress.

   Note during this procedure there is no stopping point until wafers have been loaded in the mouth of the furnace.

   The dry oxidation process is to be carried out at 1100° C. The procedure is:

   a. Load in N_2 (idle gas)
   b. Dry O_2 45 minutes
   c. Unload in N_2 (idle gas)

7. Ramp the furnace controller up to the oxidation temperature of 1100° C. Wait until the temperature has stabilized, (ramp mode is set at 20° / per min.)

8. Begin dry oxygen flow through the tube:

   >> turn oxide furnace valve to O_2
   >> valve to Dry or Wet should be facing Dry

   Dry oxygen is now flowing through the tube. ADJUST the flow rate to 94.7sccm (which is equivalent to 1000 sccm flow), set time for 45 minutes.

9. When 45 minutes have elapsed, turn oxide furnace valve to N_2. The gas delivery system is back to IDLE CONFIGURATION

10. Return furnace setting to 900° C, lock in ramp mode and wait to cool down.

11. Pull wafer boat slowly to the mouth of the furnace with push rod. Let wafers cool briefly before completely removing boat from furnace. Make sure that the wafers stay in laminar flow hood at all times.

12. Allow wafers to cool completely in boat before removing and storing in N_2 dry box.

13. With boat loader, return boat to oxidation furnace. Slowly push boat into furnace with push rod, approximately ¼ of the way into the furnace tube. Loosely replace end cap and store boat holder inside the metal furnace door.

14. Estimate the thickness of the grown oxide using the color chart as well as well as your calculation of approximately how thick the grown oxide should be.

15. Measure grown oxide thickness of control wafer using Ellipsometer, referring to Ellipsometer procedure (this may be deferred to later lab for time reasons).

METAL FILM DEPOSITION WORKSEET

DATE: ________________, WAFER #: ________________,

Film Material : ________________,

(Single Run)

Distance between Source / Wafer: ____________,

Deposition rate: ____________,

Monitor reading: ______________,

Tencor reading: ______________,

Notes / Comments;

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INTRODUCTION TO METALLIZATION

Semiconductor device structures require a number of different layers or films. These layers can be dielectrics, semiconductors or conductors and are placed on the wafer by a variety of techniques. During the past several years there has been a dramatic increase in the uses and number of these layers.

Deposited conductors are an integral part of every device, in the role of surface wiring. Conductors also provide other functions in I.C. structures, such as fuses and back side electrical contact for the packaged die. *Metallization* is the general term used to describe this segment of semiconductor processing.

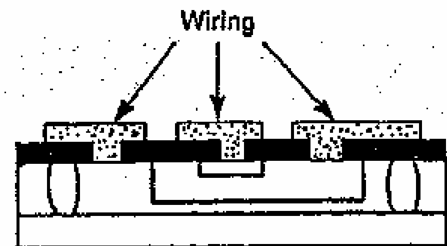
Conductors:

Metal films are used in semiconductor technology to wire together the various components formed in the wafer surface. The wiring is accomplished by the deposit of a thin (10 to 15 thousand angstroms) layer of metal on the wafer. This metal layer, after being patterned through a photomasking process, connects the devices as required by the circuit operation. The metal strips on the wafer surface are called *leads* or *interconnects*. Generally, a wafer heating step called *alloy* follows deposition to insure good electrical contact between the metal and the wafer surface.

Patterned conductive films serve two other roles in device structures. They function as the gate electrodes in MOS structures, and are used as electrodes in thin film capacitors.

The following metals and alloys are used for these purposes:

1. Aluminum
2. Aluminum Alloys
3. Titanium/Tungsten
4. Doped Polysilicon
5. Refractory Metals and their Silicides
6. Gold



Thin Film Wiring

Aluminum and Aluminum Alloys:

Aluminum has been the traditional "wiring" metal. In fact the development of thin film aluminum technology has been one of the major contributions to planar technology. Aluminum achieved this status because it meets the requirements that a metal must have to be compatible with silicon technology.

1. Good Current carrying Density
2. Superior Adhesion to SiO_2
3. Ease of Patterning
4. High Purity
5. Good Electrical contact with Silicon

Aluminum meets all of the above requirements. It has good conductivity, adheres very well to silicon dioxide, can be patterned with conventional photomasking techniques and is obtainable in high purity. Aluminum has to be purified to between 99.9999 and 99.99999% for semiconductor use. Electrical contact of aluminum with silicon, while adequate for LSI level technology has reached its limits in the VLSI era.

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DEPOSITION METHODS:

Metallization techniques, like the other fab processes, have undergone improvement and evolution in response to the demands of the new circuits. The mainstay of metal deposition techniques was and is *vacuum evaporation*. Aluminum, gold and the fuse metals are deposited by evaporation. The newer metal systems as well as the dielectrics and semiconductors can be deposited by sputtering. This technique offers superior film composition and thickness control and will become the dominant deposition method by the end of the century.

The two systems are similar in construction and operation. Each a source of the material to be deposited, a method to convert the source to atoms and / or molecules, wafer holders to insure even film deposition, an evacuated chamber and a pumping system to remove the air.

Evaporation Theory:

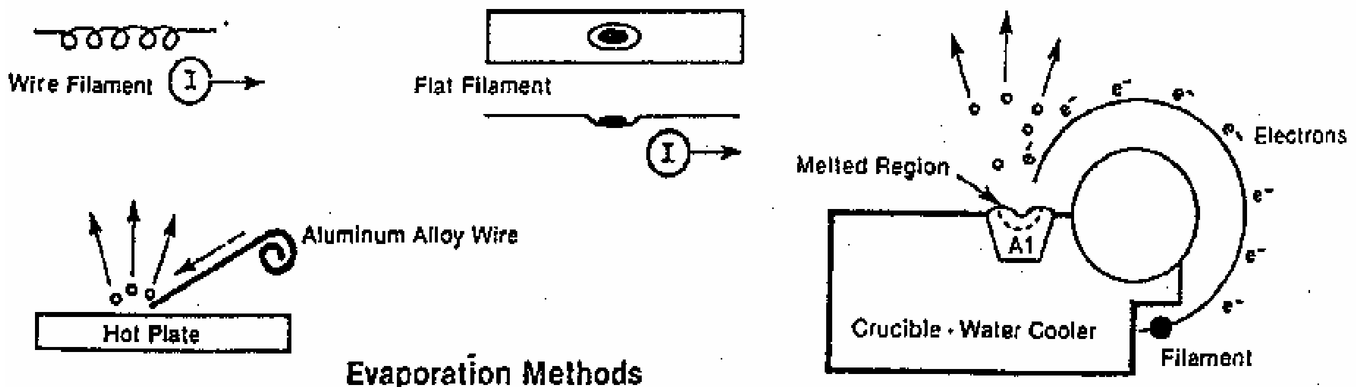
The evaporation of metal onto wafers relies on the same process by which water will evaporate out of a glass. At the liquid air interface some of the water atoms have enough internal energy to break the surface and escape into the air. Over time, enough atoms will escape from the water and remain in the air, reducing the volume of the water. This same evaporation process can be made to occur in a solid. When the temperature is raised high enough, atoms of the solid material will melt and "evaporate" into the atmosphere.

Three methods are used to provide the external energy needed to evaporate aluminum and the other metals. They are:

1. Filament
2. E-beam
3. Flash

Filament:

The filament technique is used primarily for gold and nichrome evaporation. An electrical current is passed through a tungsten filament of wire or pan design. The metal to be evaporated is wound on the wire or placed in the pan and is raised to the evaporation temperature by the current flowing through the filament. Atoms from the source material are "evaporated" into the atmosphere. In alloys, such as nichrome, each of the elements in the alloy will evaporate at a different rate. Each rate is characteristic of the evaporation rate of the element at the particular temperature of the filament. In the case of nichrome, the composition of the nickel and chromium on the wafer will differ from the composition in the source alloy.



Evaporation Methods

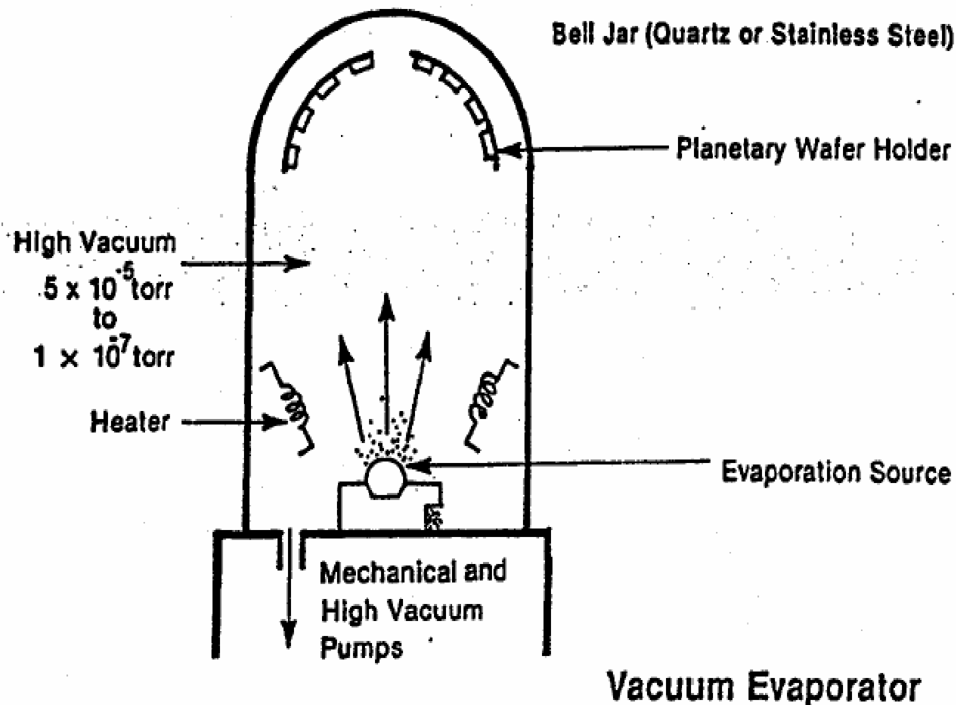
Flash System:

This method is used primarily to evaporate aluminum / silicon alloys. The source is a wire of the alloy. A mechanical feeder automatically pushes the wire onto a hot plate. Upon contact the end of the wire very quickly evaporates or "flashes" into the gas state. Since all of the elements in the wire are evaporated instantaneously the composition of the film on the wafer is very close to the source composition.

Evaporation Chamber:

The evaporation must take place in an evacuated chamber. If the evaporation took place in air, the high energy aluminum would combine with the oxygen in the air to form Al_2O_3, an insulator. The chamber itself is made of heavy wall quartz or stainless steel to withstand the low pressures that are ($5X10^{-5}$ torr, or 0.00005 mm Hg).

Chamber design is either the familiar bell jar or the refrigerator style configuration. Bell jars have the advantage of maximum strength and good vacuum sealing from the bottom circular gasket, but the disadvantage of slower productivity due to the time required to raise and lower the jar. The front opening styles have the opposite advantages and disadvantages.



Vacuum Evaporator

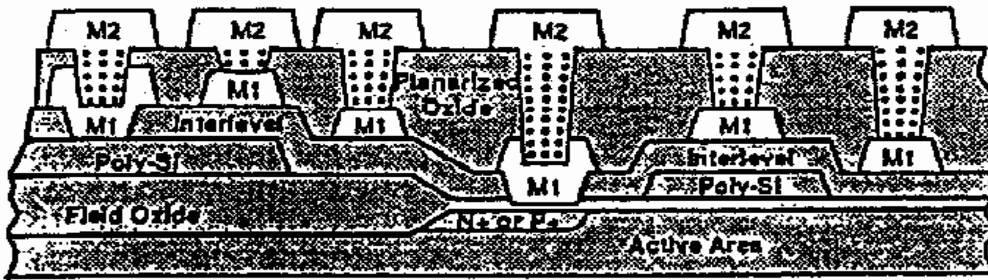


Figure 13.2 Cross section of typical planarized two-level metal VLSI structure showing range of via depths after planarization. (*Courtesy of Solid State Technology.*)

Next comes a layer of some dielectric material, called an intermetallic dielectric. This dielectric may be a deposited oxide, silicon nitride, or a polyimide film. This layer receives a masking step that etches contact holes, called *vias*, down to the first-level metal. The whole process is repeated, with the final structure having two or three levels of metal connected to each other and protected by a final passivation layer. In some schemes the via holes are filled with metals other than the main conducting material. The particular metals for via filling are discussed in the following pages.

A multilevel metal system is more costly, of lower yield, and requires greater attention to planarization of the wafer surface and intermediate layers to create good current-carrying leads.

In the role of surface conductor, a metal must meet the following criteria:

- Good electrical current-carrying capability (current density)
- Good adhesion to the top surface of the wafer (usually SiO_2)
- Ease of patterning
- Good electrical contact with the wafer material
- High purity
- Corrosion resistance
- Long-term stability
- Capable of deposition in uniform void- and hillock-free films

Fuses

The development of thin-film fuse technology allowed creation of the programmable read-only memory (PROM) circuit. The fuse allows field programming of data in the memory section of the chip. In this role the fuse is not a protective device, as in most electrical circuits, but is included specifically to be "blown" or disabled.

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PAN ETCH PROCEDURE:

Pan Etch Consist the Following Parts by Volume: (Add Acid to Water)

H20 -- 2 Parts
Phosphoric -- 16 Parts
Acetic -- 1 Parts
Nitric -- 1 Part

This Should Be Handled with Safety in Mind:

1. Pour a generous amount of Pan Etch in a petri dish
2. Heat solution to 40° C to 45° C
3. Carefully immerse wafer aluminum side up with tweezers
4. Begin to gently rotate wafer in solution to prevent bubbles from forming on top surface of wafer

NOTE: Bubbles may prevent the etch from removing the aluminum

5. Aluminum should begin to react immediately and remove all the exposed aluminum depending on the thickness of the deposition.
6. When the aluminum is etched, carefully remove the wafer and place in petri dish filled with DI water.
7. Load wafer in wafer carrier and continue to rinse for several minutes both front and back

NOTE: Pan Etch tend to leave a clear residue

8. Dry with N_2 gun
9. Inspect under microscope for clear, clean, patterns

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TECHNICS PLASMA ETCHING PROCEDURE:

NOTE: The instructor will see that the following steps have been checked

1. Vacuum pump is ON
2. Oxygen tank in ON
3. Main Power to Technics Machine is ON

AUTOMATIC OPERATION PROCEDURE

1. Lift chamber lid up
2. Load the wafer to be treated
3. Carefully bring down the chamber lid
4. Push to Start / Stop button. This will start the Systems Automatic Sequence

THE SEQUENCE WILL BEGIN BY

1. Pumping the chamber down to the low setpoint
2. Once the low setpoint has been reached Gas #1
   Will turn on the Flow Controller
3. After a time delay of approximately 30 seconds the sequence will begin
4. When the timer reaches 00.0 minutes the RF power and the gases will turn OFF. The chamber will pump down and the system will give off and audible alarm
5. With the chamber vented, lift chamber lid up and remove your wafer
6. Turn OFF Vent Valve

mTorr Pressure: ______________________

Watt Power: ______________________

Time: ______________________

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SINTER / ANNEAL PROCEDURE:

Verify that the Gas Flowing through the Sinter / Anneal furnace is N_2

Note: That in the Idle Configuration the gas valve is turned facing the N_2
Gas flow regulator should be set at 87.11 sccm (approximately 1000 sccm)

1. Set temperature to furnace controller marked sintering / anneal at 400° C.
2. Remove quartz boat from mouth of furnace using sinter push rod.
3. Carefully slide boat onto boat carrier and place on table under laminar hood.
4. Load wafers to be sintered on wafer carrier
5. Slide mounted wafers carefully into mouth of furnace.
6. Wait a few seconds for wafer to adjust to furnace temp.
7. Slide boat using quartz rod up to marked line flushed with metal doorway, this will place wafer carrier to center of furnace.
8. Set timer to 30 MINUTES.
9. When time has expired slide quartz boat back to mouth of furnace.
10. Wait for the wafers to cool, approximately 5 minutes, remove and unload wafers.

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LABORATORY MEASUREMENT

NOTE: YOU NEED TO TEST ALL TRANSISTORS OF DIFFERENT GATE DEMINSION TO COMPLETE YOUR EVALUATION

These laboratory handout details the measurements you need to take on your fabricated wafers. You will be measuring various types of devices on your wafers; the metal resistor, the diffused resistors, several N and P MOSFETS, and an inverter. Note that some of these laboratory steps do not need to be done in front of the curve tracer, and you will save time by doing them before or after the actual laboratory period.

In several of the measurement steps, the probe station will be used. Your instructor will show you how this probe station is to be operated.

NOTE: Complete and submit 4 total tested transistors, one of each gate dimension from P-MOS and N-MOS devices. Complete and submit data on 1 working Inverter; noting the gate dimension used. This is a total of (8) transistors and 1 Inverter. In addition, complete and submit data on a metal resistor, a born resistor, a P+ resistor, and a P-well resistor.

1. METAL RESISTOR MEASUREMENT

Note that only step (B) must be performed on the curve tracer.

- **A.** **Calculate the number of squares in the metal resistor. Neglect the resistance of the pads.**
- **B.** **Measure the resistance of five different metal resistors on your wafer. Note that each resistor has nominally the same geometry.**
- **C.** **Calculate the sheet resistivity of the aluminum in ohms per square. Also, quantitatively calculate the uniformity of the sheet resistance Based on your measurements in part B.**
- **D.** **Calculate the resistivity of the aluminum in ohm-cm. (Note that you Have to measure the aluminum thickness to get this number. Your Instructor will help you do this). How does your value compare to The resistivity of bulk aluminum (available in CRC handbook and / or at the library).**

2. DIFFUSED RESISTOR MEASUREMENT

Note that only step (B) must be performed on the curve tracer. This process should be repeated for the P+ resistor, the P-well resistor, and the boron resistor.

- **A.** **Calculate the number of squares in the diffused resistor. Neglect the resistance of the pads.**
- **B.** **Measure the resistance of five different diffused resistors on your wafer. Note that each resistor has nominally the same geometry.**
- **C.** **Calculate the sheet resistivity of the diffusion in ohms per square. Also, quantitatively calculate the uniformity of the sheet resistance based on your measurements in part B.**
- **D.** **Calculate the junction depth and estimate the hole mobility by comparing this junction depth calculation to the sheet resistivity measurement in part (C).**

3. TRANSISTOR MEASUREMENT

Perform the following measurement on each transistor. There is a question regarding transistor scaling at the end. You may find it faster to perform step A on all of them, then step B, etc.

A. **Determine the threshold voltage of your transistor. This can be done by using a power supply and curve tracer and observing the gate voltage necessary to get the drain current to rise from zero independent of the drain voltage (with source voltage = 0).**

> **Note: If the drain current is nonzero when the gate voltage is zero, you have a *depletion mode transistor* (oops!). Otherwise, you have an *enhancement mode transistor* (yes!)**

B. **Plot the transistor characteristic curves (drain current vs. drain voltage as parameterized by the gate voltage). Do you see transistor action? Print or trace your 'best-looking' curves, labeling all axes and curves. On the same axes, compare the measured curves to MOSFET theory. How well do they match?**

C. **Calculate the transconductance for your device, using estimated values of dielectric constant, gate oxide thickness, and hole mobility as obtained from Eq. 1 below along with results from part 3B. Compare the transconductance with measurement at these five gate voltages. Is your transistor in the saturation or linear regime during these measurements? Try to get it saturated if possible. (Make sure you compare all transistors at similar conditions). Does the transconductance change as you change the gate voltage?**

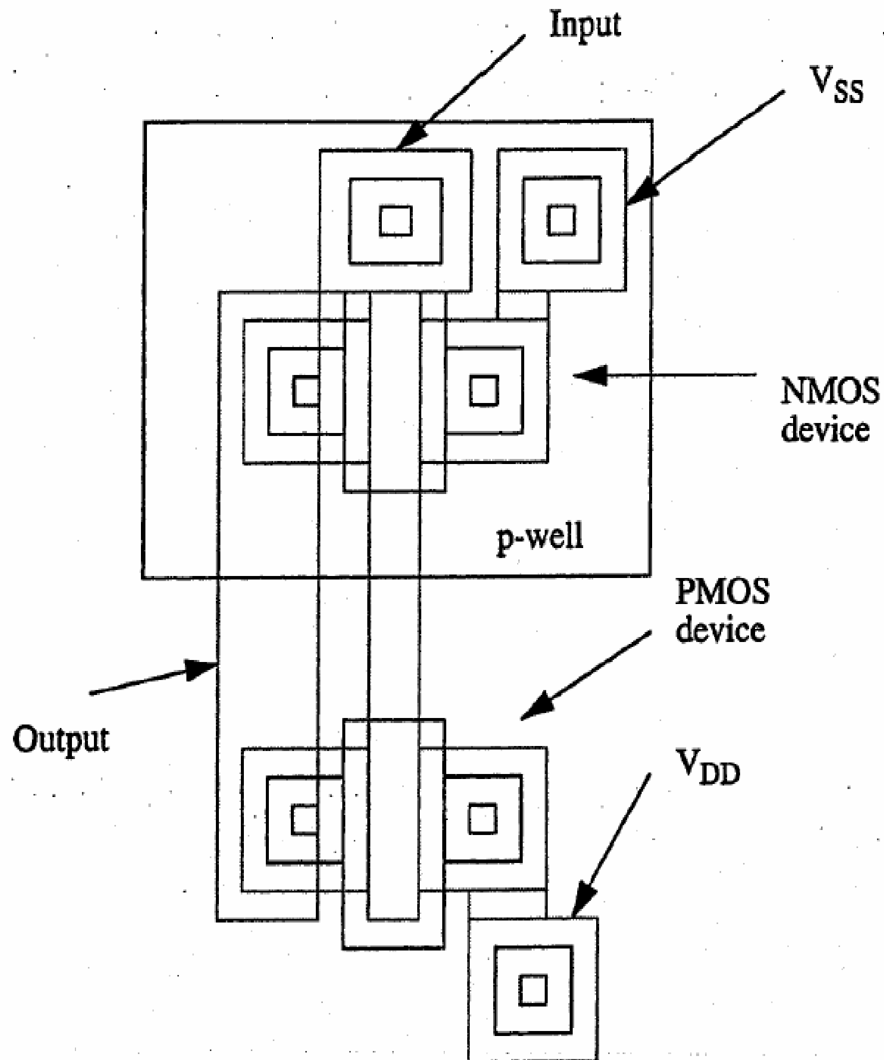
D. **Compare how your measurements scale with varying W/L ratio of your transistors.**

$$I_{Dsat} = \frac{\mu_p C_{ox} W}{2L}\left[V_{GS} - V_T\right]^2.$$

Note: Be sure that measurements of gm for transistors of differing W/L ratios are compared at the same gate voltages

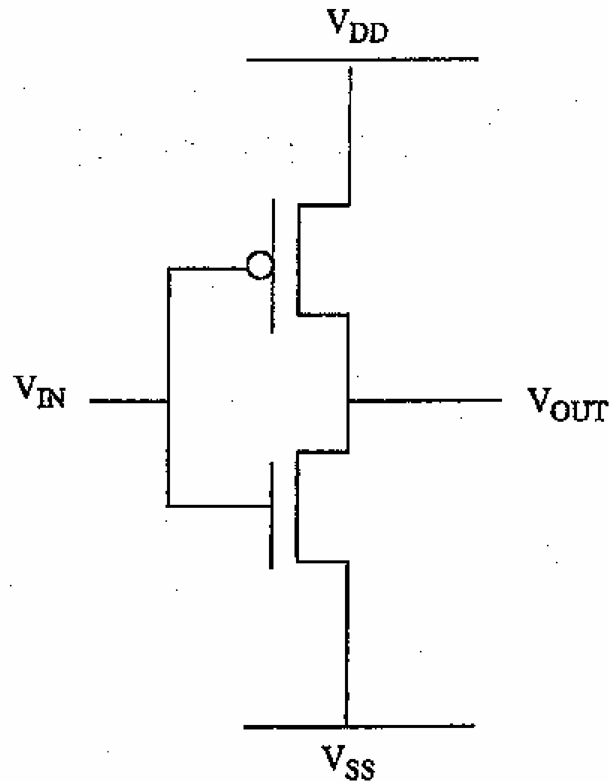
4. CMOS INVERTER MEASUREMENT

The CMOS inverters on your wafers have the following appearance (top view):



A. Choose any inverter on your wafer. Determine and record the width and length of the NMOS and PMOS transistors which comprise the inverter. (The length is either 20 μm or 60 μm. The width of each device is 200 μm).

B. Using the HP 6225A dual power supply (the two supply voltages are labelled V_{DD} and V_{SS}, respectively, in the figure below), connect this inverter in the following circuit configuration:



C. Set $V_{DD} = 5$ V and $V_{SS} = 0$ V.

D. Using the Tenma power supply, sweep V_{IN} from 0 to 5 V in 0.5 V increments. Using the digital multimeter, measure and record V_{OUT} for each value of V_{IN}.

E. Plot the voltage transfer characteristic (VTC) of your inverter (V_{OUT} vs. V_{IN}) using the above data.

F. Based on the VTC plot, estimate and record V_{OH}, V_{OL}, V_{IH}, and V_{OL}. Compute the noise margins of this inverter (NM_H and NM_L).

G. Compare your results to theoretical values and *try* to explain any discrepancies.*

*Note: Your measured VTC is likely to be very far from ideal. Credit will be given for ***plausible*** (but not necessarily correct) explanations of the discrepancies