

Chip-Package Co-Simulation with Multiscale Structures

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Abstract – Chip-package co-simulation is required to predict the interaction between the chip and package at the system level. The FDTD method can be used to analyze these structures but is limited by the Courant condition. In this paper, an alternate method is suggested by combining Laguerre Polynomials with the FDTD method. Since, the solution is implicit, the Courant condition is no longer an issue and therefore the method provides unconditional stability. In addition, the time domain response can be computed similar to the FDTD scheme. The formulation allows the conversion of an electromagnetic problem to a circuit representation with resistors, voltage and current sources. Such a representation is useful since a DC solution can be used to obtain the transient response. To obtain the low frequency response using an FDTD based method, computing the time domain response over long time duration is required. Due to the behavior of the Laguerre Polynomials, this can be difficult. In this paper, computing the time domain response over several micro-seconds is discussed using Laguerre Polynomials combined with the FDTD scheme. This method now can be applied to compute the frequency response from DC to very high frequencies for multi-scale structures arising in chip-package co-simulation.

I. INTRODUCTION

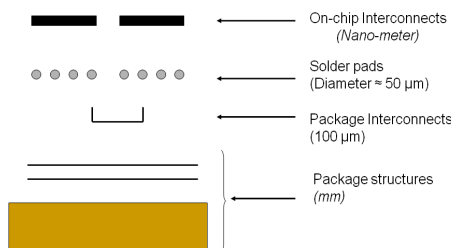


Fig. 1. Multi-scale dimension of chip-package structure

As size of chip and package shrinks and electronic system's performance increases, in order to prevent the system from failure, chip-package co-simulation is required. Such simulations enable signal and power integrity assessments at the system level. When a chip and package needs to be co-simulated, a major bottleneck is the multi-scale dimension of the structures, as shown in Fig 1. The interconnections on the chip are in the nanometer (nm) range while the package level interconnections are in the millimeter (mm) range, resulting in a scale ratio of $1:10^6$. Such structures are difficult to analyze using conventional numerical techniques.

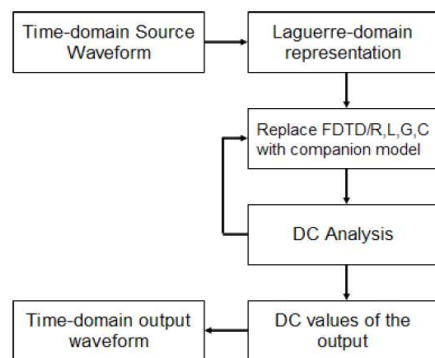


Fig. 2. Flowchart of SLeEC methodology

A method that is very useful for analyzing such multiscale structures is the Laguerre-FDTD scheme. The conventional FDTD scheme proposed in [1] is limited by the Courant condition [2] since the smallest mesh size limits the time step that can be used to ensure stability of the solution. The alternating-direction implicit FDTD (ADI-FDTD) scheme can be used to speed up simulation and has been shown to provide a 10x improvement in simulation time [3]. In this paper, the Laguerre-FDTD scheme has been used where a speed-up of 80 – 200x over the conventional FDTD scheme [4] is possible. This is especially true for multiscale problems.

Since the introduction of Laguerre-FDTD in [4], several modifications have been made to the algorithm for improving its performance [5]. The modified algorithm has been named SLeEC which stands for “Simulation using Laguerre Equivalent Circuit”.

Due to the behavior of Laguerre Polynomials, the current implementation of SLeEC has limitations in the maximum time duration over which the structure can be simulated. Hence obtaining the low frequency response using SLeEC can be a challenge.

In this paper, a method for using the Laguerre-FDTD scheme for simulating over long time is proposed that can then be used to compute the low frequency response in addition to the high frequency response. In this paper, this method has been applied to two structures representative of multi-scale geometries arising in chip-package co-simulation to show the advantages of the technique. This paper is organized as follows: The SLeEC methodology is discussed in Section II. In Section III, details on the formulation for simulating over long time using Laguerre-FDTD is discussed. Simulation results from two test cases are provided in Section V, followed by the conclusion in Section VI.

II. SLEEC METHODOLOGY

The transient EM simulation methodology using Laguerre polynomials is shown in Fig. 2. Only a qualitative description of SLeEC is given in this section. Mathematical details are available in [5]. The first column in Fig. 2 represents operations done in the time-domain and the second-column represents the Laguerre-domain. The first step is to convert a time-domain source waveform from the time domain into the Laguerre domain by representing the time domain waveform using Laguerre Polynomials. The FDTD grid is replaced by an equivalent companion model composed of resistors, voltage controlled-current sources and independent current sources [5]. In the circuit model of the

FDTD grid, the DC solution of the nodal voltages represents electric-field Laguerre coefficients and the branch currents represent magnetic-field Laguerre coefficients. For each of the coefficients that represent the source-waveform, a DC analysis is done once. At the end of each DC analysis, the solution is used to update the companion model before the next DC analysis is done using the next value of the Laguerre-domain coefficient of the source-waveform. Although the number of DC analysis is same as the number of Laguerre coefficients that represents the source-waveform, inversion of matrix is needed only once since the companion model has the same circuitry and resistors for every DC analysis. The final step is to convert the values obtained from the DC solution of the output field of interest into a time-domain waveform.

III. SIMULATION FOR LONG TIME

Mathematically, any time-domain waveform $W(t)$ can be represented in Laguerre-domain as a sum of Laguerre basis functions scaled by Laguerre basis coefficients W_p as shown in (1) [4].

$$W(t) = \sum_{p=0}^{\infty} W_p \varphi_p(t) \quad (1)$$

In-Laguerre FDTD, for efficiency, time-domain waveform $W(t)$ is approximated with only N basis functions as long as error from the approximation is negligible.

$$W(t) = \sum_{p=0}^N W_p \varphi_p(t) \quad (2)$$

The first five Laguerre basis functions are plotted in Fig. 3. Since Laguerre basis function's fluctuation is too slow to describe the interested time-domain behavior in the range of nanosecond or microsecond, time t is transformed into scaled time \bar{t} using a time scale factor s and \bar{t} is used instead of t in the actual simulation

$$\bar{t} = s \cdot t \quad (3)$$

However, in this paper, the use of the time-scale factor is omitted for simplification.

As shown in Fig. 3, Laguerre basis function $\varphi_p(t)$ decays to 0 as t increases where $\varphi_p(t)$ decays slower as its order p is higher. Therefore, as interested time-duration gets longer, higher order Laguerre-domain requires are required for accurate result in the approximation as (2). However, due to the difficulty in computing Laguerre basis functions with high order and long time, Laguerre-FDTD method proposed in [4] has the limitation that simulation can only be performed for a limited time-duration and cannot be done for all time. Consequently, if Laguerre basis functions with sufficiently high order and long time can be computed, the limitation on time-duration can be resolved.

The Laguerre basis function is represented as the product of an exponentially decaying function and the Laguerre polynomial. The n th Laguerre basis function $\varphi_n(t)$ can be represented by multiplying the Laguerre polynomial with an exponential function as:

$$\varphi_n(t) = L_n(t) \cdot e^{-\frac{t}{2}} \quad (4)$$

where $L_n(t)$ stands for n th Laguerre polynomial.

Fig. 4(a) shows a flowchart of the approach used in [5] to compute $\varphi_n(t)$. The Laguerre polynomial of order p can be calculated by using the following recurrence relation.

$$L_0(t) = 1 \quad (5)$$

$$L_1(t) = -t + 1 \quad (6)$$

$$L_p(t) = \frac{1}{p}((2p-1-t)L_{p-1}(t) - (p-1)L_{p-2}(t)) \quad (7)$$

By following the recurrence loop in Fig. 4(a), the Laguerre polynomial $L_n(t)$ has very large value as order n increases and beyond a large enough order number, the value of the basis functions becomes very large to be represented using IEEE 754 floating point standard, and therefore are computed as *Inf*. On the other hand, as is well known, the exponential function $e^{-t/2}$ decays to 0 rapidly and therefore the exponential function is treated as absolute 0 in the computer beyond a certain time-point. Therefore, after some time, the basis function no longer has any meaningful value and is represented as *Inf* \times 0 or *NaN* (not a number), as shown in Fig. 5 that graph terminates abruptly around $t=1440$.

This limitation can be overcome by introducing balancing process in the recurrence loop as shown in Fig. 4(b).

For the description of balancing process in the proposed algorithm, $\varphi_n(t)$ is represented as

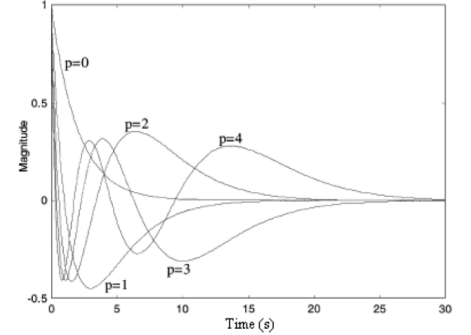


Fig. 3. Laguerre basis functions for order $p=0-4$

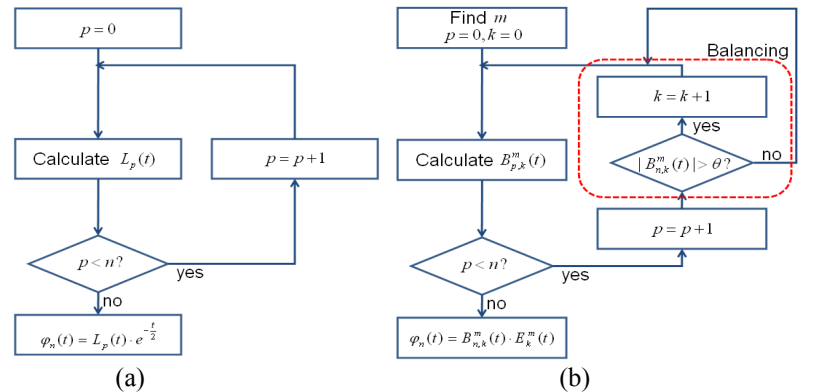


Fig. 4. Algorithm to compute the Laguerre basis function (a): algorithm in [5], (b): proposed algorithm

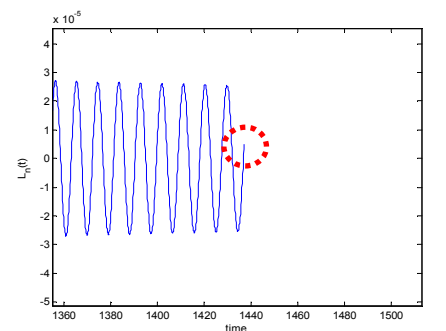


Fig. 5. Calculated 1000th Laguerre basis function by the method in [5]

follows:

$$\varphi_n(t) = B_{n,k}^m(t) \cdot E_k^m \quad (8)$$

where

$$B_{n,k}^m(t) = L_n(t) \cdot e^{-\frac{k}{m}t} \quad (9)$$

$$E_k^m = e^{-\frac{(1-\frac{k}{m})t}{2}} \quad (10)$$

$B_{n,k}^m(t)$ and $E_k^m(t)$ in (9) and (10) are called balanced Laguerre polynomial and balanced exponential function, respectively. $B_{n,k}^m(t)$ can be calculated by using (7) and (9). New parameters and variables such as θ , m , and k are introduced related to the balancing process. θ is a threshold value limits the magnitude of the balanced Laguerre polynomial in the recurrence loop. m and k represents the strength of balancing process and degree of balancing, respectively. Relation between the balanced Laguerre polynomials before and after the increment of degree of balancing is

$$B_{p,k}^m(t) = B_{p,k-1}^m(t) e^{-\frac{1}{m}t} \quad (11)$$

m should be selected to ensure $e^{-\frac{1}{m}t}$ is large enough to handle in IEEE 754 floating point standard. For large t , $e^{-\frac{1}{m}t}$ can be too small to be represented as non-zero value in the computer. This should be avoided since $B_{p,k}^m(t)$ goes to 0 by the increment of degree of

balancing k in that case. Therefore, m needs to be sufficiently large to make $e^{-\frac{1}{m}t}$ treatable in IEEE 754 floating point standard.

A rule of thumb for representing the m in terms of threshold value θ is the following:

$$m \approx \frac{t}{2 \ln \theta} \quad (12)$$

It is to make threshold value θ as follows in terms of m .

$$\theta \approx e^{-\frac{1}{m}t} \quad (13)$$

If (13) is satisfied, by (11), the magnitude of the balanced Laguerre polynomial goes to around 1 as degree of balancing increases.

Balancing process is for preventing the magnitude of balanced Laguerre polynomial from being too large. If the magnitude of balanced Laguerre polynomial gets larger than the threshold value θ , the balancing process is performed by increasing degree of balancing k . Since m and t have positive values, the magnitude of the balanced Laguerre polynomial reduces as degree of balancing k increases as shown in (11). Therefore, the balanced Laguerre polynomial will always remain less than θ in the recurrence loop, which circumvents the NaN problem.

After the computation of $B_{n,k}^m(t)$ is done, the Laguerre basis function can be calculated by using (8). Hence, this formulation enables the application of the Laguerre-FDTD method for computing the response over long time duration.

The computation of the 1000th Laguerre basis function $\varphi_n(t)$ by the proposed method and the earlier method used in [5] is plotted in Fig. 5 and Fig. 6. The method in [5] cannot calculate the basis function $\varphi_n(t)$ when t is larger than 1440, which is equivalent to 20ns when a time-scale factor is 7×10^8 , the proposed method successfully obtains the value of Laguerre basis function at time t greater than 1440, as shown in Fig. 6.

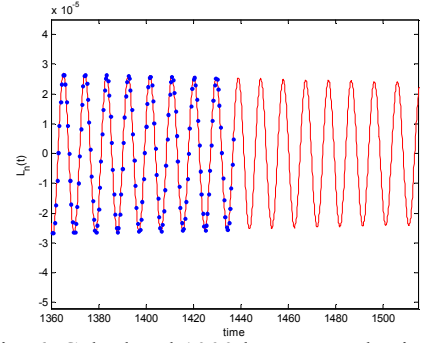


Fig. 6. Calculated 1000th Laguerre basis function

red: proposed method,
blue dots: conventional method in [5]

IV. TEST CASES

A. Simulation of Chip-Package Multi-scale Structure containing SRAM cell over short time

The bird's eye view of the structure modeled is shown in Fig. 7(a). The on-chip structures, along with the interface between the chip and the package, are shown in Fig. 7(b). The zoom of the region marked by the circle in Fig. 7(b) is shown in Fig. 7(c). The on-chip structures in Fig. 7(c) represent the interconnections in M1 and M2 layers of an SRAM cell. The cross-sectional view of the structure is given in Fig. 8. The structure has on-chip interconnects in the metal layers M1 and M2, connected by vias and routed on the redistribution layer, through the solder pads, to the package and routed as package-level interconnects. A feature of the chip-package structure is the multiscale

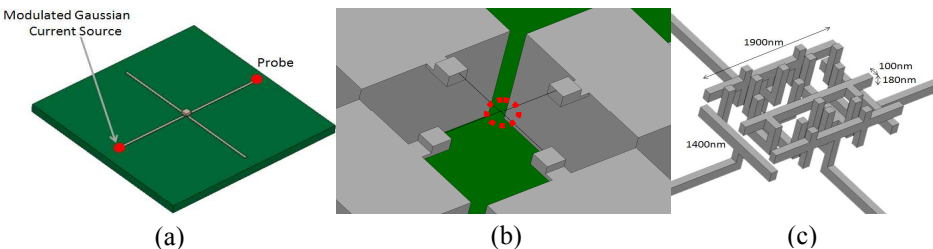


Fig. 7. The bird eye's view of test case A

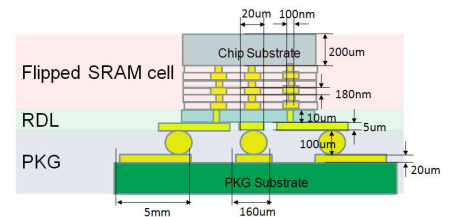


Fig. 8. Cross section of different metal layers with dimensions

dimension from the nanometer (nm) range to the millimeter (mm) range, resulting in a scale ratio of 1:50,000 in this example. The on-chip structures that are in the nm scale require a very fine mesh, and therefore the simulation time can become prohibitively large using the conventional FDTD scheme due to the Courant time-step condition. The time-domain response of the electric field at the location marked probe in Fig. 7(a) up to 5ns has been computed. The Modulated Gaussian current source is used to excite the structure at the end of the package trace as shown in Fig. 7(a). There is good correlation between SLeEC and FDTD as shown in Fig. 9. While FDTD takes 30 hours, SLeEC took only 9 minutes to complete the simulation for the same structure with the same number of cells. This represents a 200x speed-up over the conventional FDTD scheme. The simulations were run on a Pentium quad core, 2.4GHz processor with 4GB RAM.

B. Simulation of Chip-Package Coplanar Transmission Line over long time

As shown in Fig. 10, a coplanar transmission line in the package is connected to on-chip co-planar line through solder bumps [6]. Two ports are defined on the package trace. The structures are assumed lossless in this example. This structure has a scale ratio of 1:10,000. Due to very fine mesh required for the on-chip structure and based on the Courant condition, the estimated simulation time for 1us long simulation is around 212 days. This structure was simulated using SLeEC which took 36 hours. In this example SLeEC showed 100x speed-up over FDTD. Since the transient response was computed for 1us duration, the insertion loss (s21) from 1MHz to 10GHz could be extracted from the simulated time domain waveform using FFT, as shown in Fig. 11. Computing time of test case A and B are summarized in Table 1.

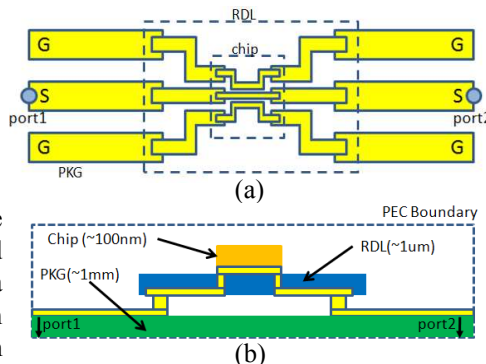


Fig. 10. test case B: coplanar transmission line structure from PKG to chip (a): top view (b): cross-sectional view

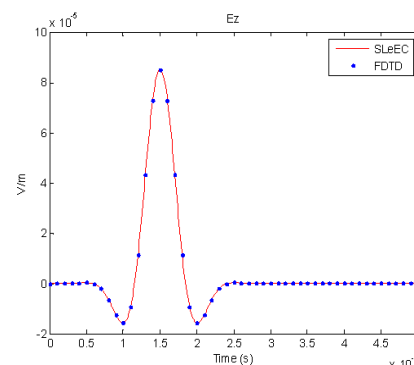


Fig. 9. SLeEC and FDTD results of test case A

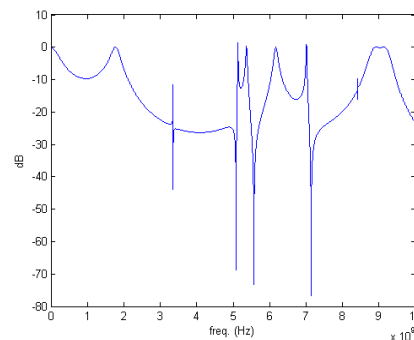


Fig. 11. Insertion loss (s21) of test case B

Structure	SLeEC	FDTD	Speed-up
Test case A (5ns)	9 minutes	30 hours	200x
Test case B (1us)	36hours	212days (estimated)	140x

Table 1. CPU running time

V. CONCLUSIONS

This paper describes a method using Laguerre-FDTD (SLeEC) to compute the transient response of multi-scale interconnect structures. To enable simulation from DC to high frequency, the basis function representations have been modified in this paper. Simulation results using SLeEC show 100 – 200X speed-up over the FDTD scheme, making it a viable candidate for the co-simulation of the chip-package interconnect structures.

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