

# Noise Induced Jitter in Differential Signaling

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## Abstract

Differential lines are extensively used in high-speed digital circuits due to their ability to improve signal integrity by rejecting common-mode noise. However noise is injected into differential signals when there are irregularities in the signaling setup. These anomalies may be via transitions of differential lines through power planes in power distribution systems, via stubs, asymmetric lengths of differential lines, different transition points for each of the differential vias etc. This paper quantifies noise due to irregular differential structures in frequency domain. Presence of noise in differential signaling is verified through a set of test vehicles. The effect of signal to power coupling from differential lines on signal jitter is also investigated.

## 1. Introduction

Ascending data rates and simultaneous miniaturization of electronic packages exacerbates the effect of imperfections in routing of signal traces. It is well known that coupled lines with a differential source excitation are more impervious to noise than single lines [1]. This rejection of noise in differential signaling is made possible by cancellation of opposing return currents [1-2]. Single lines, on the other hand, are very vulnerable to non-idealities in their return path [2] [9].

Prior work on differential signaling focused on perfectly symmetric differential lines where each line in the pair has the same dimensions and is perfectly identical [2]. Noise due to high data rates has increased the importance of study of imbalances in differential signaling. Delay skew introduced by differential sources increases the radiation in differential signaling to high levels as if it were caused by a pure common mode input [3]. It was found that the presence of differential vias causes an additional delay that may be critical in some timing circuits and also degrades signal quality at high frequencies [4]. FDTD simulation was used to prove that differential lines couple considerably to reference planes that are in close proximity [5]. Therefore differential signaling is affected by non-idealities like via transitions, via stubs, slots in reference planes and asymmetric via spacing in packages.

Another important issue in high frequency digital circuits is the accurate prediction of Simultaneous Switching Noise (SSN) effects in packaged electronic systems. Presence of power/ground planes in power distribution networks (PDN) aggravates this problem since these planes act like cavity resonators at high frequencies [6-7]. These planes present a high impedance path to the return displacement current at resonant frequencies when there are interconnect discontinuities in the system. This couples some of the signal energy to the power/ground planes creating cavity noise and increasing the overall power noise. Accurate modeling techniques to capture the effect of signal coupling to planes

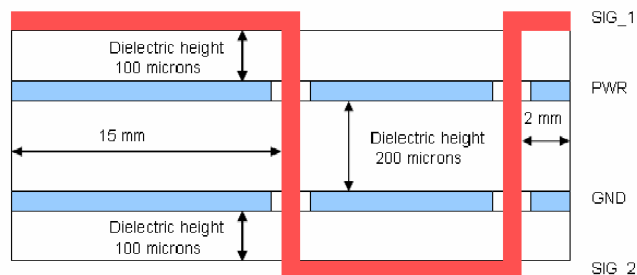


Fig. 1: Cross section of the via transition structure to investigate signal to power coupling

with good correlation to measurements have been developed previously [8].

Coupling of signal energy to the power/ground planes is less in differential signaling when compared to the single-ended scheme [9] [2]. However, in the presence of vertical signal transitions and reference plane changes there is an increase in signal to power coupling even if the differential lines are matched in length. This is because the differential signal not only references the other line but also the planes [5] [9]. Thus even in symmetric and matched differential lines signal energy still couples to planes due to the presence of discontinuities. This phenomenon is not restricted to via transitions. Presence of differential via stubs or asymmetric lengths of differential lines also contribute to the increase of signal to power coupling. Therefore imbalances in differential signaling increase signal to power coupling which in turn amplifies SSN. This paper identifies the amount of signal energy coupled to power planes in various irregular differential structures by simulation and measurements.

Another issue caused by these anomalies in differential signaling is an increase in jitter and other signal degradation effects. Sufficient energy coupling to the power/ground planes can result in corrupted signal transmission on even matched differential lines. This paper quantifies the jitter produced in a differential via transition structure and compares it to ideal differential lines.

This paper is organized in the following manner: Section 2 describes a passive test vehicle designed to capture the noise effects of irregular differential lines. Comparison between measurement results and simulations for signal to power coupling in the different test cases are also presented. Section 3 describes the equivalent circuit model of the differential via transition structure created using Agilent ADS [14]. The accuracy of this circuit model is verified by comparing its S parameter response to measurements. In section 4 prediction of jitter in differential lines with via transitions is performed by using the same circuit model in the time domain.

## 2. Signal to Power Coupling

Different test structures were created to quantify the amount of energy coupled to plane pairs from signal lines in power distribution networks (PDN). Via transitions, via stubs and staggered via transitions are the irregular differential structures studied in this paper. Each of these differential cases is compared to their equivalent single-ended structures. Simulations were performed using the Multi-layer Finite Difference Method (MFDM) [10] and were compared with measurement results. All test structures contain a pair of square planes whose size is 30mm by 30mm. The results for the various structures are given below:

### a) Differential Via Transition

Single-ended and differential structures with via transitions were manufactured with the same cross-section shown in Fig. 1. As seen in Fig. 1, the signal lines undergo a microstrip-to-microstrip transition from layer SIG\_1 to layer SIG\_2 through a pair of planes, PWR and GND. The dielectric used in all layers was FR4 with a dielectric constant of 4.4 and  $\tan \delta = 0.02$  with thicknesses as indicated in Fig. 1.

Coupling to planes was observed in measurements and simulations by exciting the signal lines at one end and simultaneously probing at a point between the plane pairs. Measurements were performed on three different structures to illustrate the amount of energy coupled to the PDN due to differential via transitions. One of these structures was a pair of differential lines with differential impedance of  $100 \Omega$  with edge-to-edge spacing of 0.55 mm and line width of 0.17 mm. Another was a single via transition structure with  $50 \Omega$  single transmission lines designed on layer SIG\_1 with a line width of 0.17 mm referenced to the PWR layer. The third structure was identical to the first differential one except with via transitions. Via transitions occur in the manner illustrated in Fig. 1; one via pair passes through the center of the planes while the other transitions 2 mm away from the edge of the planes.

The signal to plane coupling is measured by the  $S_{31}$  parameter. In the differential via transition structure, ports 1 and 2 are considered to be differential ports while port 3 is single-ended as illustrated in Fig. 2 while all three ports are single ended for the equivalent single via transition. For differential structures, differential to single-ended mixed

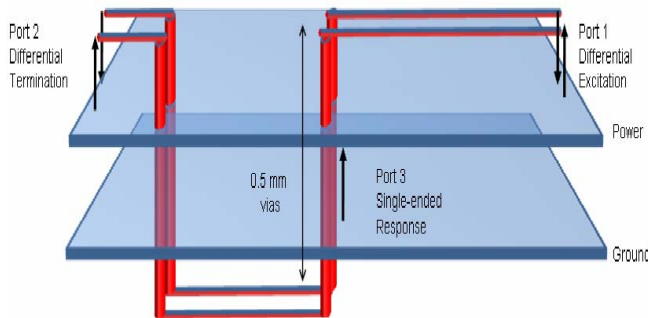


Fig. 2: Differential Via Transition Structure with measurement ports 1, 2 and 3

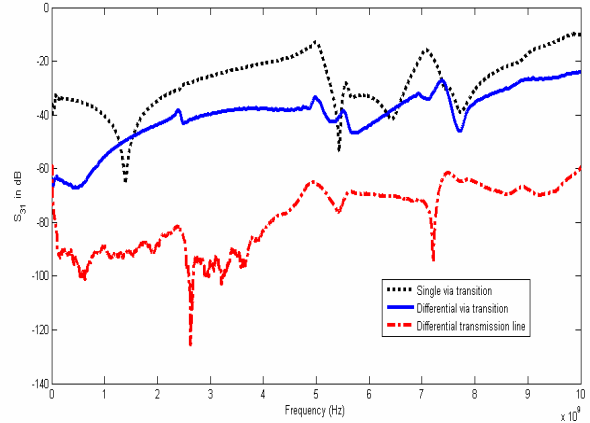


Fig. 3: Signal coupling to planes for Single via transition, Single transmission line, Differential transmission line and Differential via transition -  $S_{31}$  (dB)

mode coupling parameter  $Sds_{13}$  was compared to its equivalent single-ended  $S_{31}$  parameter.

Fig. 3 presents the measured coupling parameters for these three cases. Although coupling due to differential via transition is lower than that for single via transition, it is still significantly more than the coupling for perfect differential transmission lines. This proves that presence of an irregularity such as a via transition in differential signaling increases the signal coupling to planes from -80 dB to -30 dB.

Comparison of measurements and simulation results from the Multi-layer FDM for signal to power coupling in a single via transition structure is presented in Fig. 5. Therefore good model to hardware correlation for power plane energy coupling in single ended structures was verified.

Next the variation in coupling to planes in differential via transition was investigated when the spacing between the differential lines was altered. For this purpose several test cases were formulated which varied the spacing to width ratio (S/W) of the lines. Spacing, S refers to the edge-to-edge spacing between each line in the differential pair and W is the width of the line as indicated in Fig. 4. The  $Sds_{13}$  parameter

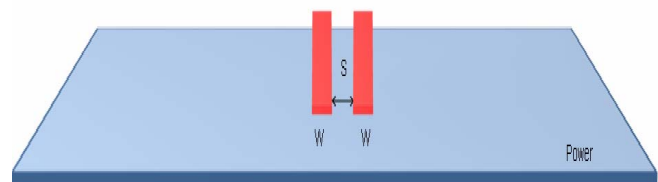


Fig. 4: Spacing by width ratio (S/W) for differential structures

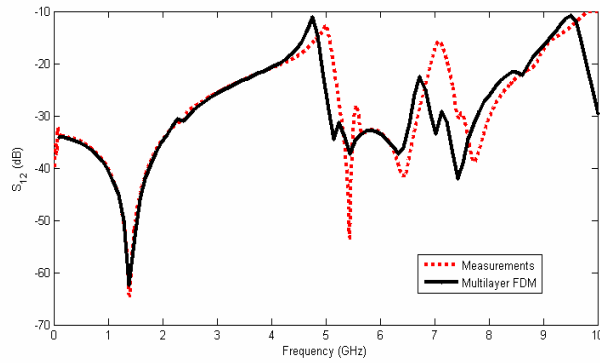


Fig. 5: Coupling to planes,  $S_{31}$  for a Single Via transition

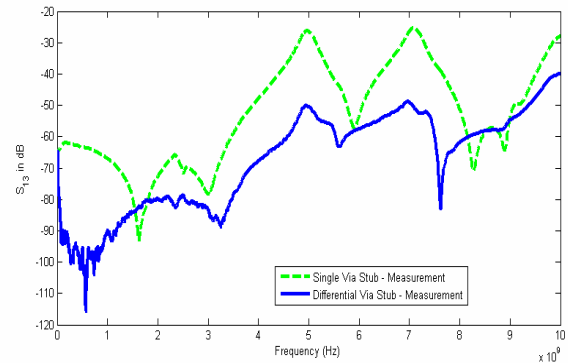


Fig. 9: Coupling to planes due to via stubs

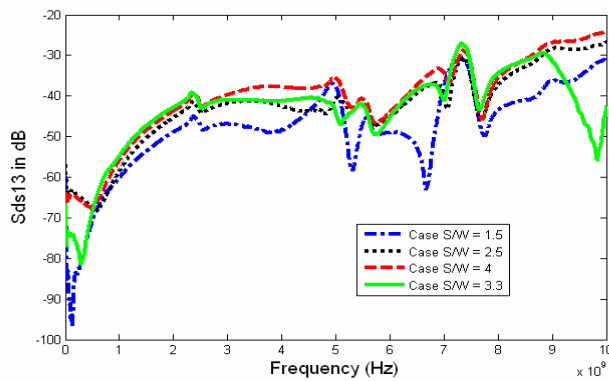


Fig. 6: Coupling to planes for Differential via transitions – varying spacing by width ratio (S/W)

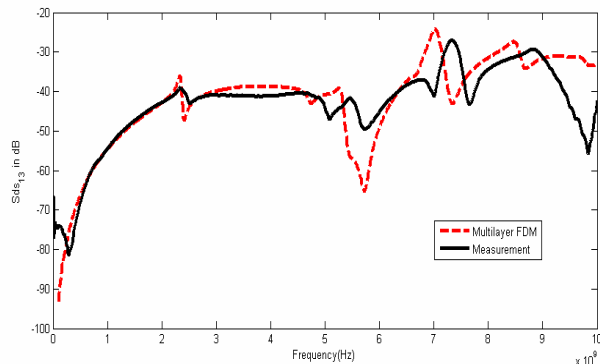


Fig. 7: Measurement versus simulation results for coupling to planes for differential via transition with  $S/W=4$

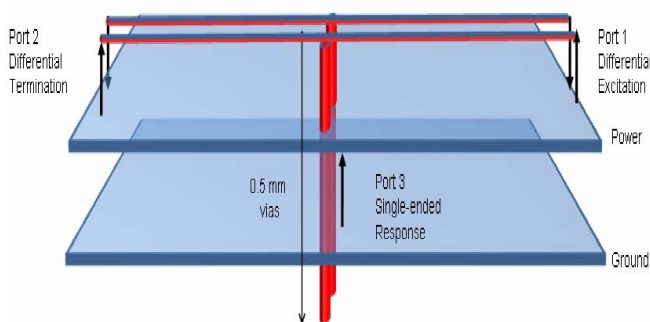


Fig. 8: Differential Via Stub structure

for structures with S/W ratio of 1.5, 2.5, 3.3 and 4 were measured.

As expected, it was found that increase in S/W ratio results in the augmentation of coupling to planes which is shown in Fig. 6. This implies that in the presence of via transitions one must ensure tight coupling between differential lines to reduce energy leaking to planes. The rule of thumb is to keep  $S/W \leq 3$  to ensure adequate coupling between the lines in the differential pair [11]. There is good correlation between simulation and measurement for differential via transition – one example with  $S/W=4$  is illustrated in Fig. 7.

Therefore, model to hardware correlation proves that coupling to planes is significantly larger in the presence of discontinuities like via transitions rather than in symmetric and closely-coupled differential lines

### b) Via Stubs

Another irregular structure in boards and packages is caused by through-hole vias used in lieu of blind/buried vias. These through-hole vias act like via stubs that radiate significant signal energy into the PDN. A single via stub was compared to a differential one to examine the difference in signal to power coupling between them. The via stub structure was considered to be a through hole via hanging from a microstrip line in both differential and single-ended test vehicles as shown in Fig. 8. The dimensions of the signal lines and vias were identical to the via transition case as shown in Fig. 1.

Measurements indicate that the level of coupling in differential via stub structure is lower than that of single via stubs as presented in Fig. 9. Differential via stubs still produce significant coupling at approximately 10 GHz as indicated by measurements of this test vehicle. This anomaly in differential signaling is usually not taken into consideration and could produce unexpected power noise.

### c) Staggered Differential Via Transition

High noise rejection is the main advantage of differential signaling and it can be utilized only by routing the individual traces in close proximity. Moreover, the traces have to be symmetric so that any common mode noise injected into the lines can cancel out each other. Thus the general rule of thumb is to route discontinuities like via transitions in a symmetric manner so that noise infiltrates both the lines in the

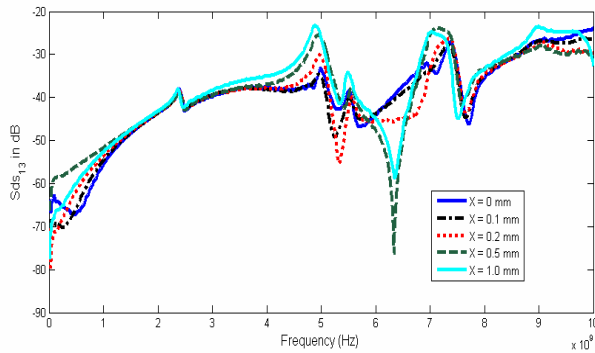


Fig. 10: Coupling to planes due to staggered differential via transitions

differential pair equally.

Test vehicles were designed to probe into the effects of staggered differential via spacing on the signal to plane coupling. Staggered spacing refers to increasing asymmetry in the placement of vias in differential lines as shown in Fig. 11. The total physical length of each line in the differential pair still remains the same. All other dimensions are identical to the case described in the differential via transition section. In all the test vehicles the effect of staggered vias on plane pair coupling was investigated by increasing spacing  $x$  from 0 mm to 1 mm.

Measured  $Sds_{13}$  for values of  $x$  equal to 0 mm, 0.1 mm, 0.2 mm, 0.5 mm and 1 mm are displayed in Fig. 10. Increase in via asymmetry amplifies the signal to plane coupling from -35 dB to -25 dB. A rule of thumb can be formulated from these results; staggering via transitions by more than 0.2 mm causes significant increase in energy coupling to PDN. Therefore to minimize signal to plane coupling, differential vias must be routed in a symmetric manner.

In this section it was quantitatively established that irregularities in differential lines like via transitions, via stubs and staggered vias amplify signal to plane coupling. It is important to be careful of such discontinuities while designing differential lines because loss of signal energy to power planes could deteriorate the quality of signal transmitted. Therefore signal integrity could be worsened by fall in the voltage margin of the signal and introduction of jitter.

### 3. Model to Hardware Correlation – Equivalent Model

Simulations performed using the Multilayer FDM provided good model to hardware correlation with measurements. A comparable circuit model was required to examine the effects of signal to power coupling in time domain. Thus an equivalent model was constructed using the circuit solver Agilent ADS. In this paper, the only structure considered for time domain analysis is the differential via transition. Thus a circuit model was created for this case and S parameter response of this model was matched with measurements and simulations.

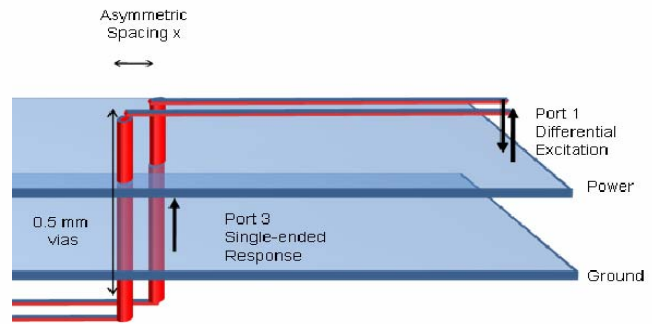


Fig. 11: Cross section of staggered via transition structures

The differential via transition was broken into three blocks, two microstrip lines and one plane pair, to construct the equivalent model as illustrated in Fig. 12. Here the top plane is the power (Vdd) plane while the bottom is the ground (Vss) plane. Each block in the model consists of pre-simulated S parameter files. The microstrip models were obtained from Agilent ADS and the plane pair block was simulated using the Multilayer FDM. The via model was constructed from two simple inductors, one for each differential line, and accounted for mutual inductance. Formulae for self and mutual inductance were obtained from [12].

The differential insertion loss  $Sdd_{21}$  obtained from the model was compared to measurements and simulations as indicated in Fig. 13. Signal to plane coupling,  $Sds_{13}$  was also compared as shown in Fig. 14. It was found that the equivalent circuit model correlated well with measurements for the differential via transition. Therefore investigation of jitter in differential via transitions was reliably performed using this circuit model.

### 4. Time Domain Simulations

As observed from measurements, an increase in the S/W ratio of differential via transition structures resulted in a corresponding amplification of signal to power coupling in the frequency domain. In this section, results of a time domain analysis of the signal to power coupling is presented.

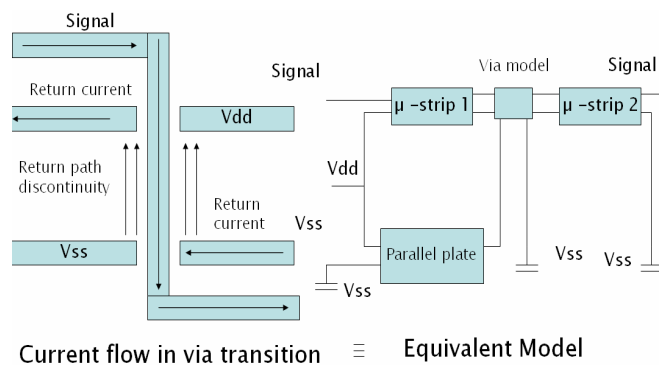


Fig. 12: Equivalent model for a microstrip-to-microstrip signal via transition

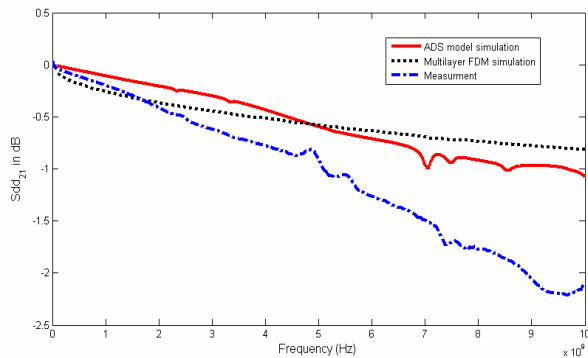


Fig. 13: Comparison of Differential Insertion Loss between the equivalent model, measurement results and other simulations

The equivalent model developed in Agilent ADS was used to determine the amount of jitter on differential lines in the presence of vias. The effect of S/W ratio of differential lines on jitter was also investigated.

Total jitter in a signal can be described as a combination of random and deterministic jitter [13]. Deterministic jitter is caused by electromagnetic interference (EMI), crosstalk and reflections. EMI due to signal to power coupling causes ground bounce and other power supply variations. Power noise produced in this manner causes jitter on the signal lines referenced to these planes. Thus the jitter studied in this paper is deterministic and it will not increase with an increase in the number of samples as long as sufficient input bits are provided to the circuit model. In this section only peak to peak jitter is considered.

At first the jitter in differential lines without any discontinuities or irregularities was computed. For differential lines with spacing to width ratio (S/W) at 1.5, 2, 3.3 and 4, jitter was calculated after simulating the time domain waveform in Agilent ADS for 10000 bits at a data rate of 5 Gbps. The eye diagram for a 29 mm long differential line with spacing to width ratio (S/W) of 3.3 and 100  $\Omega$  differential impedance is shown in Fig. 15. The eye diagram was plotted for the differential output voltage  $y_{diff}$  and peak to peak jitter was calculated to be 1.2 psec. The jitter for all the other differential line cases with varying S/W ratio is displayed in Table 1. Thus differential lines display negligible jitter in the absence of via discontinuities.

A pseudo-random bit source (PRBS) with a linear feedback shift register design was utilized to provide random input bits to the differential signal lines. Frequency spectrum of the input signal contains components at many frequency points due to the randomness of the voltage bit stream. The return current in the differential structure is dependent on the input voltage; hence it will also contain significant components at many frequencies. In the differential via transition structure the return current flows through the dielectric between the planes because of the via discontinuity. Thus the return displacement current will face impedance that varies with frequency because the impedance profile of the plane pair is frequency dependent. This will cause variance in

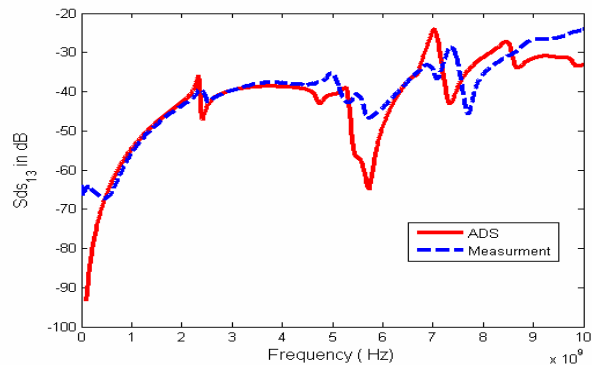


Fig. 14: Comparison of signal to plane coupling between equivalent model, measurements and other simulations

the rising and falling slopes of the output signal during transitions between voltage levels causing jitter on these lines. Jitter will be further exacerbated when the impedance of the plane pair increases due to signal to power coupling. Thus actual amount of jitter caused will largely depend on the quantity of noise coupled to the power/ground planes increasing the PDN impedance.

The time domain simulation of differential via transitions used the equivalent model shown in Fig. 12. Differential excitation was provided by two pseudo-random bit sources and the lines were correctly terminated with a 100  $\Omega$  resistor. The jitter caused due to the loosely coupled differential via transition structure lines where S/W= 4 is shown in Fig. 16. The data rate of the random input bit stream was maintained at 5 Gbps and the output calculated for 10000 bits. The jitter computed for this case was equal to 11.69 psecs. Eye diagram for the tightly coupled differential via transition (S/W =1.5) was also plotted and is displayed in Fig. 17. Peak to peak jitter was computed for differential via transitions with spacing to width ratio (S/W) of 1.5, 2, 3.3 and 4 and displayed in Table 1.

It was found that there is a definite increase in the amount of peak to peak jitter in differential signaling due to via transitions. Jitter increases from approximately 0.64 psec to nearly 12 psec in the case where S/W ratio is 4 as shown in Table 1. This trend is observed in differential signaling irrespective of the S/W ratio.

It was also determined that increase in the S/W ratio of differential via transitions does not correspondingly amplify jitter. Jitter increases from 8.36 psec to only 11.69 psec with a corresponding change in S/W from 1.5 to 4. Thus it can be concluded that even in tightly coupled differential lines the effect of via transitions still can not be ignored or compensated by a reduction in edge-to-edge spacing.

In a bus of differential lines with via transitions every pair of lines could experience a jitter of greater than 12 psec. This is because, all these differential lines will switch in random patterns and couple increased signal energy to the PDN. Thus SSN could be adversely affected and this will cause an amplification of jitter. Therefore, though jitter of 12 psec in a differential via transition pair may seem small in comparison to its 5 Gbps pulse width it is non-negligible when considering a bus of differential via transitions.

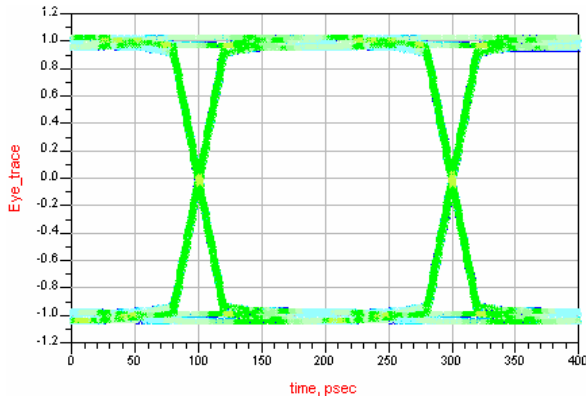


Fig. 15: Eye diagram for differential line with spacing by width ratio (S/W) equal to 3.3

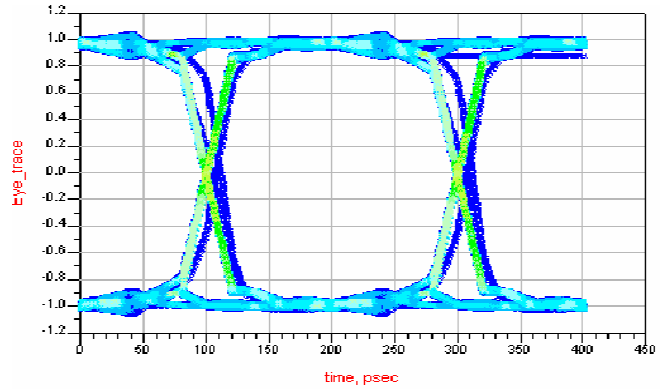


Fig. 17: Eye diagram for differential via transition with differential line spacing to width ratio (S/W) = 1.5

Spacing by Width Ratio (S/W)	Peak to Peak jitter for differential lines with no vias	Peak to Peak jitter for differential lines with vias
1.5	0.26 psec	8.36 psec
2	0.35 psec	9.44 psec
3.3	1.20 psec	11.16 psec
4	0.64 psec	11.69 psec

Table 1: Peak to Peak jitter calculated for differential lines

### Conclusions

Model to hardware correlation proves that anomalies in differential signaling such as via transitions, via stubs and asymmetry in differential vias couple significant energy to the power distribution network. This signal to power coupling is found to vary with the spacing by width ratio (S/W) of differential lines. Time domain simulations of the equivalent circuit model for differential via transition structure indicate an increase in peak to peak jitter in the presence of via transitions. This jitter is found to vary very little with spacing by width ratio of differential lines. Jitter in differential via transitions is observed to be more than the amount found in perfectly routed differential lines. Experiments and simulations have been performed to validate the above

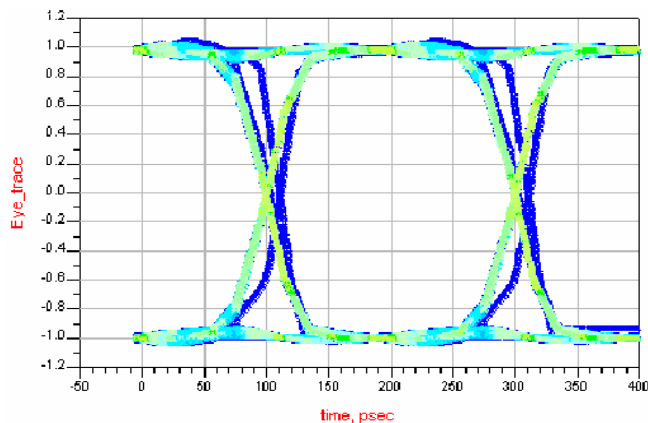


Fig. 16: Eye diagram for differential via transition with differential line spacing to width ratio (S/W) = 4

conclusions. Consequently jitter due to discontinuities like via transitions could prove to be critical when irregular differential bus structures are routed in packages and boards.

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