

An Optical Clock Distribution Network for Gigascale Integration¹

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Abstract

A novel system-level model describing a printed wiring board-level, high-fanout, curved aperture optical waveguide H-tree network using volume grating focusing couplers is presented. The intra-chip optical network globally distributes an optical signal to monolithic CMOS receivers for local clock distribution. An estimation for the available optical output power as a function of distribution fanout is presented. Assuming -2 dB optical loss per Y-junction, a distribution fanout of 256 can be achieved for an optical input power of 1.23 W.

Introduction

One proposed alternative to avoid the global electrical interconnection limitations that inhibit multi-GHz microprocessor clock frequency distribution [1] is the use of optical clock distribution networks (OCDN) [2,3]. Architectural projections for gigascale microprocessors implemented in future technology generations call for single-chip multi-processors to overcome conventional single core throughput [4]. There is a need for local frequency multiplication circuitry within each node of a multi-processor operating at GHz clock frequencies due to the inherent bandwidth limitations of global interconnections [5]. To avoid the need for frequency multiplication circuitry within each processing node, a performance requirement for an optimized optical clock distribution network is the capability to propagate the local clock frequency globally across chip.

Optical Clock Distribution Network

Figure 1 illustrates the target system for application of the proposed distribution. This system exhibits the following key features: a) no on-chip photonic sources; b) monolithic silicon-based detection; c) global optical signal propagation through a board-level guided-wave H-tree distribution; and d) the use of volume grating focusing couplers to provide tolerance relative to horizontal and vertical misalignment of the flip-chip assembly. The waveguide distribution and volume couplers are described in the following sections.

Waveguide Distribution

The high achievable fanout, scalability, and symmetry of an optical waveguide H-tree distribution complement the projected multi-processor architecture. To estimate the amount of optical power available at the output of a multi-level optical H-tree, the approach of Bakoglu [6] in describing an n-level electrical H-tree distribution is adapted. In the case of an optical waveguide H-tree, the index m is used to represent the number of complete H's implemented optically. The m -level network is viewed as a series of arcs connected sequentially from the point of optical power input to the point of output coupling. In this model, the optical signal propagation path consists of two arcs of radius R_m connected in succession within every m^{th} level, seen in Fig. 2. In presenting an optical power budget for a waveguide-based H-tree distribution, six elements of optical loss must be incorporated: 1) coupling loss in going from the board-level laser source to the board-level distribution network; 2) waveguide propagation loss due to intrinsic waveguide material absorption and scattering losses; 3) bending loss incurred along each curved path of radius R_m due to the inherent mismatch between the phase velocity of the guided mode and radiation mode in the outer cladding region [7]; 4) power-splitting loss at each Y-junction due to reflection and scattering losses into the propagation path and surrounding medium, respectively [8]; 5) loss incurred at each volume grating focusing coupler [9-11]; and 6) reflection loss at the air/dielectric interface of the chip-scale package (Fig. 1).

An expression for the approximate optical output power (in W/W) of an m -level waveguide-based H-tree distribution is given by

$$\frac{P_{out}}{P_{laser}} = \left(\frac{T_{yjunc}}{2} \right)^{2m} \eta_{input} \eta_{grating} \eta_{reflection} e^{-2 \left\{ \sum_{k=1}^m \alpha_{bend}(k) L_{arc}(k) \right\}} \quad (1).$$

P_{laser} is the average output power of the photon source. The factor of two in the denominator of Eq. (1) represents the division of power between each Y-junction arm and T_{yjunc} represents the transmission coefficient of the optical wave through each Y-junction. Three key optical efficiencies are represented by η_{input} , $\eta_{grating}$, and $\eta_{reflection}$, where η_{input} is the laser-to-waveguide coupling efficiency,

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η_{grating} is the grating diffraction efficiency, and $\eta_{\text{reflection}}$ is the transmission efficiency across the air/dielectric package interface. The exponential term represents the bending loss incurred within each successive distribution arc [7], where $\alpha_{\text{bend}}(m)$ and $L_{\text{arc}}(m)$ are the bending loss coefficient and arc length, respectively, for a single arc within the m^{th} level. Propagation losses for polyimide optical waveguides have been reported as low as 0.1-0.5 dB/cm [12], and are therefore neglected in these simulations.

A key element of the proposed distribution network is the means by which coupling of the board-level optical signal to chip-level monolithic receivers is achieved. An acceptable degree of tolerance to variability in the horizontal and vertical positioning of the chip is critical. Research targeting inter-chip clock distributions for a Cray Supercomputer employs a tilted binary surface-relief grating coupler [13]. The proposed distribution uses a volume grating focusing coupler, which allows for focusing of the optical beam with high transmission efficiency to an area enclosed by both a) the range of worst-case horizontal and vertical divergences of the flip-chip assembly [14], and b) variations in the output wavelength of the photon source [15]. Figure 3 shows a schematic of the volume grating focusing coupler.

A volume grating focusing coupler design based on the analysis in [9-11] is presented in Table 2. The uncoupled beam is focused to a rectangular line located 215 μm above the center of the coupler. The target focal point of the line was chosen as $(x_f, z_f) = (0 \mu\text{m} \pm 5 \mu\text{m}, 215 \mu\text{m} \pm 10 \mu\text{m})$, assuming a) a solder ball height, $t_{\text{solder}} = 100 \mu\text{m}$ [16]; b) a chip-level package thickness, $t_{\text{package}} = 100 \mu\text{m}$ [17]; c) an overall thickness, $t_{\text{wiring}} \cong 15 \mu\text{m}$ for the monolithic multi-level interconnect network [18]; d) a horizontal x and y deviation of $\pm 5 \mu\text{m}$ due to the flip chip process [19]; and e) a vertical bump deviation of $\pm 10 \mu\text{m}$ [16]. The design wavelength is chosen as $850 \pm 10 \text{ nm}$ [15]. Figure 4 illustrates a series of ray traces which describe the coupler output at the target focal point for wavelengths corresponding to 840 nm, 850 nm, and 860 nm (top to bottom, respectively) produced by a 150 μm long coupler. Under the assumed wavelength and spatial variations, the minimum required detector area is given by

$$A_{\text{detect}} = (\Delta x_{\Delta\lambda} + 2\Delta x)(w_g + 2\Delta y). \quad (2)$$

In (2), $\Delta x_{\Delta\lambda}$ is the horizontal optical beam width transverse to the width of the waveguide, w_g is the grating (waveguide) width, and Δx and Δy are the maximum placement variations due to the solder attach process. To determine beam-defined minimum detector size, the difference between the maximum horizontal beam width over $z_f \pm \Delta z_{\Delta\lambda}$ at $(\lambda + \Delta\lambda)$ and $(\lambda - \Delta\lambda)$ is calculated. For a horizontal beam width $\Delta x_{\Delta\lambda}$ of 18 μm (labeled in Fig. 4), the approximate detector area required for full coverage of the optical beam is found to be 560 μm^2 . Estimations

for optical output power, P_{out} , based on Eq. 1 are obtained assuming a) 817 mm^2 for the ITRS projected die size, b) -2 dB loss per Y-junction in the distribution, c) 88% transmission efficiency of the grating couplers, and d) a projected value of 1.23 W of available optical output power for a monolithic two-dimensional vertical cavity surface emitting laser (VCSEL) array [20].

Conclusions

Table 3 lists the optical power available at the surface of the chip-level detectors for various levels of fanout. To compute a preliminary optical power budget, a receiver sensitivity of -10dB is assumed at the target clock frequency, along with the incorporation of 6dB of optical power margin for lifetime performance degradation. From Table 3, for an optical input power of 1.23 W, global optical distribution of the local clock frequency to each output node is achieved for optical fanouts ≤ 256 .

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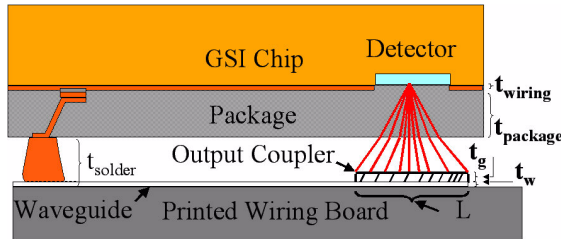


Figure 1: Proposed structure of OCDN

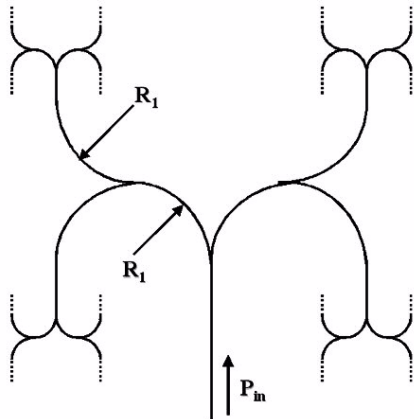


Figure 2: Board-level guided wave H-tree distribution

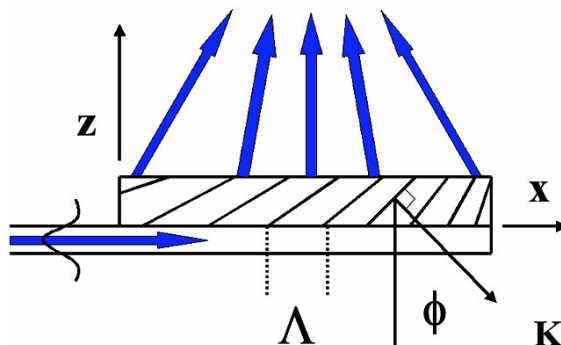


Figure 3: Volume grating focusing coupler

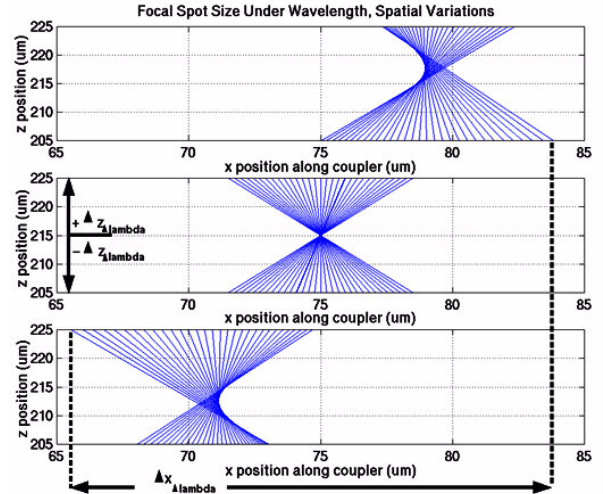


Figure 4: Ray trace of focal spot size under wavelength, placement variations

Table 1: Grating design summary

Coupler Structure	
Coupler Length, L	150 μ m
Cover index, n_c	1.00
Substrate index, n_s	1.46
Waveguide index, n_w	1.56
Grating (Waveguide) width, w_g	10.00 μ m
Waveguide thickness, t_w	0.35 μ m
Grating thickness, t_g	10.00 μ m
Maximum slant angle, ϕ_{max}	50.4 $^\circ$
Minimum slant angle, ϕ_{min}	37.8 $^\circ$
Max grating period, Λ_{max}	0.44 μ m
Min grating period, Λ_{min}	0.36 μ m
Coupler Performance	
Waveguide effective index, N	1.51
Coupling Efficiency	88%
Focal spot width, $\Delta x_{\Delta\lambda}$	18 μ m

Table 2: Optical system properties

Horizontal placement variations, Δx and Δy	$\pm 5\mu$ m
Vertical placement variations, $\Delta z_{\Delta\lambda}$	$\pm 10\mu$ m
Min detector area (μm^2)	560 μm^2
Wavelength, λ (nm)	850 \pm 10
Laser-to-Waveguide Coupling Loss	- 3dB
Loss per Y-junction	- 2dB
Air/Dielectric Reflection Loss	- 0.2dB

Table 3: Optical output power vs. distribution fanout

Level, m	1	2	3	4
No. Nodes, H-tree	4	16	64	256
Input Power (dBm)	30.89	30.89	30.89	30.89
Distribution Loss (dB)	-11.74	-19.77	-27.80	-35.81
P_{out} (dB)	19.14	11.12	3.10	-4.92
Lifetime Degradation (dB)	6	6	6	6
Sensitivity (dB)	-10	-10	-10	-10
Loss Margin (dB)	23.14	15.12	7.10	-0.92