Compliant Probe Substrates with Two-Material, Air-Clad, Grating-in-Waveguide Optical I/O Interconnects

Hiren Thacker, Anthony Mule', Ricardo Villalaz, Thomas Gaylord, and James Meindl

Microelectronics Research Center, Georgia Institute of Technology, Atlanta, Georgia 30332-0269, E-mail: hdt@ece.gatech.edu.

Introduction

Optical interconnects have been identified as a potential solution to overcome the performance limitations imposed by electrical interconnects in gigascale integration (GSI) chips [1]. The bandwidth provided by optical interconnects is especially attractive for chip-to-package and chip-to-chip communications [2]. While numerous efforts are underway to investigate the integration of optical interconnects and silicon microelectronics [3]-[6], virtually no work has been reported relating to the hybrid wafer-level testing of these chips. A novel, high-density compliant probe substrate with electrical and optical probes is demonstrated in this paper. The primary purpose of this probe substrate is to provide a non-damaging, temporary interface between the device-under-test (DUT) and automated test equipment (ATE) during wafer-level testing. The probe substrate would find application for testing a full range of devices with electrical and optical I/O interconnects.

Design

Figure 1 shows a schematic of the probe substrate configuration. The electrical probes are comprised of compliant interconnects capped with metal contacts [7]. They are compliant in the z-direction (normal to the surface) but maintain x-y (in-plane) positional accuracy. The compliance is desirable to account for any height variations in the DUT or in the probe substrate itself. Test signals are transferred to the back-side of the probe substrate via plated, through-substrate interconnects. The pads on the back-side interface with the ATE.

The probing of optical I/O differs from that of their electrical counterparts. While in most cases an optical-to-electrical conversion would be needed, there will be situations where a simple loopback of the high-speed optical signal is warranted. Hence, the design and layout of optical components on the probe substrate is dependent on the intended test plan.

The optical "probes" consist of waveguides terminated by volume grating couplers, which have been shown to have high input (80% [8]) and output (95% [9]) coupling efficiencies. Using this configuration, in-plane optical signals are directed normal to the surface, towards the DUT, or vice-versa. Optical sources, mounted either on the probe module or ATE, supply test signals to the DUT via the grating-in-waveguide structures. Similarly placed photodetectors perform an optical-to-electrical conversion of the test response collected from the optical I/O. A waveguide with volume grating couplers on each end could be used for scenarios where signal loopback is desired.

Fabrication

The compliant probe substrate is built on a silicon (Si) wafer so that standard microelectromechanical systems (MEMS) and integrated circuit (IC) fabrication techniques can be used. First, through-wafer vias are drilled in the silicon using the Bosch process in a Si deep reactive ion etcher (DRIE). Following this, the vias are passivated, and filled with electroplated copper to make them conductive. A polishing and etching process is then used to planarize the overplated copper, and to yield pads on the back-side of the wafer. A 6μm thick layer of SiO_2 is then deposited, and a volume grating layer, pre-fabricated in Omnidex HRF 600 photopolymer (from Dupont), is laminated on top of the oxide. Raised-strip grating channels are produced through hard-mask patterning and reactive ion etching. Next, a 0.12μm layer of low-temperature (150°C) SiO_2 is deposited to provide better adhesion between the Omnidex grating polymer and Avatrel 2190P polymer from Promerus, LLC, which has been shown to be a suitable waveguide material [10]. The photo-definable Avatrel is spun on to the substrate, and patterned, using wet developing, into waveguides (Figure 2). This concludes the two-material, grating-in-waveguide fabrication.

The compliant electrical probes and metal contacts are then fabricated using repeated photolithography and electroplating steps [7] (Figures 3-4). The metallurgy of the contacts is important in assuring a long-lasting, reliable, electrical probe.

Characterization

The electrical probes have an average contact resistance of 0.5 ohm. The diffracted intensity output of a grating-in-waveguide structure on the probe substrate (Figure 5) is plotted against distance in Figure 6. It has a measured grating coupling coefficient $\alpha = 3.95\ mm^{-1}$. Detailed characterization of the two-material, grating-in-waveguide I/O is provided in [10].

Conclusions

A probe card for wafer-level testing of GSI chips with electrical and optical I/O interconnects is reported for the first time, to the author's knowledge. The probe substrate, comprising of compliant electrical probes, and two-material, air-clad, grating-in-waveguide, optical probes, has been fabricated, demonstrated, and characterized.

References

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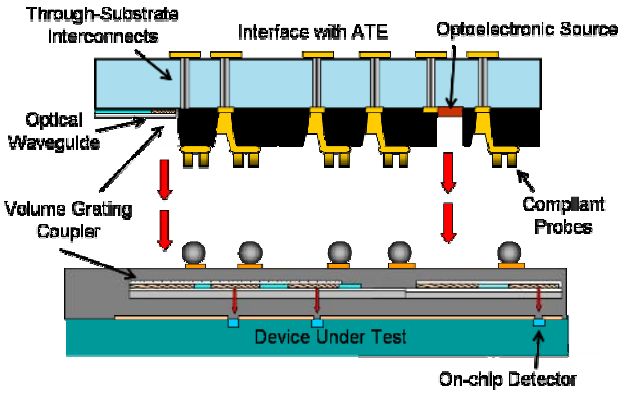

Figure 1: Schematic of compliant probe substrate with two-material, grating-in-waveguide optical interconnects.

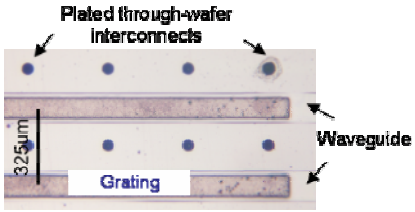

Figure 2: Image of two-material, grating-in-waveguide interconnects fabricated on silicon with plated through-wafer interconnects.

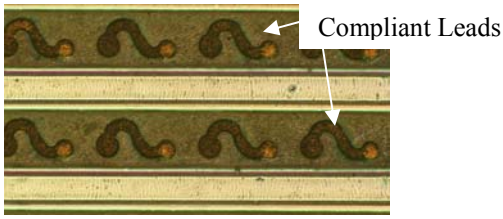

Figure 3: Image of compliant leads fabricated alongside grating-in-waveguide optical interconnects.

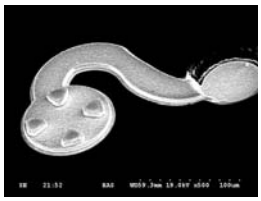

Figure 4: SEM image of a single compliant, electrical probe with plated metal contacts.

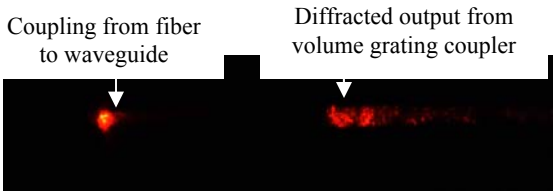

Figure 5: Image of diffracted output from a patterned grating-in-waveguide channel.

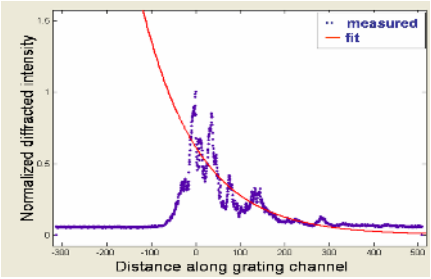

Figure 6: Robust linear least squares fit to normalized diffracted intensity of patterned grating channel corresponding to a coupling coefficient $\alpha = 3.95\ mm^{-1}$