

Performance Issues in High Density Printed Wiring Board design for High I/O Compliant Wafer Level Packages

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Biography:

Chirag Patel is a Ph.D. candidate in the school of electrical and computer engineering at Georgia Institute of Technology. His dissertation is on the design, development and analysis of Compliant Wafer Level Package technology under the guidance of Professor James D. Meindl and Dr. Kevin P. Martin. His work on the Compliant Wafer Level Packaging involves the fabrication, design, theoretical model development, analysis and testing of the package. He has held an internship at Tesser where he worked on the development of low temperature wafer level processing of high reliability joints for *m*BGA packages.

Abstract:

Chip scale and wafer level packages demand very high density printed wiring boards (PWB). In this paper we concentrate on various performance issues associated with the design of high density PWB required for high I/O Compliant Wafer Level Packages (CWLP). First, we develop an analytical model to understand the need of high density PWB. Second, we discuss the impact of high density wiring on off-chip speed, signal integrity, I/O current density, heat removal, and electrical properties of materials.

Introduction:

Electronics packaging has come a long way to meet the increasing demands of the semiconductor industry. The size, weight and performance requirements of portable and mobile

communications markets have necessitated the development of chip scale packages (CSP) and Compliant Wafer Level Package (CWLP) [1] that are by definition 1 to 1.2 times the area of the silicon chip it packages. Furthermore the growing functionality of electronic products have required high I/O density packages. It is a major challenge to supply high I/O density packages that are continuously shrinking in size. Four factors contribute to the applicable limit on the I/O density of chip scale packages. These are: a) the package area, b) the pitch of the I/Os on the package, c) the number of printed wiring board (PWB) routing layers, and d) the PWB device feature sizes. The first two of these factors determine the number of I/Os on the package and the remaining factors calculate the routability of these I/Os when the package is mounted/attached to the PWB for system assembly. To preserve the size, weight and performance advantages of CWLP and to provide the I/O density required by the application, an optimum balancing of these parameters must be achieved to assure that all of the I/Os on the CWLP are routed within its footprint on the PWB. The practical limits on the I/O density of chip scale packages are obtained when the I/Os on the package are equal to the I/Os routed on the PWB.

The objective of this paper is to develop an analytical model to describe the practical limitations on the I/O density of CWLP and to offer concrete solutions to apply CWLP to high I/O density products. We also explore the impact

of high density wiring, minimum feature sizes on off-chip speed, signal integrity, I/O current density, heat removal, and electrical properties of PWB materials.

Model Development

The number of I/Os routed by multi-layer PWB is primarily function of the PWB device feature sizes (i.e. size of I/O pads, via pads, signal traces, spacing, etc.), number of routing layers and the partition of these layers into routing regions on each level. To achieve high I/O density, the I/Os are distributed in an area array fashion on the package. For the purpose of this paper we assume an area array distribution of I/Os. An important condition to be satisfied when area array I/Os are routed on the PWB is to make sure that all of the inner I/Os escape to the edge of the routing regions. The model is developed under purview of this condition. A routing region is defined to be a region where the PWB devices are placed and routed. Given this we first calculate the number of I/Os routed on a single layer PWB and then extend the model to include multi-layer PWB design. The geometrical descriptions of devices on the PWB: the I/O pad, via pad and signal traces are shown in Figure 1.

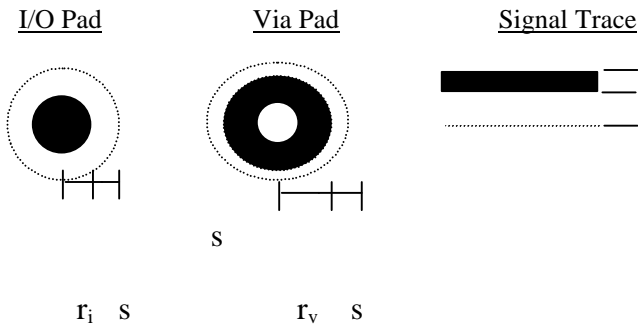


Figure 1: PCB device feature sizes

The I/O pads have radius, r_i , via pads have radius, r_v , the traces have thickness, t and s denotes the clearance spacing required by each devices. The package I/Os are connected to the I/O pads on the PWB; signal traces on PWB are used to route these pads to the periphery of the routing region

and via pads are used to connect the I/O pads to traces on another layer. Since all of the inner I/Os have to escape to the edge of the routing region, the number of traces or lanes that can be established on the periphery of the region will limit the I/Os routed in that layer. A channel is defined to be the space between two I/O pads and the number of lanes/traces that can be placed per channel is expressed as:

$$N_l = (P_p - 2r_i)/(t + s) \quad (1)$$

where P_p is the I/O pad pitch. Total number of channels, N_c , on one edge of the routing area, A , is:

$$N_c = (\sqrt{A}/P_p) - 1 \quad (2)$$

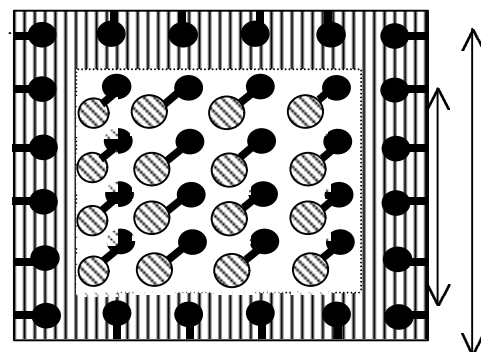
The first part of (2) calculates the number of pads on the edge and one is subtracted to yield the number of channels on the edge of the routing region. The number of I/Os routed in single layer is equal to:

$$N_{total} = 4[N_l N_c + (N_c + 1)] \quad (3)$$

$$P_p \geq 2r_i + s$$

The first part of (3) calculates the total number of traces placed on the edge of the board to access the inner I/O pads. The second part calculates the total number of pads placed on the edge. Summation of these two terms multiplied by four, to represent four sides, gives the number of I/Os routed in one layer PWB. The underlying condition for (3) is that the package pitch must be large enough to allow the placement of I/O pads. The failure of the condition set in (3) would suggest the inability to place the I/O pads on a layer. This is never the case in practical designs; the purpose of its inclusion is to provide the limits of operations when making future projections.

The next step is to extend the single layer model to multi-layer and calculate the number of I/Os routed by multi-layer PWB. The model is illustrated by Figure 2.



L_i L_o

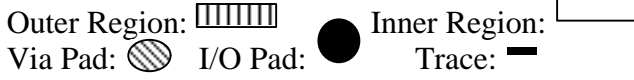


Figure 2: Multi-layer board modeling

The I/Os that can be routed in a layer are found from equation (3). The board layer is optimally partitioned in such a way that only those I/Os that can be routed in this layer are placed in the shaded region (outer region) and the rest are placed in the clear region (inner region) to be sent to next layer as permissible by the routing density of that layer. In this way we define the inner and outer routing region of a layer as shown in the Figure 2. This allows the accommodation of the maximum number of I/Os on the PWB. Furthermore to generalize the model to multi-layer PWB, we develop the model in terms of present and next routing layers. The present layer is denoted by the subscript, k , and the next layer is denoted by the subscript $k+1$. The total number of I/Os that can be placed in the outer region of k th layer, $N_{out,k}$, is:

$$N_{out,k} = \left\lfloor \frac{L_{o,k}^2 - L_{i,k}^2}{P_p^2} \right\rfloor \quad (4)$$

where $L_{o,k}$ is the outer region edge length and $L_{i,k}$ is the inner region edge length. Starting from layer 1, the outer region edge length, $L_{o,k}$, is simply equal to square root of the area available for routing. Therefore, the inner region routing length, $L_{i,k}$, is the only unknown in (4). Subsequently carrying this on to multiple board layers note that the outer region length is always known and the inner region length must be optimally determined to yield the maximum I/O density. We want, $N_{out,k}$, to be equal to the total number of I/Os routed in k th layer. This is found from substituting k th layer parameters in (3). We

denote total number of I/Os routed in k th layer as, Nt_k .

$$Nt_k = 4 \left\{ \left(\frac{P_p - 2r_i}{t + s} \right) \left(\frac{L_{o,k}}{P_p} - 1 \right) - \frac{L_{o,k}}{P_p} \right\} \quad (5)$$

This enables the calculation of the optimum inner region routing length, $L_{i,k}$ by setting Nt_k equal to $N_{out,k}$.

$$L_{i,k} = \sqrt{L_{o,k}^2 - Nt_k P_p^2} \quad (6)$$

The I/Os that are placed in the inner region, $N_{in,k}$, have to be routed in the $k+1$ layer and is given by:

$$N_{in,k} = L_{i,k}^2 / P_p^2 \quad (7)$$

However, as in the case of k th layer, there is a limitation to the number of I/Os that can be routed in $k+1$ layer denoted by, Nt_{k+1} , and found by substituting the new edge length, $L_{i,k}$, into (3).

$$Nt_{k+1} = 4 \left\{ \left(\frac{P_p - 2r_i}{t + s} \right) \left(\frac{L_{i,k}}{P_p} - 1 \right) - \frac{L_{i,k}}{P_p} \right\} \quad (8)$$

If the I/Os placed in the inner region of k th layer, $N_{in,k}$, is less than the I/Os routed in $k+1$ layer, Nt_{k+1} , then it is useless to go to higher board layers since there will not be any I/Os to route. If, however, Nt_{k+1} is less than $N_{in,k}$ then similar strategy, as discussed above, is used to design the optimum partition between successive layers. This is repeated until two of the following situation occurs: i) we exceed the total number of routing layer and ii) the I/Os placed in the inner region is less than the I/Os routed in the next available layer. The total number of I/Os accommodated by the multi-layer board, N_{total} , is finally expressed as:

$$N_{total} = \sum_{k=1}^n Nt_k \quad ; \quad N_{in_k} \geq Nt_{k+1} \quad (9)$$

$$N_{total} = N_{in_k} + \sum_{k=1}^n Nt_k \quad ; \quad N_{in_k} < Nt_{k+1} \quad (10)$$

$$P_p \geq 2(r_i + r_v + s)$$

where n is the total number of routing layers. Equation 9 is valid for cases where the I/Os placed in the inner region of k th layer is greater than or equal to the number of I/Os routed in $k+1$ layer. In the reverse situation, (10) becomes valid and availability of greater board layers does not

give more I/O density on the printed circuit board. The condition underlying these derivations is that the pad pitch must be large enough to allow the placement of via and I/O pads. So for given number of board layers, we have developed a very simple model that can calculate the maximum number of I/Os supported by that board under practical considerations. By placing the capability of PWB under the constraint of area and terminal pitch of CWLP, the limit on the I/O density of CWLP can be obtained. The CWLP area is equal to the area of the chip. The package terminal pitch is obtained as projected in the NTRS [2].

PWB I/O Density

We apply the model to study the impact of package area, terminal pitch, number of PWB routing layers and the PWB device feature size on the limit on the I/O density of chip scale packages. The limits on the I/Os routed on the board and, in turn, the limits on the I/O density of CWLP as function of layers and feature size are plotted in Figure 3. The layers are varied from 1 to 5 and the PWB trace thickness, t , is varied from 6 mils (0.15mm) to 4 mils (0.10mm) to 2 mils (0.05mm) acknowledging existing commodity, leading edge and state-of-the-art technologies, respectively. The package terminal pitch, P_p , is scaled from 1.27mm to 0.8mm to 0.5mm, respectively. Table 1 lists the device sizes as used in the analysis.

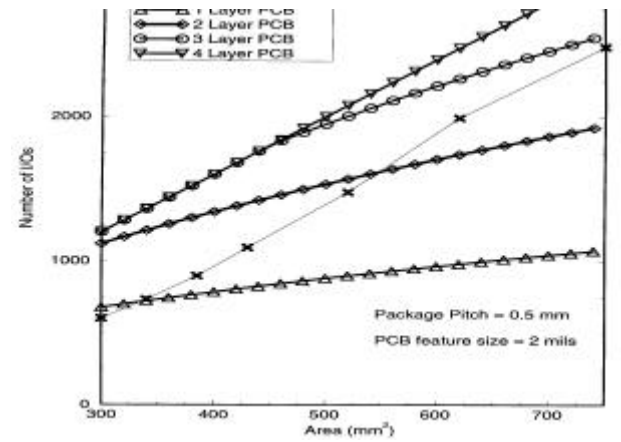
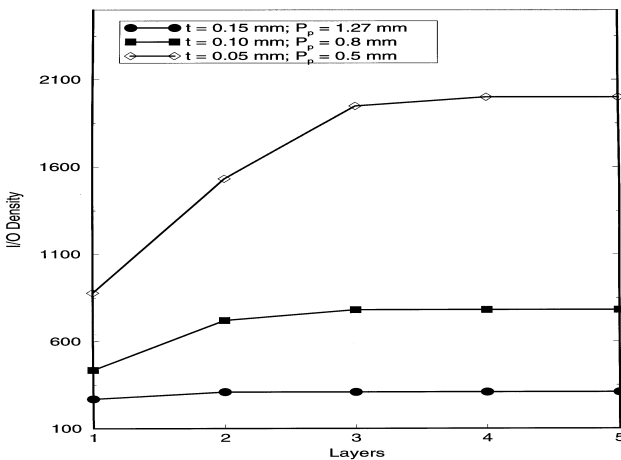


Figure 3: I/Os as a function of number of board layers

Table 1: PCB Device Feature Sizes

Devices	Size
Trace (t)	t
I/O pad (r_i)	t
Via pad (r_v)	$2t$

For a specific PWB technology, Figure 3 gives the limits on the I/O density of CWLP. As an example, for leading edge technology (0.10mm), this limit is determined to be roughly 750 I/Os for 500 mm² CWLP area and 0.8 mm CWLP terminal pitch. The limit depends on the number of board layers used. The density increases with the increase in the board layer and it is held constant as the number of I/O pads placed on the surface of the PWB (function of t , P_p) is less than the number of I/Os routed in specified layers. And therefore the availability of higher number of board layers does not increase its I/O density since there are no I/Os to route. Higher densities can only be achieved by two means: a) scaling down the feature size and b) decreasing the pad pitch. This is shown in the third curve where state-of-the-art PWB technology (0.05mm) is used along with smaller pad pitch (0.5mm) to yield a new limit of roughly 2000 I/Os. One can always scale down the feature size if permitted by progress in technology, however, the scaling down of pad pitch is limited with respect to the feature size. From (3) and (9) we know that the pad pitch has to be large enough to allow the placement of via and I/O pads. The limit on the



pad pitch can be calculated using the values tabulated in Table 1.

Figure 4: I/O Density limits with respect to NTRS Projections

Increasing the area of CWLP to achieve higher I/O density is not an available option since this will be counter productive to the use of chip scale packages. Figure 4 analyzes the limits with respect to the I/O projections of the NTRS for cost/performance sector.

The I/O projections are plotted as a function of chip area. The limits on the I/O density of CWLP depending on the number of board layers, the state-of-the-art PWB technology, and terminal pitch of 0.5mm is also plotted. For CWLP to meet the I/O projections of cost/performance market, technologies that yield curves above the NTRS curve has to be used. Specifically, this means using more than two board layers in our example. Subsequently, we can address the applicability of CWLP to various technology markets and generate accurate technology parameters needed to meet the I/O density requirements of these applications.

Impact of High Density PWB on Performance:

We have thus far analyzed the need of high density PWB from the perspective of high I/O chip scale and Compliant Wafer Level Packages. Very careful analysis and survey of advances in the printed wiring board technologies show that the PWB industry is able to meet the high I/O density requirement of high performance electronic product [3]. It is an interesting question to study the implication of minimum feature size PWB design on electrical performance. We qualitatively examine various issues in the realm of high density PWB.

I. Off-chip speed:

The prime advantage of chip size packages is that they require very small footprint on the PWB. This allows one to place them much closer to

each other and achieve very high chip to chip speed. Ideal situation would “tile” these packages to achieve maximum off-chip speed. With the use of CWLP where package parasitics are negligible [1], tiling can provide off-chip speeds that are close to on-chip clocking frequencies.

II. Signal Integrity/Conductor Width

As more wiring densities are sought, electrical signal integrity is bound to become a dominant issue in the design of future PWB. Inductive and capacitive coupling between lines will induce cross talk and high switching noises. To minimize these noises, low self-inductance and interline capacitance and inductance must be achieved by means of shifting to lower dielectric materials. Low dielectric materials not only improve the transitional characteristics of signal lines, they improve the density by allowing to reduce the width and spacing between conductor lines. Multilevel boards are inevitable and so are the problems that come with it. Furthermore, smaller feature lines increase the current density of conductors that may approach their limit. As far as performance of the high density PWB is concerned, very strong attention has to be paid to electronic materials. We may have to move from traditional epoxy to high performance polymers. The industry is already searching for an alternative in low-k dielectrics such as BCB.

III. Heat Removal

Heat removal from multilevel PWB will become more complex as these boards are used for chip size packages. The power density will shoot up since the footprint of these packages will be the same as the semiconductor chip, limiting the size of PWB. However, there may be hope since more wiring also means more thermal conduction paths and hence lower thermal resistance. We may not be far from the idea of cooling the back side of the PWB.

Conclusion:

We have examined the I/O density and performance issues surrounding high density

PWB design for high I/O Compliant Wafer Level Packages. The I/O densities required by future chip size packages will be met by the printed wiring board and new innovations in board fabrication material must take place to sustain electrical and thermal performance.

References:

1. C. S. Patel, "Compliant Wafer Level Package (CWLP)," *Semiconductor Packaging Symposium*, SEMICON West, July 1999.
2. 1997 National Technology Roadmap for Semiconductors.
3. C. S. Patel, S. Ogitani, P. Kohl, K. P. Martin, J. D. Meindl, "An Analysis of the Gap between PWB Technology and Chip I/O Interconnect Technology, and a New Wafer-Level Batch Packaging Concept," *to appear in 32nd International Symposium on Microelectronics (IMAPS)*, October 1999.