

Compact Physical IR-Drop Models for GSI Power Distribution Networks

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Abstract

The supply voltage decrease and power density increase of future GSI chips demands accurate models for the IR-drop voltage. Compact physical IR-drop models are derived for two types of packages. These models help designers estimate the required amount of interconnects and package pins which need to be dedicated for power distribution. Comparison with SPICE simulations show less than 1% and 5% error for the wire-bond package and the area-array package, respectively.

I. Introduction

IR-drop voltage is the voltage drop in the power distribution network because of the current passing through the resistances of the power distribution grid of the chip. As technology advances the power dissipation in GSI chips increases which results in higher current densities [1]. The tolerable IR-drop, however, decreases for future technologies because of lower supply voltages. The IR-drop, therefore, is becoming more serious as technology advances. The amount of IR-drop which can be tolerated determines the amount of wiring resources and the number of package pins which need to be dedicated to power distribution. Hence, designers need a simple and accurate model for IR-drop voltage to be able to design the power distribution network in the early stages. This model also enables them to predict the number of power/ground I/O's that a package should have for a target IR-drop. Currently, wire-bond and area-array packages are commonly used. In a wire-bond package, power and ground are distributed through a ring surrounding the chip and in an area-array package the power is provided from power and ground pins which are distributed on the chip. Previously, different models have been introduced, however, they are either curve fitting or limited in accuracy [2], [3]. In this paper, a partial differential equation is rigorously derived for power grid voltage, and then solved for two types of packages, the wire-bond package and the area-array package, and finally, the models are compared to SPICE simulations.

II. Partial differential equation of the power distribution grid

The power is distributed across the chip through a two-metal-level grid network made of horizontal and vertical global wires that are connected by vias. Fig. 1 shows the power distribution network on a GSI chip.

The number of segments of the grid is usually large; therefore, the power distribution grid can be modeled as a continuous planar surface which distributes power across the chip. Each node of the power distribution grid is connected to the four neighboring nodes as shown in Fig. 2.

The voltage of each node can be calculated from the voltage of the four neighboring nodes as

$$\frac{V_{IR}(x,y) - V_{IR}(x+\Delta x,y)}{R_0 \frac{\Delta x}{\Delta y}} + \frac{V_{IR}(x,y) - V_{IR}(x,y+\Delta y)}{R_0 \frac{\Delta y}{\Delta x}} + \frac{V_{IR}(x,y) - V_{IR}(x-\Delta x,y)}{R_0 \frac{\Delta x}{\Delta y}} + \frac{V_{IR}(x,y) - V_{IR}(x,y-\Delta y)}{R_0 \frac{\Delta y}{\Delta x}} = -I_0 \cdot \Delta x \cdot \Delta y \quad (1)$$

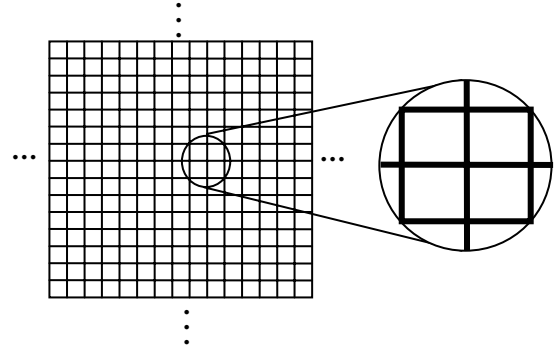


Fig.1. Power Distribution grid of the chip.

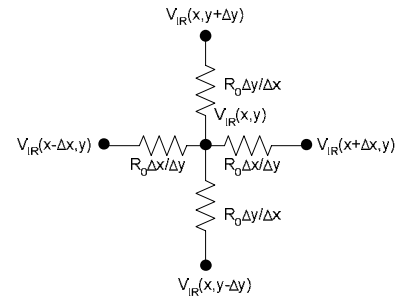


Fig.2. Differential model for a node in the grid.

where R_0 is the segment resistance, and I_0 is current density. Replacing each of the neighboring voltages with their Taylor series, and simplifying it we have

$$\frac{\partial^2 V_{IR}(x, y)}{\partial x^2} + \frac{\partial^2 V_{IR}(x, y)}{\partial y^2} = R_0 I_0, \quad (2)$$

which can be rewritten as

$$\nabla^2 V_{IR}(x, y) = R_0 I_0. \quad (3)$$

The IR-drop voltage for different packages can be calculated applying the appropriate boundary condition to this partial differential equation (3). In the following sections this equation is solved for two types of packages.

III. IR drop for a wire-bond technology package with a power ring

In this kind of package, the pins are connected with wire-bonds to a power ring surrounding the chip. Hence, IR-drop is zero at the power ring. The boundary condition for this case is as shown in Fig. 3. Solving the partial differential equation with the boundary condition shown in Fig. 3 results in

$$V_{IR}(x, y) = \frac{16 \cdot R_0 \cdot I_0}{\pi^4} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left(\frac{(2k+1)\pi}{a} \cdot x\right) \sin\left(\frac{(2l+1)\pi}{b} \cdot y\right)}{(2k+1)(2l+1) \left(\frac{(2k+1)^2}{a^2} + \frac{(2l+1)^2}{b^2}\right)} \quad (4)$$

where a and b are the sizes of each side of the ring, R_0 is the resistance of each segment, and I_0 is current density. The IR-drop voltage is shown in Fig. 4. As shown in Fig. 4, the maximum voltage drop is at the center of the chip. The maximum IR-drop voltage, therefore, can be calculated from

$$V_{IR_{max}} = V_{IR}\left(x = \frac{a}{2}, y = \frac{b}{2}\right) \quad (5)$$

For the case that the chip is square ($a=b$), IR-drop is equal to

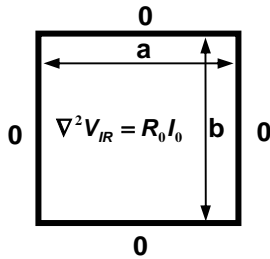


Fig 3. Boundary condition for wire-bond package with a power ring.

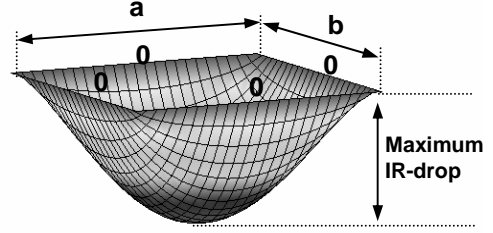


Fig. 4. IR-drop voltage of the wire-bond package.

$$V_{IR}(x, y) = \frac{16 \cdot R_0 \cdot I_0 \cdot a^2}{\pi^4} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left(\frac{(2k+1)\pi}{a} \cdot x\right) \sin\left(\frac{(2l+1)\pi}{a} \cdot y\right)}{(2k+1)(2l+1) \left((2k+1)^2 + (2l+1)^2\right)} \quad (6)$$

The maximum IR-drop can be simplified for the square chip and is equal to.

$$V_{IR}\left(x = \frac{a}{2}, y = \frac{a}{2}\right) = 0.0736 \cdot R_0 \cdot I_0 \cdot a^2 \quad (7)$$

SPICE Simulations show that the results have less than 1% error.

VI. IR drop for area-array package

In an area-array package, I/O pads are distributed across the chip. Fig. 5 shows the power and ground pads for an area-array package. Assuming a constant current density in each region, the area between each four pads is the same. Hence, the partial differential equation needs to be solved for the area between four neighboring pads called a cell which is shown shaded in Fig. 5. A single cell is shown in detail in Fig. 6.

If current is uniform, no current passes through the cell borders; therefore, the boundary condition is as shown in Fig. 7.

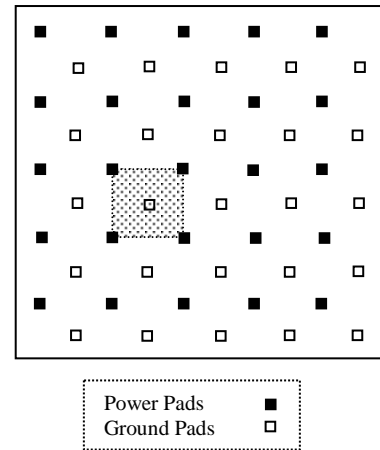


Fig. 5. Power and ground pads for an area-array package.

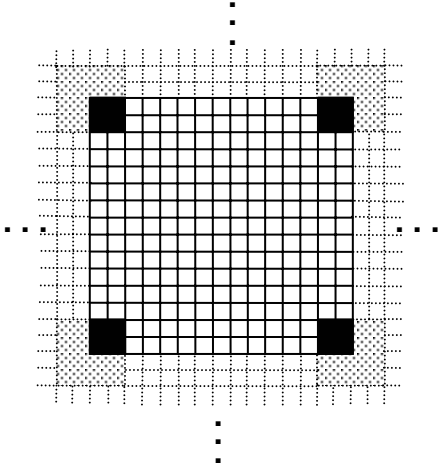


Fig. 6. Grid between four neighboring pads.

The partial differential equation with the boundary condition shown in Fig. 7 can be divided to two partial differential equations with boundary conditions as shown in Fig. 8. The IR-drop voltage can be calculated from

$$V_{IR} = u_1 + u_2, \quad (8)$$

where u_1 and u_2 are the solutions of the partial differential equations shown in Fig. 8. The IR-drop voltage for this case is shown in Fig. 9. As shown in Fig. 9 the maximum IR-drop voltage happens at the center of the cell. Solving the partial differential equation rigorously and simplifying results in a simple analytical equation for the IR-drop

$$V_{IR} = \frac{R_0 I_T}{2\pi} \ln\left(\frac{0.65 \cdot N}{M}\right), \quad (9)$$

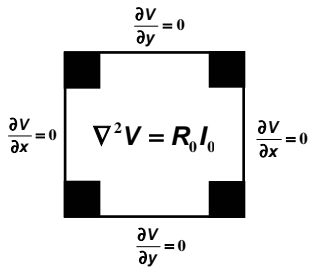


Fig. 7. Boundary condition for each region surrounded by four pads.

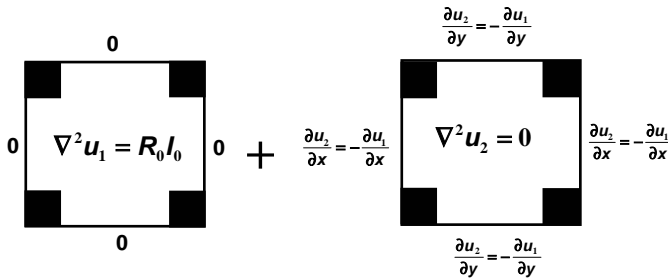


Fig. 8. Equivalent partial differential equations with boundary conditions for an area-array package.

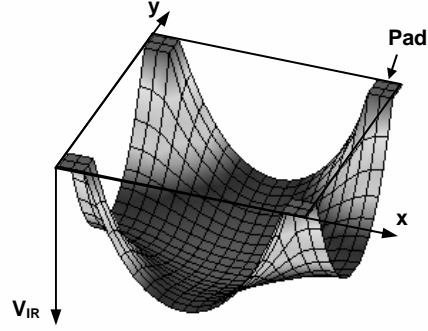


Fig. 9. IR-drop voltage of the area-array package.

where R_0 is the segment resistance, I_T is the current distributed by a pad, N is the number of segments between two pads, and M is the size of the pad in segment units. SPICE simulations show that the results have less than 5% error.

For the case that a pad is connected to only one node of the grid, the IR-drop is equal to

$$V_{IR} = \frac{R_0 I_T}{2\pi} \ln(1.931 \cdot N), \quad (10)$$

which agrees with the model derived in [3] through curve fitting. The maximum error for this case is less than 1%.

V. Conclusion

Compact physical models for IR-drop voltage are presented to enable designers to predict the amount of resources which are needed for the power distribution in the early stages of the design. A partial differential equation is developed for voltage of the power distribution grid and solved rigorously to find physical IR-drop models for two types of packages, wire-bond and area-array packages. SPICE simulations show that the models have less than 1% and 5% error for wire-bond and area-array packages, respectively. The implications of these new models for the power distribution networks of future ASIC generations as projected by International Technology Roadmap for Semiconductors (ITRS) will be presented.

References

- [1] Semiconductor Industry Association, "International Technology Roadmap for Semiconductors (ITRS)," 2001.
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- [3] J. W. Joyner, J. D. Meindl, "A Compact Model for Projection of the Future Power Supply Distribution Network Requirements," Asic/SOC Conference, pp. 376-380, September 2002.