

Optimum Chip Clock Distribution Networks

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Abstract

Clock skew, clock signal degradation (attenuation) and power dissipation are the three main concerns in designing a chip clock distribution network. Two new design planes, utilizing compact models for clock skew, clock signal degradation and power dissipation are proposed. An example of a 0.18 μm CMOS technology shows that the maximum clock frequency of 610 MHz for a typical $2 \times 2 \text{ cm}^2$ chip design, can be achieved by using 4 levels of H-tree.

I. Introduction

In high-speed digital systems, clock distribution is a challenging problem consuming an increasing fraction of resources such as design time, power, and wiring [1]. Three main conditions must be satisfied for a clock distribution network to be selected for a design: (1) clock skew, (2) clock signal degradation, and (3) clock power dissipation. A combination set of the three criteria in a design plane is used to optimize the clock distribution network.

A compact model of clock skew consisting of all device, interconnect, and system parameter variations [2], is used here to define the first criterion. The compact model for clock skew is reviewed in Section II. The second basis is clock signal degradation which is defined by interconnect bandwidth. A simplified model for clock signal degradation is discussed in Section III. Finally the power dissipation model for clock distribution network, as the third criteria, is described in Section IV. Section V illustrates the interconnect design plane using the above conditions. An example of a clock distribution network design using 0.18 μm CMOS technology is also investigated.

II. Clock Skew Model

Clock skew, by definition, is the variation of timing signal delay in the clock distribution network. In a balanced clock tree (BCT) structure, the nominal value for clock skew is asymptotically zero, since the clock path lengths from the source to the sinks are equalized. In this case, clock skew reduces to the variations of the clock path from

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the clock generator to the registers. These variations may originate from process and circuit parameter tolerances, which are codified hereafter.

A. Device Parameter Variations

In the IC fabrication process, all device parameters are subject to deviations from their nominal values. Statistical models have been developed for transistor parameter deviations such as threshold voltage (ΔV_T), gate oxide thickness (Δt_{ox}), and effective channel length (ΔL_{eff}) [4].

B. Interconnect Parameter Variations

Interconnect width (ΔW_{int}) and thickness (ΔH_{int}) and interlevel dielectric (ILD) thickness (ΔT_{ILD}) variations are the main parameters of interest. Although using chemical mechanical polishing (CMP) greatly reduces the metal and ILD non-uniformity in multi-layer structures, metal dishing and oxide erosion are still vexing issues, which create ILD and interconnect thickness variations even after CMP.

C. System Parameter Variations

Besides process parameter variations, which are mainly the tolerances of device and interconnect physical parameters, system level fluctuations may create clock skew. Power supply voltage fluctuation (IR drop, ΔV_{DD}), temperature variations (ΔT), and non-uniform distribution of clocked registers (clock driver load mismatch, ΔC_L) are considered as system level parameter variations.

In order to derive the compact model for clock skew, a simplified equivalent circuit of a balanced clock distribution network is examined as illustrated in Fig. 1. As shown, the delay of the entire clock network can be written as:

$$T_{Delay} = T_{H-Tree} + T_{Driver} + T_{Sub-Blk} \quad (1)$$

where T_{H-Tree} , T_{Driver} , and $T_{Sub-Blk}$ are signal delay of H-Tree global clock distribution, clock driver delay, and sub-block routing delay, respectively. The total delay is, then, given by [2]

$$T_{Delay} \approx 0.4 \left(\frac{\rho \cdot \epsilon_r}{H_{int} \cdot T_{ILD}} \right) \cdot D^2 \left(1 - \frac{1}{2^{n/2}} \right)^2 + \frac{\sqrt{\epsilon_r}}{c_o} \cdot D \left(1 - \frac{1}{2^{n/2}} \right) + 0.7 \left(\frac{L_{off}/W}{\mu \cdot C_{ox} (V_{DD} - V_T)} \right) \cdot C_L \quad (2)$$

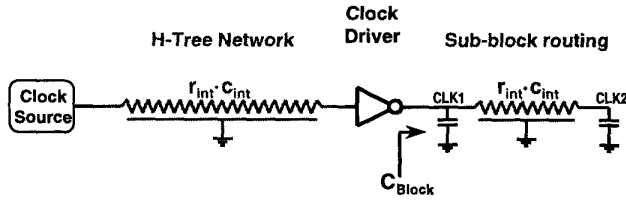


Fig. 1 Equivalent circuit of a balanced clock tree network

where D is the die size, n is the number of branch levels of an H-tree as defined in [3], c_0 is the speed of light in free space, ρ is the line conductor resistivity, ϵ_r is the relative dielectric constant of the ILD material, and μ is the MOSFET channel carrier mobility. Other parameters are defined in Table I. Equation (2) contains all device, interconnect, and system parameters. Assuming that these parameters have small variations compared to their nominal values, the clock skew, T_{CSK} , can be evaluated by

$$T_{CSK}(x) = \Delta T_{Delay} = \left| \frac{\partial T_{Delay}}{\partial x} \right| \Delta x \quad (3)$$

where T_{Delay} is the complete delay function of (2), and x is any variation of clock skew components such as ΔH_{int} , ΔT_{ILD} , ΔV_{DD} , ΔV_T , Δt_{ox} , ΔL_{eff} , and ΔC_L . The complete closed form expressions for clock skew components, which are discussed in detail in [2], are summarized in Table I. Therefore the overall clock skew is given by

$$T_{Sub-Blk} = 0.4(r_{int}c_{int})\frac{D^2}{2^n} + \frac{\sqrt{\epsilon_{r,ox}}}{c_0} \frac{D}{2^{n/2}} + \sum_i \left| \frac{\partial T_{Delay}}{\partial x_i} \right| \Delta x_i \quad (4)$$

TABLE I. CLOCK SKEW COMPONENTS

Physical Parameter and Derivation Used		Clock Skew Compact Model
ILD Thickness Variation	$\left \frac{\partial T_{Delay}}{\partial T_{ILD}} \right $	$T_{CSK}(T_{ILD}) = 0.4(r_{int}c_{int}) \cdot D^2 \left(1 - \frac{1}{2^{n/2}}\right)^2 \left(\frac{\Delta T_{ILD}}{T_{ILD}}\right)$
Wire Thickness Variation	$\left \frac{\partial T_{Delay}}{\partial H_{int}} \right $	$T_{CSK}(H_{int}) = 0.4(r_{int}c_{int}) \cdot D^2 \left(1 - \frac{1}{2^{n/2}}\right)^2 \left(\frac{\Delta H_{int}}{H_{int}}\right)$
Threshold Voltage Fluctuation	$\left \frac{\partial T_{Delay}}{\partial V_T} \right $	$T_{CSK}(V_T) = 0.7R_p C_L \left(\frac{V_T}{V_{DD} - V_T}\right) \left(\frac{\Delta V_T}{V_T}\right)$
Transistor Channel Length Tolerance	$\left \frac{\partial T_{Delay}}{\partial L_{eff}} \right $	$T_{CSK}(L_{eff}) = 0.7R_p C_L \left(\frac{\Delta L_{eff}}{L_{eff}}\right)$
Gate Oxide Thickness Tolerance	$\left \frac{\partial T_{Delay}}{\partial t_{ox}} \right $	$T_{CSK}(t_{ox}) = 0.7R_p C_L \left(\frac{\Delta t_{ox}}{t_{ox}}\right)$
IR Drop	$\left \frac{\partial T_{Delay}}{\partial V_{DD}} \right $	$T_{CSK}(V_{DD}) = 0.7R_p C_L \left(\frac{V_{DD}}{V_{DD} - V_T}\right) \left(\frac{\Delta V_{DD}}{V_{DD}}\right)$
Non-uniform Register distribution	$\left \frac{\partial T_{Delay}}{\partial C_L} \right $	$T_{CSK}(C_L) = 0.7R_p C_L \left(\frac{\Delta C_L}{C_L}\right)$
Temperature gradient	$\left \frac{\partial T_{Delay}}{\partial T} \right $	$T_{CSK}(T) = 0.7R_p C_L \left(\frac{E_A/q + V_T}{V_{DD} - V_T}\right) \left(\frac{\Delta T}{T}\right)$
Internal Clock Skew	—	$T_{CSK}(internal) = (r_{int}c_{int})\frac{D^2}{2^n} + \frac{\sqrt{\epsilon_{r,ox}}}{c_0} \frac{D}{2^{n/2}}$

where the first and second terms are often called *internal clock skew* [3] which is the time difference between CLK1 and CLK2 in the sub-block circuit as shown in Fig. 1. The third term in (4) is the summation of all skew components shown in Table I.

III. Clock Signal Degradation Model

The resistance and capacitance of on-chip wires create a limit on the maximum wire length for given frequency due to interconnect bandwidth. An interconnect can be modeled as an RC low-pass filter with the bandwidth

$$f_{-3dB} = \frac{1}{2\pi(r_{int}c_{int}) \cdot l^2} \quad (5)$$

where r_{int} and c_{int} are the distributed resistance and capacitance per unit length of the interconnect, and l is the length of the line. An example of the frequency response of the clock wiring structure for three distinct lengths is depicted in Fig. 2. It is observed that the maximum clock frequency for a 2cm line, in this example, is limited to about 350MHz. Using the expression for the length of the H-tree versus die size, D , and the number of H-tree levels, n , defined in [3], then (5) becomes

$$f_{-3dB} = \frac{1}{2\pi(r_{int}c_{int}) \cdot D^2 \left(1 - \frac{1}{2^{n/2}}\right)^2} \quad (6)$$

IV. Clock Power Dissipation Model

The total power dissipation of a clock distribution network is assorted into three parts: i) clock wiring capacitance, ii) clock driver capacitance, and iii) clock loading capacitance. The simplified expression for clock power dissipation is

$$P_{Clock} = f_c V_{DD}^2 \left(\frac{\epsilon_{ox} \cdot \epsilon_r \cdot W_{Leq} \cdot D}{T_{ox}} \cdot (2^{n+1} + \sqrt{N_{FF}}) + 2^n C_{Driver} + N_{FF} C_{FF} \right) \quad (7)$$

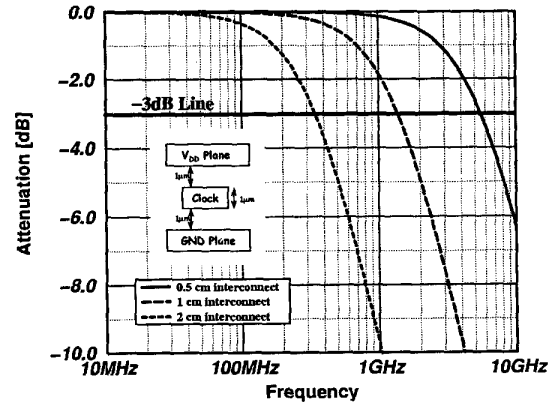


Fig. 2 Interconnect frequency response and bandwidth

where W_{leaf} is the width of the last branch of the H-tree, n is the number of branch levels of the H-tree, C_{Driver} is the clock driver input capacitance, N_{FF} is the number of clocked registers (or Flip-Flops), and C_{FF} is the input capacitance of a clocked register.

V. Design Plane for Optimum Clock Distribution

Assuming that clock skew is 10% of clock cycle time, the clock frequency can be computed from $f_c = 0.1/T_{CSK}$, where T_{CSK} is given in (4). Using the data of Tables II and III, which are provided by [2], a plot of clock frequency versus number of H-tree levels for the clock skew criterion is depicted in Fig. 3. Similarly, using (6), the clock signal degradation criterion is represented in the same graph. Then, the optimum number of H-tree levels, $n=4$, and the maximum achievable clock frequency, $f_c=610$ MHz, is given by the intersection of the two criteria. In order to have a symmetric clock distribution network, only the even number of H-tree levels are allowable. Figure 3 also shows that the ultimate clock frequency is limited by process and design variations. This case can be achieved by reducing the interconnect attenuation through utilizing repeaters in the clock distribution network.

The clock power dissipation for the case of study is depicted in Fig. 4. As shown the clock power dissipation increases dramatically by increasing the number of H-tree levels beyond six.

VI. Conclusion

Clock distribution networks are characterized by three main criteria of clock skew, clock signal degradation, and power dissipation. Compact models for the three criteria are derived. Based on the compact models, a new design plane for a clock distribution network is presented. Utilizing the new design plane, the maximum clock frequency, the optimum number of H-tree levels, and the ultimate clock frequency can be computed for any technology generation. An example of a 0.18 μm CMOS technology shows that the maximum clock frequency of 610 MHz for a typical $2 \times 2 \text{ cm}^2$ chip design, can be achieved by using 4 levels of H-tree.

TABLE II. PROCESS AND DESIGN PARAMETERS

Parameters		Values
Process Parameters	L_{eff}	0.18 [μm]
	V_T	0.32 [V]
	V_{DD}	1.8 [V]
	$r_{int}C_{int}$	115 [ps/cm^2]
Design Parameters	R_{tr}	12.0 [Ω]
	C_L	6.25 [pF]
	D	2.0 [cm]

TABLE III. PROCESS AND DESIGN VARIATIONS

Parameters	% of Variations	Parameters	% of Variations
T_{ILD}	3%	t_{ox}	1.2%
H_{int}	3%	V_{DD}	10%
V_T	5%	C_L	20%
L_{eff}	5%	T	8%

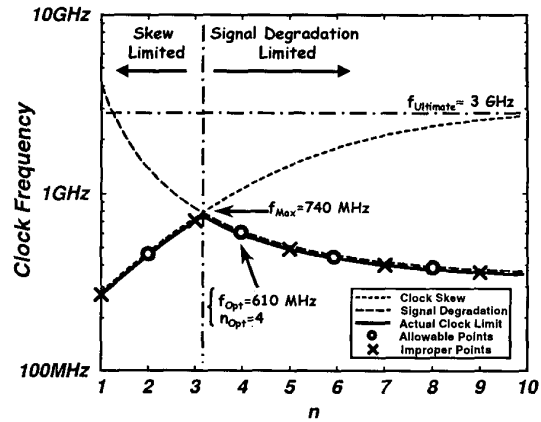


Fig. 3 Design plane for clock distribution networks

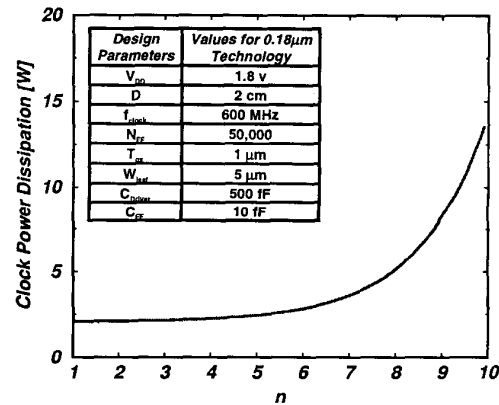


Fig. 4 Clock power dissipation versus n

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