

Asymptotically Zero Power Dissipation Gigahertz Clock Distribution Networks

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Abstract

A novel global clock distribution network design with zero asymptotic power dissipation for the GHz frequency range is proposed. Power dissipation and clock skew of the new global clock distribution network are analyzed. A simple experiment on a transmission line, as a scaled model of a clock distribution network, demonstrates a 97% reduction in power dissipation.

Introduction

Clock distribution has become an increasingly challenging problem for digital systems. As clock frequency continues to increase toward the GHz range, a large percentage of chip power dissipation is due to the clock distribution network. For example, the 300 MHz Alpha microprocessor clock consumes 20 W, which is about 40% of the total chip power dissipation [1]. Since by technology developments device size shrinks while chip size enlarges, interconnect capacitance in global clock distribution networks becomes more dominant compared to gate input capacitance [2]. Therefore reducing the power dissipation of clock distribution networks can significantly reduce the overall system power consumption.

In order to enhance clock distribution performance and reduce power dissipation, a global clock distribution based on low loss package interconnect has been proposed in [3]. Using low resistance off-chip global clock distribution networks that are driven with fast transition times of clock signals, leads to treating clock interconnects as ideal transmission lines. A salient property of transmission lines is used here to asymptotically eliminate global clock wiring power dissipation. Compact models for power dissipation, and clock skew for the new clock distribution network are derived. To verify the method, the results of a simple experiment are presented.

Asymptotically Zero Wiring Power Dissipation

It has been shown previously that the most efficient method for driving transmission lines in CMOS circuits is the source end termination, which eliminates dc power dissipation [4]. However, as depicted in Fig. 1, power is still consumed within the transition of period $2t_f$, where t_f is the ideal transmission line time of flight. As $2t_f$ becomes closer to the pulse width (half of the clock period), the power dissipation becomes more significant.

If the interconnect length is designed such that the reflected clock pulse, after $2t_f$, arrives at the source precisely at the beginning of the next clock period, then the power dissipation is reduced to zero. This is because the energy for each clock period is virtually provided by the reflected pulse from the previous clock period as shown in Fig. 2. This advantage is achieved when the following condition is obtained:

$$\text{Supported by the SRC through RPI (subcontract):} \quad \ell = \frac{c_o}{2f_c \sqrt{\epsilon_r}} \quad (1)$$

where ℓ is the interconnect length, c_o is speed of light in free space, f_c is the clock frequency, ϵ_r is the dielectric constant of the insulator,

and n is any integer number. For example at 3GHz clock frequency, the best length for on-package clock distribution wires in Alumina media ($\epsilon_r=9.5$) is 1.6 cm, which is in the range of contemporary microprocessor die size.

The length of clock interconnect can be adjusted to ℓ by using balanced clock tree (BCT) structure shown in Fig. 3. Figure 3-a illustrates a global clock distribution network supplying four points of the chip utilizing on-package multilevel interconnects. In order to prevent radiation from clock wires, a ground shielding is provided by power supply distribution network as shown in Fig. 3-b.

Clock Skew Analysis

Clock skew, by definition, is the variation of timing signal delay in the clock distribution network. For off-chip global clock distribution of Fig. 3, the delay is

$$T_{Delay} = t_f = \ell \sqrt{lc} \quad (2)$$

where l and c are the wiring inductance and capacitance per unit length respectively. Due to variations of interconnect dimensions and non-uniform return paths, clock delay variations arise. Assuming small variations for l and c , clock skew can be expressed as a derivative of (2), which is

$$T_{CSK} = \frac{\partial T_{Delay}}{\partial l} \Delta l + \frac{\partial T_{Delay}}{\partial c} \Delta c = \frac{1}{2} \left(\frac{\Delta l}{l} + \frac{\Delta c}{c} \right) \cdot \ell \sqrt{lc} \quad (3)$$

where $\Delta l/l$ and $\Delta c/c$ are the relative variations of inductance and capacitance in clock distribution network. Using the ground shielding of Fig. 3, reduces $\Delta l/l$ and $\Delta c/c$ resulting in a very small clock skew.

Power Dissipation Analysis

Although the nominal wiring power dissipation is designed to asymptotically approach zero, non-ideal effects cause power consumption. Figure 4 shows a SPICE simulation to illustrate the impact of non-ideal effects on clock power dissipation. In this figure, (b) shows the ideal case of source current compared to clock pulse waveform, (a), using the typical parameters given by Table I. The source current waveforms (c), (d), and (e) are for the cases of 2.2 dB/cm lossy line ($r=25 \Omega/\text{cm}$), 10% mismatch of wire length ($\ell=1.1\text{cm}$), and 50 fF loading capacitance, respectively.

Assuming a small deviation from the ideal case, the expression for total clock power dissipation is derived as

$$P \approx \frac{V_{dd}^2}{16R_s} (1 - e^{-R_m/Z_o})^2 + \frac{V_{dd}^2 f_c}{R_s} \cdot \mathbf{D}_f + C_l V_{dd}^2 f_c \quad (4)$$

where the first, second and third terms represent the impact of wiring loss, deviation of time of flight from nominal value, and capacitance loading at the end of the line, respectively. In (4), R_{int} is the total line resistance, Z_o is the line characteristic impedance, R_s is the source termination resistance, and C_l is the load capacitance which is the input capacitance of a sub-block clock driver.

Experimental Results

The feasibility of the new clock distribution network is investigated by building an up-scaled model using a 30m long coaxial cable with 50Ω characteristic impedance. Figure 5 illustrates the measurement results where Ch1 and Ch2 are connected to the source and near end nodes, respectively. M1 is the voltage across source termination resistor ($M1=Ch1-Ch2$) that is proportional to source current.

For the case of $T_c=2t_f=320\text{ns}$ shown in Fig. 5-a, the source current is 3.36mA which results in a power dissipation of 0.56mW . Using a conventional criterion of $2t_f=0.1T_c=32\text{ns}$ [3] shown in Fig. 5-b, the source current is 25.6mA and power dissipation is 32.8mW . Therefore a 97% reduction in power dissipation is achieved by the new design method.

Conclusion

Based on recycling the energy of reflected pulses in transmission lines, an asymptotically zero power dissipation clock distribution network is proposed. Compact models for power dissipation and clock skew are derived. A simple experiment, by building an up-scaled model, demonstrates a 97% reduction in power dissipation.

References

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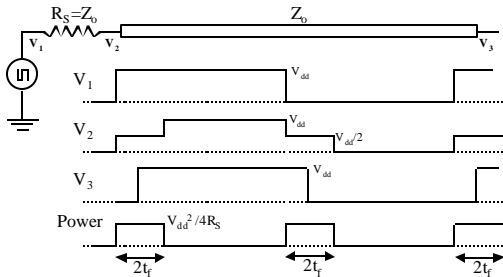


Fig. 1 Power dissipation in source termination transmission line

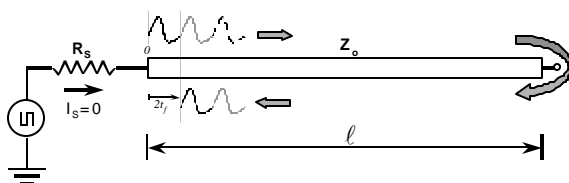


Fig. 2 Recycling the reflected clock pulse energy

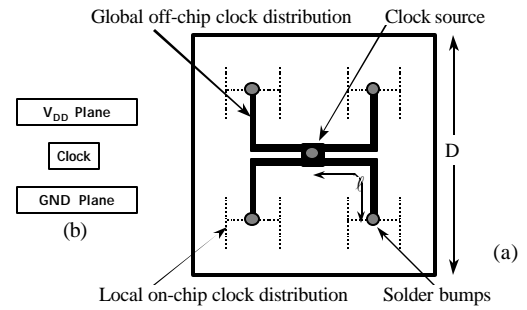


Fig. 3 Global clock distribution structure using BCT

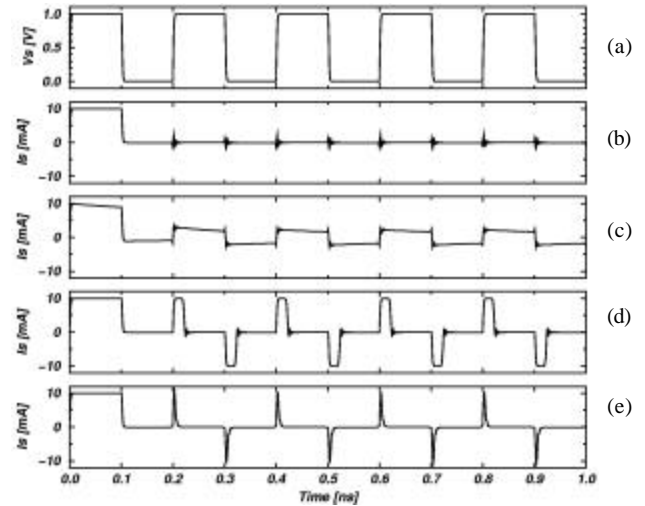


Fig. 4 The impact of non-ideal effects modeled with SPICE

TABLE I. PARAMETERS USED IN SPICE SIMULATION

$r = 1 \quad \Omega/\text{cm}$	$l = 5 \quad \text{nH}/\text{cm}$	$c = 2 \quad \text{pF}/\text{cm}$
$\ell = 1 \quad \text{cm}$	$f_c = 5 \quad \text{GHz}$	$R_s = Z_o = 50 \quad \Omega$

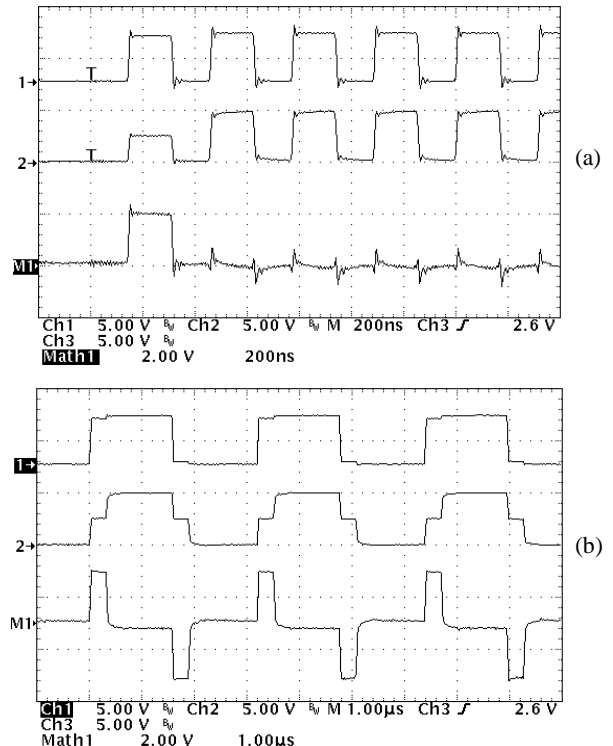


Fig. 5 Experimental results