Characterization and Modeling of Clock Skew with Process Variations

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ABSTRACT

A new compact model for on-chip clock skew as a function of device, interconnect, and system parameter variations is derived. Unlike previous models that describe qualitative behavior of clock skew components, the new model provides a closed form expression for each clock skew component. An example of clock skew components for a typical design using 0.18μm CMOS technology is investigated.

INTRODUCTION

Performance of high-speed synchronous digital systems is reduced significantly by clock skew of the clock distribution network [1]. The concept of zero clock skew balanced networks has been previously proposed by [2][3], however clock skew created by process parameter variations is still unavoidable. It is, therefore, imperative to characterize the clock skew components due to process parameter variations. To enhance this understanding, a new closed form model for clock skew is derived to enable first-order estimation of clock skew in digital systems. Unlike previous models that describe qualitative behavior of clock skew components [3], the new model provides a closed form equation for each clock skew component which consists of both process and circuit parameter fluctuations.

A complete set of clock skew components in balanced clock tree networks is described in Section II. In Section III, the assumptions and derivation of the new clock skew model are examined. Using the new model, an example of clock skew components for a design in 0.18μm technology is illustrated in Section IV. Finally, some conclusions are offered in Section V.

II. CLOCK SKEW COMPONENTS

Clock skew arises mainly from unequal clock path lengths to various modules. To equalize line lengths, and thus reduce the clock skew, a common practice is the use of a balanced clock network. In this way the nominal value of skew becomes zero and clock skew reduces to the variations of the clock path from the clock generator to the registers. These variations may originate from process and circuit parameter tolerances, which are codified hereafter.

A. Device Parameter Variations

In the IC fabrication process, all device parameters are subject to deviations from their nominal values. Statistical models have been developed for transistor parameters such as threshold voltage (ΔV_T), gate oxide thickness (Δt_{ox}), and effective channel length (ΔL_{eff}) [4].

B. Interconnect Parameter Variations

Interconnect width (ΔW_{int}) and thickness (ΔH_{int}) and interlevel dielectric (ILD) thickness (ΔT_{ILD}) variations are the main parameters of interest. As technology advances, the number of interconnect layers increases, and the interconnect lines become more non-uniform. This non-uniformity, which is caused by manufacturing processes, produces large variations of interconnect parameter values. Chemical mechanical polishing (CMP) is a new manufacturing process for planarization of metal and ILD layers that greatly reduces the ILD non-uniformity in muli-layer structures. However, the CMP process still does not eliminate interconnect parameter variations completely. Metal dishing and oxide erosion are the vexing issues in CMP which degrade the planarization efficiency [5]. The amount of metal dishing and oxide erosion, in general, is a function of metal width and pattern density [5]. Hence interconnect and ILD thickness variations are important considerations even after use of CMP processes.

C. System Parameter Variations

Besides process parameter variations, which are mainly the tolerances of device and interconnect physical parameters, system level fluctuations may create clock skew. Power supply voltage fluctuation (IR drop, ΔV_{DD}), temperature variations ($\Delta \mathcal{T}$), and non-uniform distribution of clocked registers (clock driver load mismatch, ΔC_L) are considered as system level parameter variations.

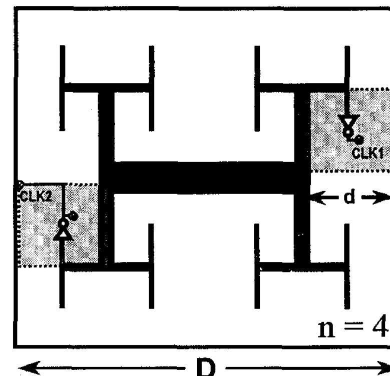

Fig. 1. Symmetric H-tree structure

Supported by the Semiconductor Research Corporation through RPI (subcontract: A70510e)

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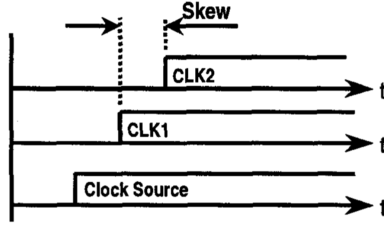

Fig. 2. Clock skew between the two points CLK1 and CLK2 in Fig. 1

III. Derivation of Clock Skew Model

The goal of the derivation of a clock skew model is to understand the impact of process and system variations in an ideally zero skew clock network distribution. A most common strategy to ensure zero nominal clock skew, which is often used for distributing high frequency clock signals in digital systems, is a symmetric H-tree structure [2]. Although a model is derived here specially for the symmetric H-tree structure, the model can be easily modified for any balanced clock tree network.

A. Assumptions

Although the growing importance of on-chip transmission line effects has been predicted [6], the difficulty of modeling and simulating lossy, non-uniform transmission lines using existing CAD tools has prevented consideration of these effects in most cases. There are some methods, however, to reduce the inductance effects in actual design. For instance, for the clock distribution described in [7], ground return path wiring has been implemented on the two metal levels above and below the clock wire to reduce inductance effects. To simplify the derivation of a clock skew model, good return path wiring has been assumed to surround the clock wiring network. Therefore, in this simplified study the inductance effect is ignored. Moreover, without lose of generality, it is assumed that the clock network is a balanced H-tree structure. This model, however, can be easily modified for any balanced clock tree network.

B. The Complete Clock Skew Model

Figure 1 shows a symmetric H-tree clock distribution with n=4 levels of H-tree branches. At the end of the 4th level, drivers are implemented to feed the clock signal to all registers in the sub-blocks. The total clock skew, by definition, is the time difference between the maximum and minimum delays as illustrated in Fig. 2.

Using the equivalent circuit diagram shown in Fig. 3, The delay of the entire clock network of Fig. 1 is assorted into three parts: i) H-tree network, ii) clock driver, and iii) sub-block routing.

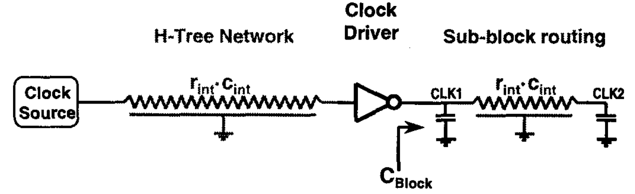

Fig. 3. Equivalent circuit of clock network in Fig. 1

(i) Interconnect delay from the clock source located at the center of the chip through the H-tree to the driver – Assuming that the H-tree network is driven by a single driver and the line capacitance of the H-tree network is much greater than the transistor input capacitance of a sub-block clock driver, then the interconnect delay expression for the approximate 50% time delay of the distributed RC line using Sakuri's model is [8], [2]

$$T_{H\text{-}Tree} = 0.4(r_{int}c_{int}) \cdot l^2 + \frac{\sqrt{\varepsilon_r}}{c_o} \cdot l \quad (1)$$

where l is the length of the H-tree network, r_{int} and c_{int} are the distributed resistance and capacitance of the line, ε_r is the relative dielectric constant of the ILD material, and c_o is the speed of light in free space. Since the wires in clock distributions are often much wider than the minimum wire width [6], the fringing capacitance is negligible compared to parallel plate wiring capacitance. Using the expression for the length of the H-tree versus die size, D, and the number of H-tree levels, n, defined in [2], then (1) becomes

$$T_{H\text{-}Tree} = 0.4\left(\frac{\rho \cdot \varepsilon_r}{H_{int} \cdot T_{ILD}}\right) \cdot D^2 \left(1 - \frac{1}{2^{n/2}}\right)^2 + \frac{\sqrt{\varepsilon_r}}{c_o} \cdot D\left(1 - \frac{1}{2^{n/2}}\right) \quad (2)$$

where H_{int} is interconnect thickness, T_{ILD} is interlevel dielectric thickness, and ρ is the line resistivity.

(ii) Transistor delay of the sub-block clock driver – The clocked registers within sub-blocks are assumed to be randomly placed and routed, therefore the delay expression for the approximate 50% time delay of the sub-block drivers is simply

$$T_{Driver} = 0.7R_{tr} \cdot C_L = 0.7\left(\frac{(L_{eff}/W)}{\mu \cdot C_{ox}(V_{DD} - V_T)}\right) \cdot C_L \quad (3)$$

where C_L is the total wiring and register input capacitance within the sub-block, L and W are transistor channel length and width respectively, μ is the mobility, C_{ox} is the gate oxide capacitance, and V_{DD} and V_T are supply and transistor threshold voltage respectively.

(iii) Internal wire routing delay within the sub-block from the clock driver to registers – The wiring delay inside the sub-block is computed in a similar way from (1) except that the length of wire, l, is the Manhattan distance from center to the corner of the sub-block ($d = D/2^{n/2}$ [2]).

$$T_{Sub-Blk} = 0.4(r_{int}c_{int})d^2 + \frac{\sqrt{\varepsilon_{r,ox}}}{c_o}d = 0.4(r_{int}c_{int})\frac{D^2}{2^n} + \frac{\sqrt{\varepsilon_{r,ox}}}{c_o}\frac{D}{2^{n/2}} \quad (4)$$

Since, in general, the placement of clocked registers is not uniform, the routing within the sub-block is not equidistance. For instance, in Fig. 1 the clock signal at the point CLK2 arrives later than CLK1. This delay, which is often called *internal clock skew* [2], in the worst case is given by (4).

The overall delay of the entire clock distribution network, from the clock source to the clocked registers, is $T_{Delay} = T_{H-Tree} + T_{Driver} + T_{Sub-Blk}$. Since the sub-block size is often much less than the chip size, the wiring delay within the sub-block, $T_{Sub-Blk}$, can be ignored. Therefore the total delay is given by

$$T_{Delay} \approx T_{H-Tree} + T_{Driver} \approx 0.4\left(\frac{\rho \cdot \varepsilon_r}{H_{int} \cdot T_{ILD}}\right) \cdot D^2\left(1 - \frac{1}{2^{n/2}}\right)^2 + \frac{\sqrt{\varepsilon_r}}{c_o} \cdot D\left(1 - \frac{1}{2^{n/2}}\right) + 0.7\left(\frac{(L_{eff}/W)}{\mu \cdot C_{ox}(V_{DD} - V_T)}\right) \cdot C_L \quad (5)$$

Equation (5) contains all device, interconnect, and system parameters described in Section II. Assuming that these parameters have small variations compared to their nominal values, the clock skew, T_{CSK}, can be evaluated by

$$T_{CSK}(x) = \Delta T_{Delay} \approx \left|\frac{\partial T_{Delay}}{\partial x}\right| \Delta x \quad (6)$$

where T_{Delay} is the complete delay function of (5), and x is any variation of clock skew components such as ΔH_{int}, ΔT_{ILD}, ΔV_{DD}, ΔV_T, Δt_{ox}, ΔL_{eff}, and ΔC_L. Table I shows the closed form equations for each individual clock skew component by using (6).

C. Clock Skew for Temperature ($\mathcal{T}$) Variation

The clock skew due to temperature gradient on a chip, in general, is more complex since there are three main parameters that vary with temperature; resistivity of interconnect $\rho(\mathcal{T})$, threshold voltage $V_T(\mathcal{T})$, and mobility $\mu(\mathcal{T})$. Assuming that the variation of threshold voltage is greater than that of mobility and resistivity of lines, then the clock skew due to temperature difference is given by

$$T_{CSK}(\mathcal{T}) = \Delta T_{Delay} \approx \left|\frac{\partial T_{Delay}}{\partial V_T} \cdot \frac{\partial V_T}{\partial \mathcal{T}}\right| \cdot \Delta\mathcal{T} \quad (7)$$

where $\Delta\mathcal{T}$ is temperature difference of two points in the chip. The first expression, $\partial T_{Delay}/\partial V_T$, is computed from (5) as

$$\frac{\partial T_{Delay}}{\partial V_T} = 0.7R_{tr} \cdot C_L \cdot \left(\frac{1}{V_{DD} - V_T}\right) \quad (8)$$

Also the second expression, $\partial V_T/\partial\mathcal{T}$, is [9]

$$\frac{\partial V_T}{\partial \mathcal{T}} = \frac{1}{\mathcal{T}}\left(2 - \frac{Q_B}{2C_{ox}\varphi_f}\right) \cdot \left(\varphi_f + \frac{E_g}{2q}\right) \quad (9)$$

TABLE I. Clock Skew Components

Physical Parameter and Derivation Used		Clock Skew Compact Model
ILD Thickness Variation	$\left\|\frac{\partial T_{Delay}}{\partial T_{ILD}}\right\|$	$T_{CSK}(T_{ILD}) = 0.4(r_{int}c_{int}) \cdot D^2\left(1 - \frac{1}{2^{n/2}}\right)^2 \cdot \left(\frac{\Delta T_{ILD}}{T_{ILD}}\right)$
Wire Thickness Variation	$\left\|\frac{\partial T_{Delay}}{\partial H_{int}}\right\|$	$T_{CSK}(H_{int}) = 0.4(r_{int}c_{int}) \cdot D^2\left(1 - \frac{1}{2^{n/2}}\right)^2 \cdot \left(\frac{\Delta H_{int}}{H_{int}}\right)$
Threshold Voltage Fluctuation	$\left\|\frac{\partial T_{Delay}}{\partial V_T}\right\|$	$T_{CSK}(V_T) = 0.7R_{tr}C_L\left(\frac{V_T}{V_{DD} - V_T}\right) \cdot \left(\frac{\Delta V_T}{V_T}\right)$
Transistor Channel Length Tolerance	$\left\|\frac{\partial T_{Delay}}{\partial L_{eff}}\right\|$	$T_{CSK}(L_{eff}) = 0.7R_{tr}C_L \cdot \left(\frac{\Delta L_{eff}}{L_{eff}}\right)$
Gate Oxide Thickness Tolerance	$\left\|\frac{\partial T_{Delay}}{\partial t_{ox}}\right\|$	$T_{CSK}(t_{ox}) = 0.7R_{tr}C_L \cdot \left(\frac{\Delta t_{ox}}{t_{ox}}\right)$
IR Drop	$\left\|\frac{\partial T_{Delay}}{\partial V_{DD}}\right\|$	$T_{CSK}(V_{DD}) = 0.7R_{tr}C_L\left(\frac{V_{DD}}{V_{DD} - V_T}\right) \cdot \left(\frac{\Delta V_{DD}}{V_{DD}}\right)$
Non-uniform Register distribution	$\left\|\frac{\partial T_{Delay}}{\partial C_L}\right\|$	$T_{CSK}(C_L) = 0.7R_{tr}C_L \cdot \left(\frac{\Delta C_L}{C_L}\right)$
Temperature gradient	$\left\|\frac{\partial T_{Delay}}{\partial \mathcal{T}}\right\|$	$T_{CSK}(\mathcal{T}) = 0.7R_{tr}C_L\left(\frac{E_g/q + V_T}{V_{DD} - V_T}\right) \cdot \left(\frac{\Delta\mathcal{T}}{\mathcal{T}}\right)$
Internal Clock Skew	—	$T_{CSK}(internal) = (r_{int}c_{int}) \cdot \frac{D^2}{2^n} + \frac{\sqrt{\varepsilon_{r,ox}}}{c_0} \cdot \frac{D}{2^{n/2}}$

where Q_B is the depletion-region charge, C_{ox} is the gate oxide capacitance, φ_f is the Fermi level potential, E_g is the energy gap of Si, and q is the charge of electron. In order to simplify (9), the threshold voltage can be written as $V_T \approx \varphi_{Si} - Q_B/C_{ox}$ [9]. Moreover assuming that the substrate doping concentration is relatively high, then the surface potential of MOSFET transistor is given by $\varphi_{Si} = 2\varphi_f \approx 2(E_g/2)$. Therefore the first order approximation of (9) is given by

$$\frac{\partial V_T}{\partial \mathcal{T}} \approx \frac{E_g/q + V_T}{\mathcal{T}} \quad (10)$$

where E_g/q=1.12 V is the energy gap of Si in volts, and $\mathcal{T}$ is the temperature in degrees Kelvin. Equation (7) along with the results of (8) and (10) give

$$T_{CSK}(\mathcal{T}) \approx 0.7R_{tr} \cdot C_L \cdot \left(\frac{E_g/q + V_T}{V_{DD} - V_T}\right) \cdot \left(\frac{\Delta\mathcal{T}}{\mathcal{T}}\right) \quad (11)$$

TABLE II. Process and Design Parameters

Parameters		Values
Process Paramete	L_{eff}	0.18 [μm]
	V_T	0.32 [V]
	V_{DD}	1.8 [V]
	$r_{int}c_{int}$	115 [ps/cm^2]
Design Paramete	R_{tr}	12.0 [Ω]
	C_L	6.25 [pF]
	D	2.0 [cm]
	n	4

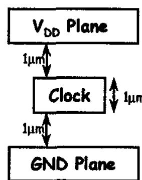

Fig. 4. Clock distribution wiring structure

IV. An Example of a Design in 0.18μm Technology

In order to illustrate the new clock skew model, a design example for 0.18μm technology has been studied using the design parameters [4] illustrated in Table II. The H-tree clock distribution is assumed to be routed by the 4th metal level shielded with the 3rd and 5th metal levels as depicted in Fig. 4. This wiring structure ensures minimal inductive effect. Equation (1) is, therefore, valid for interconnect propagation delay with $r_{int}c_{int}$=115 ps/cm^2, assuming that Cu/SiO_2 materials are used in wiring network. In this example the total number of clocked registers is set to 20,000. With an input register capacitance of 5fF, the total capacitance of each sub-block, on average, is computed as C_L=6.25 pF. A driver with R_{tr}=12.0 Ω output resistance is selected to ensure fast rise time for the total sub-block loading capacitance. Using the expressions of Table I, the complete set of clock skew components are evaluated as shown in Table III. In this Table, the second column is expressed as the sensitivity of clock skew in *picosecond per 1%* for the given parameters. The third column contains percentage of variations, which are technology and design dependent. The tolerances of interconnect and ILD thickness are roughly 3% for a well-controlled CMP process described in [5]. Statistical modeling in [4] extracted from the measurement data of 0.18μm technology shows that the fluctuations of threshold voltage, MOS effective channel length, and gate oxide thickness are about 5%, 5% and 1.2% respectively. The tolerance of supply voltage is usually limited to 10% of total supply voltage [10]. Moreover, the thermal image of the Alpha microprocessor in [10] shows a 30°C temperature gradient over the entire chip which gives

TABLE III. Clock Skew Components

Parameters	Clock Skew Coeff. [ps/1%]	%of Variations	Clock Skew Comp. [ps]
T_{ILD}	1.04	3%	3.12
H_{int}	1.04	3%	3.12
V_T	0.11	5%	0.55
L_{eff}	0.53	5%	2.65
t_{ox}	0.53	1.2%	0.64
V_{DD}	0.64	10%	6.40
C_L	0.53	20%	10.6
$\mathcal{T}$	0.51	8%	4.08
Internal Clock Skew [ps]			61.7
Total Clock Skew [ps]			92.9

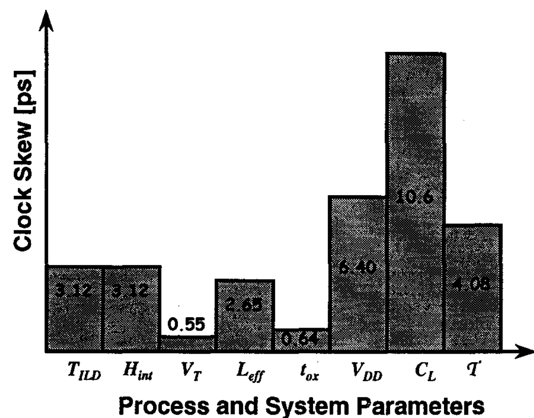

Fig. 5. Clock skew components

a temperature variation of about 8%. The variations of loading capacitance of clock drivers highly depend on the uniformity of architecture. A specific investigation of a microprocessor design shows that about 20% variation exists on the sub-block loading capacitance.

The clock skew components are evaluated based on the amount of variations in the third column of Table III. Figure 5 illustrates a graphical view of clock skew components. A skew of 10.6ps is created just by clock driver load mismatch. Also, IR drop, temperature gradient, interconnect and ILD thickness variations, and MOS channel length tolerance create 6.4ps, 4.08ps, 3.12ps and 2.65ps respectively.

V. Conclusion

Based upon the delay equation in a balanced clock tree network, new closed form expressions for clock skew as a function of device, interconnect and system parameter variations are derived. Using the new compact model, all clock skew components for a 0.18μm technology design are evaluated.

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