# The Impact of Cu/low κ on Chip Performance

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*Abstract* – **A new model to predict percentage of performance improvement using copper and/or low κ is rigorously derived. Based on the new model, it is shown that for a typical ASIC design in 0.25μm technology, using copper interconnect alone can improve the speed by about 10%; however in the same technology, using low κ dielectric ($\varepsilon_r$=2.5) alone can improve the speed by about 27%. The new model indicates that the performance gain for copper and low κ are not additive. Finally the model is applied to the NTRS projections to explore the performance gain through future technology generations.**

## I. INTRODUCTION

EMPLOYING copper instead of aluminum interconnects has been reported by IBM for the first time [1]. Although copper interconnects have hit the marketplace with IBM's initial commercial shipments of the 400-MHz PowerPC750 processor, the impact of copper is still an uncertain issue.

In this paper a new model for the percentage of speed improvement using copper and/or low κ is rigorously derived. This model strictly gives a range of performance gain that can be achieved by introduction of copper and/or low κ. Although by using system simulators such as GENESYS [2] the performance gain of copper and low κ was previously computed, these simulations do not probe the physical bases for performance gain. The following new model is so simple that not only can the speed improvement be easily computed from basic technology parameters, but it also provides some insight into the improvement in speed.

The complete derivation of the new performance gain model is presented in Section II. In Section III, the new model is applied to the NTRS technology generations. Finally, some conclusions are offered in Section IV.

## II. PERFORMANCE GAIN MODEL

In general, the performance gains of Cu/low κ depend on the combination of gate and interconnect delay. It is obvious that for an interconnect limited design, which means the delay is mostly limited by interconnect delay, the performance is enhanced by improving interconnect delay. Since Cu/low κ enhances interconnect speed, the speed gain in such a design is significant. Conversely, for a gate limited design, which means the delay is mostly limited by gate delay, the performance doesn't improve much by improving interconnect delay.

A critical path model is the main hypothesis of the performance improvement derivation since the change of interconnect system affects the critical path delay and thus results in variation of clock speed. In this section a new model of performance gain is computed by using a critical path model.

### A. Assumptions

To derive a simple model for critical path delay in different interconnect structures, two main assumptions are made.

(i) The best case scenario for copper and low κ – It is assumed that for copper and low κ structures all aluminum lines are replaced by copper and all $SiO_2$ insulator layers are replaced by low κ material. Also it is assumed that the metal liner thickness is negligible compared to metal cross section dimensions in the current technology. This assumption is the best case scenario for the new interconnect structure compared to the conventional Al/$SiO_2$ structure.

(ii) Comparison within the same technology generation assuming Al/$SiO_2$ as a base structure – It is assumed that the new interconnect structure is applied within the same technology generation. This means that there is no scaling between the new interconnect structure and the conventional Al/$SiO_2$ structure. This is reasonable because photolithography usually remains unchanged within each technology.

### B. Derivations

The performance of a design depends on the clock speed, which is dependent on the critical path delay. Figure 1 illustrates the timing relationship between the critical path and the clock period. This relationship can be written as

$$T_{Clock} = T_{Skew} + T_{Critical} + T_{Margin} + T_{Setup} \quad (1)$$

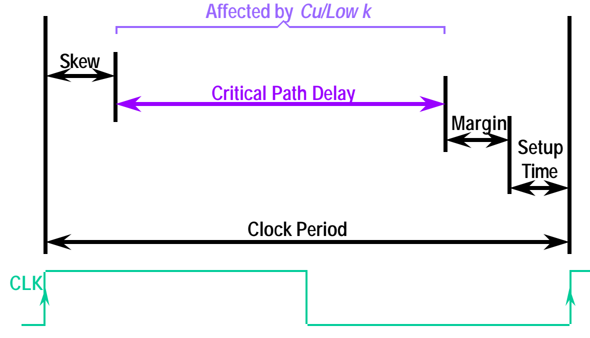



Fig. 1 – Timing relationship between the critical path and clock period

where $T_{Clock}$, $T_{Skew}$, $T_{Critical}$, $T_{Margin}$ and $T_{Setup}$ are the clock period, clock skew, critical path delay, some amount of margin and latch setup time, respectively. The impact of interconnect structure is mostly on the critical path delay and since the critical path delay is usually the dominant term in (1), the variation of critical path delay is directly translated into clock frequency.

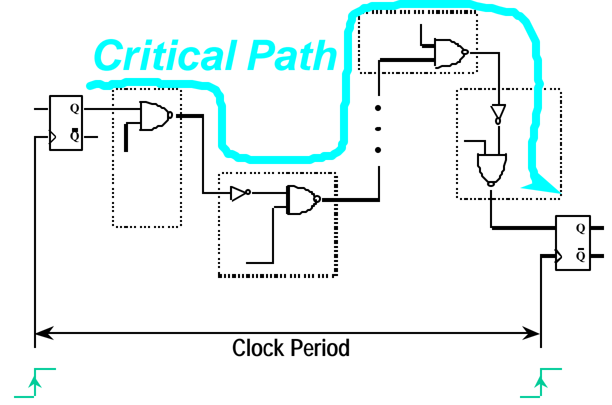
Various critical path models have been proposed [3,4]. One essential component of a critical path model for CMOS circuits is the interconnect networks loading of critical path gates. Using a simplified model of one stage of a critical path shown in Fig. 2, the total critical path delay is determined from

$$T_{Critical} \approx n_c (R_G + R_{int})(C_{int} + Fo \cdot C_G) \quad (2)$$

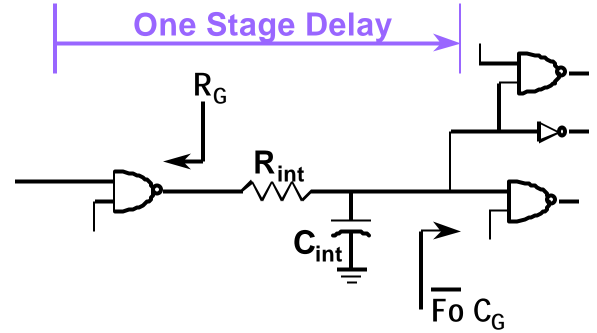
where $n_c$ is logic depth (effective number of gates in critical path), $R_G$ is gate driving resistance, $R_{int}$ is average interconnect resistance, $C_{int}$ is average interconnect capacitance, $Fo$ is the average fan-out, and $C_G$ is the gate input capacitance. Since only $R_{int}$ and $C_{int}$ depend on the interconnect structure in (2), the new critical path delay, $T'_{Critical}$, after replacing wire and insulator materials is computed by

$$T'_{Critical} \approx n_c \left[ R_G + R_{int}\left(1 - \frac{\Delta\rho}{\rho_{Al}}\right)\right]\left[ C_{int}\left(1 - \frac{\Delta\varepsilon}{\varepsilon_{SiO_2}}\right) + Fo \cdot C_G \right] \quad (3)$$

where $\Delta\rho = \rho_{Al} - \rho_{Cu}$ is the resistivity difference between the copper and aluminum resistivity, and $\Delta\varepsilon = \varepsilon_{SiO_2} - \varepsilon_{lowk}$ is the permitivity difference between the low $\kappa$ and $SiO_2$ permitivity. Subtracting (3) from (2) gives the critical path delay difference in the two designs with different interconnect structures. Substituting $R_{int}$ with $r_{int} \cdot L$ and $C_{int}$ with $c_{int} \cdot L$ where $r_{int}$ and $c_{int}$ are the interconnect resistance and capacitance per unit length, and $L$ is the length of the interconnect, the speed improvement with respect to the base $Al/SiO_2$ structure is given by




(a) An example of critical path




(b) Equivalent circuit for critical path

Fig. 2 – A simplified model for critical path delay

$$\frac{\Delta T_{Critical}}{T_{Critical}} = \frac{\Delta\rho/\rho_{Al}}{1 + \frac{R_G}{r_{int} \cdot L}} + \frac{\Delta\varepsilon/\varepsilon_{SiO_2}}{1 + \frac{Fo \cdot C_G}{c_{int} \cdot L}} - \frac{(\Delta\rho/\rho_{Al})(\Delta\varepsilon/\varepsilon_{SiO_2})}{\left(1 + \frac{R_G}{r_{int} \cdot L}\right)\left(1 + \frac{Fo \cdot C_G}{c_{int} \cdot L}\right)} \quad (4)$$

All parameters in (4) are well-defined in any technology. Interconnect average length ($L$) is the only variable which depends on design structure.

The first term in (4) represents the impact of copper alone, the second term represents the impact of low $\kappa$ alone, and the third term denotes the cross term degradation. Equation (4) clearly shows that the impact of copper and low $\kappa$ on chip performance is not additive and a cross-term degradation reduces the total speed improvement.

Equation (4) describes the complete behavior of the system in the general case. In a gate-limited design where the interconnect length in the critical path is very short ($L \ll R_G/r_{int}$ and/or $L \ll Fo \times C_G/c_{int}$), the overall speed improvement in all interconnect structures of copper alone, low $\kappa$ alone and Cu/low $\kappa$ is almost *0%*. However in an interconnect-limited design where the interconnect length in the critical path is very long ($L \gg R_G/r_{int}$ and/or $L \gg Fo \times C_G/c_{int}$), the overall speed improvement is

**TABLE I – Typical values for technology parameters in 0.25μm CMOS technology**

| Technology parameters | Symbolic representation | Typical values |
|---|---|---|
| Interconnect resistance per unit length | $r_{int}$ | *1.9 [kW/cm]* |
| Interconnect capacitance per unit length | $c_{int}$ | *1.5 [pF/cm]* |
| Average fan-out | $Fo$ | *3.0* |
| Gate output resistance | $R_G$ | *500 [W]* |
| Gate input capacitance | $C_G$ | *15 [fF]* |
| Copper resistivity with respect to aluminum | $\Delta\rho/\rho_{Al}$ | *39%* |
| Low κ permitivity with respect to $SiO_2$ ($\varepsilon_r$=2.5) | $\Delta\varepsilon/\varepsilon_{SiO_2}$ | *36%* |

$$\frac{\Delta T_{Critical}}{T_{Critical}} = \frac{\Delta\rho}{\rho_{Al}} + \frac{\Delta\varepsilon}{\varepsilon_{SiO_2}} - \frac{\Delta\rho\cdot\Delta\varepsilon}{\rho_{Al}\cdot\varepsilon_{SiO_2}} \quad (5)$$

Equation (5) shows that the ultimate speed improvement for copper alone is $\Delta\rho/\rho_{Al} = 39\%$, for low κ alone it is $\Delta\varepsilon/\varepsilon_{SiO_2} = 36\%$ assuming $\varepsilon_r = 2.5$ for the low κ material, and for Cu/low κ together is $0.39 + 0.36 - 0.39\times 0.36 = 61\%$. Note that achieving this ultimate level is nearly impossible since it requires a huge chip size (on the order of *10 ´10* $cm^2$).

### C. An Example

Table I shows typical values for the 0.25μm CMOS technology parameters used in (4). In this table the

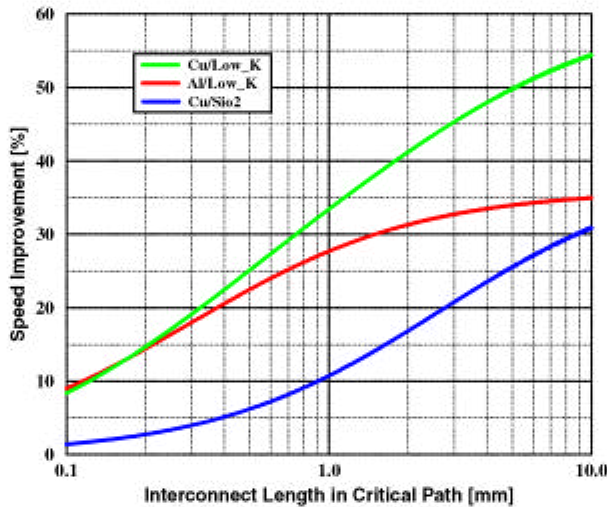



Fig. 3 – Speed improvement versus interconnect length in 0.25μm technology

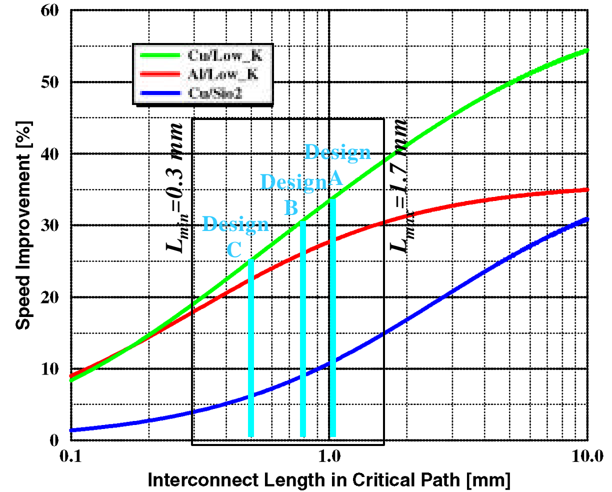



Fig. 4 – Speed improvement plane and typical interconnect lengths

interconnect resistance and capacitance are calculated for the second metal layer and/or third metal layer. The gate resistance and capacitance are calculated for a typical 2 input NAND gate. The average fan-out of 3.0 is a typical value for most ASIC designs. Note that the average fan-out lies roughly in the range of $2.0 < Fo < 4.0$ in random logic networks [5].

Figure 3 illustrates the speed improvement versus average interconnect length for three interconnect structures of Cu/$SiO_2$, Al/low κ, and Cu/low κ assuming the technology parameters shown in Table I for Al/$SiO_2$ as a base. To find a rough boundary of performance gain from the plot of Fig. 3, the average wire length in the critical path is required. A complete wire-length distribution that is derived in [6] can be used to accurately estimate the average wire length in the critical path. For simplicity, in this paper a simple empirical rule is used for average wire length. It has been observed [7] that the average wire length in typical designs is around *0.1D* where *D* is the chip size. In the current technology for a variety of ASIC designs the chip size is in the range of *3 ´3*$mm^2$ to *17 ´17*$mm^2$ and the average wire length lies roughly in the range of $0.3mm<L<1.7mm$. This region is depicted as a box in Fig. 4 to illustrate the range of performance gain for each case of copper alone, low κ alone, and copper/low κ with respect to Al/$SiO_2$. For a given chip size of *10 ´10*$mm^2$, which is the average chip size of the current technology, it can be seen from Fig. 4 that a speed improvement of *10%, 27%,* and *33%* for the case of copper alone, low κ alone, and copper/low κ is achieved respectively.

## III. Study of Performance Gain in Future Technologies

Since interconnect dimensions in future technologies are comparable to liner thickness, the assumption that we have made in Section II must be modified to study the

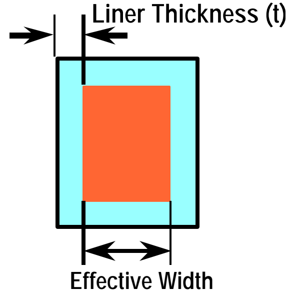



Fig. 5 – Metal cross section indicating liner thickness

performance gain in future technologies. Although the assumptions are different, the performance model derivation is done in a similar way.

### A. *New Assumptions*

New assumptions are similar to those given in Section II except for interconnect scaling.

(i) The best case scenario for copper and low κ –It is assumed that for copper and low κ interconnect systems all aluminum lines are replaced by copper and all $SiO_2$ dielectric layers are replaced by low κ material. But here, it is assumed that *the liner thickness is not negligible compared to interconnect dimensions.*

(i) Comparison within *different* technologies assuming $Al/SiO_2$ as a base structure – It is assumed that the new interconnect structure is scaled for each technology node.

### B. *Effective Copper Resistivity*

Figure 5 shows a cross section of interconnect including the liner material. The effective copper resistivity with respect to aluminum assuming $\rho_{Liner} >> \rho_{Cu}$ can be easily derived as

$$\frac{\Delta\rho_{eff}}{\rho_{Al}} \approx 39\% - \frac{2t\cdot\left(\frac{1}{W}+\frac{1}{H}\right)}{1-2t\cdot\left(\frac{1}{W}+\frac{1}{H}\right)}\frac{\rho_{Cu}}{\rho_{Al}} \qquad (6)$$

where $t$ is the liner thickness, and $W$ and $H$ are the interconnect width and thickness respectively. Equation (6) shows that the effective copper resistivity with respect to aluminum, which is the ultimate speed improvement by using copper, is affected by liner thickness as the interconnect dimensions shrink. Based on the NTRS [8] technology road map shown in Table II, the variation of copper effective resistivity versus technology generation is shown in Fig. 6, where the liner thickness is assumed to be $50\,Å$ for future technologies.

**TABLE II – Nominal interconnect parameters used in this study**

| Technology Generation | Feature Size [μm] | Interconnect width & spacing [μm] | Interconnect Thickness [μm] | ILD Thickness [μm] | $r_{int}$ [KΩ/Cm] | $c_{int}$ [PF/Cm] |
|---|---|---|---|---|---|---|
| G1 | 0.40 | 0.55 | 0.70 | 0.70 | 1.00 | 1.29 |
| G2 | 0.25 | 0.40 | 0.60 | 0.65 | 1.43 | 1.26 |
| G3 | 0.18 | 0.25 | 0.50 | 0.60 | 2.60 | 1.51 |
| G4 | 0.13 | 0.19 | 0.43 | 0.55 | 4.53 | 1.68 |
| G5 | 0.10 | 0.14 | 0.35 | 0.5 | 7.57 | 1.82 |
| G6 | 0.07 | 0.10 | 0.27 | 0.45 | 13.7 | 1.94 |

**TABLE III – Nominal device parameters used in this study**

| Technology Generation | Feature Size [µm] | Supply Voltage [V] | Gate Oxide Thickness [°A] | Transistor Aspect ratio (W/L) | $R_G$ [Ω] | $C_G$ [fF] |
|---|---|---|---|---|---|---|
| G1 | 0.40 | 3.3 | 60 | 20 | 670 | 31 |
| G2 | 0.25 | 2.5 | 50 | 25 | 570 | 20 |
| G3 | 0.18 | 1.8 | 40 | 30 | 410 | 18 |
| G4 | 0.13 | 1.5 | 30 | 33 | 390 | 15 |
| G5 | 0.10 | 1.2 | 20 | 36 | 370 | 12 |
| G6 | 0.07 | 1.0 | 15 | 40 | 360 | 9 |

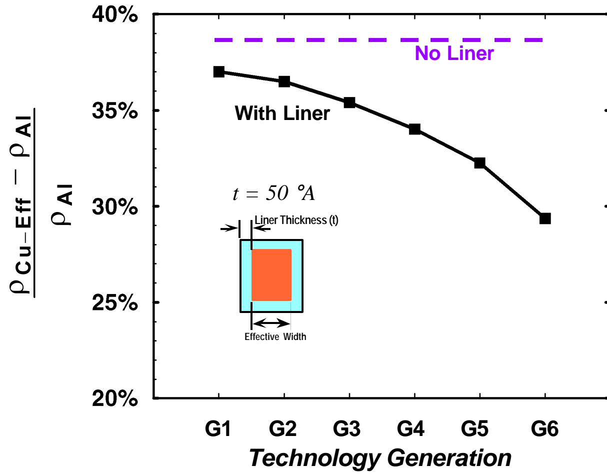



Fig. 6 – Effective copper resistivity with respect to aluminum

### C. Performance Gain versus Technology Generation

Table II and Table III show the technology parameters for each technology generation based on the NTRS road map. Using these parameters and the performance gain model presented in Section II, the performance improvement versus technology generation is depicted in Fig. 7 for each case of copper alone, low κ alone, and copper/low κ with respect to $Al/SiO_2$. The effect of liner thickness is also depicted in this figure.

As a result, Fig. 7 shows that the performance gain in copper technology with liner is diminished significantly in deep-submicron technologies. However the low κ has better performance gains in all technology generations.

## V. CONCLUSION

A new model for the percentage of performance improvement using copper and/or low κ is rigorously derived. Based on the new model, it is shown that for a typical ASIC design in a 0.25µm technology, copper alone can improve the speed by about 10%. In the same technology, low κ alone can improve the speed by about 27%. The new model clearly predicts that the performance gains for copper and low κ are not additive. Finally, the model is applied to the NTRS technology road map to explore performance gains through future technologies. A simple model for the effect of liner resistivity on effective copper resistivity is also included.

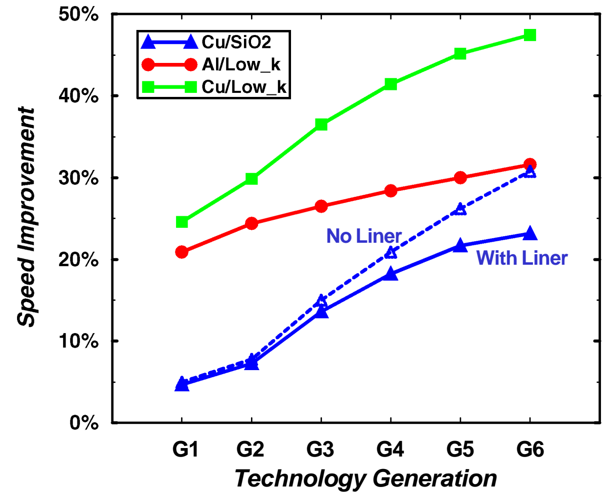



Fig. 7 – Performance improvement versus technology generation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