

Compact Physical Models for Multilevel Interconnect Crosstalk in Gigascale Integration (GSI)

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Abstract—For the first time, compact physical models are derived for crosstalk noise of coplanar resistance–inductance–capacitance lines in a gigascale integration (GSI) chip that simultaneously consider far and near aggressors in both the same metal level and distant metal levels. Since both the amplitude and duration of noise are important, the noise voltage–time integral can be defined as a figure-of-merit for crosstalk, and it is shown that this integral attains its maximum at the length at which the interconnect resistance becomes equal to twice the characteristic impedance. It is also shown that crosstalk can be prohibitively large if interconnects have small resistances. There is, therefore, a tradeoff between interconnect latency and crosstalk. The compact models are finally used to calculate the crosstalk noise voltage for the case that wire width is optimized by simultaneously maximizing data flux density and minimizing latency. It has been proven that by utilizing the optimal wire width for signal interconnects and twice of that for power and ground lines, the worst case peak crosstalk noise voltage becomes smaller than $0.25 V_{dd}$ for all generations of technology.

Index Terms—Crosstalk, inductance, interconnects, repeaters, system analysis and design, system optimization, transmission line theory.

I. INTRODUCTION

ONE OF THE most important aspects of designing a multilevel interconnect network is to keep crosstalk noise small and guarantee signal integrity. Although circuit simulators or numerical methods can be used to estimate crosstalk [1], [2] compact physical models are more insightful and can be easily incorporated in system-level optimizations. Crosstalk noise caused by one or two adjacent lines is modeled by Sakurai assuming that interconnects can be modeled by distributed RC lines [3]. As the clock frequency of chips increases and signal wavelength becomes comparable with the length of many on-chip wires, inductance can no longer be neglected [4]. Rigorous models for the crosstalk of distributed *RLC* lines above an ideal ground plane have been presented in [5] and [6]. Since the number of on-chip metal levels is limited, commonly no metal level is totally dedicated to power or ground. Instead, power and ground lines are inserted between signal lines to provide adequate return paths for signal lines and distribute power and ground across the chip. Crosstalk noise induced by an adjacent line in these coplanar transmission lines is modeled in [7] and [8]. For these models, it has been assumed that power and ground lines are wide enough that they isolate signal lines

from far lines. This assumption, however, may not be true if power and ground lines are not wide enough, and in fact, a large noise may be induced by far aggressors. In this paper, for the first time, compact physical models for the total crosstalk of coplanar *RLC* lines are presented that consider both near and far aggressors. Far aggressors that are two metal levels below the victim line also are taken into account.

The goal of this paper is to derive compact models that are insightful and can be easily incorporated in system-level optimization methodologies, which are usually performed at the early stages of design. Thereby, a simplified case is taken into account wherein a data bus consists of many parallel point-to-point interconnects. The models are then used to evaluate crosstalk noise voltage when the wire dimensions are optimized to simultaneously maximize data flux density and minimize latency [9], [10]. Data flux density is the product of interconnect bandwidth and reciprocal pitch, and represents the bandwidth of interconnects per unit width. It has been proven that once the optimal wire width is used, the worst case peak crosstalk noise voltage becomes small and constant for all generations of technology.

The rest of this paper is outlined as follows. In Section II, the problem and the methodology of solving it are defined. Far inductive crosstalk is modeled in Section III for the case that aggressor and victim lines are identical. Impact of far aggressors that are not identical to a victim line is then modeled in Section IV. In Section V, the noise voltage–time integral is introduced, and the interconnect length at which this integral attains its maximum is identified. Superposition theorem is used in Section VI to calculate crosstalk noise when a victim line is attacked by near and far lines simultaneously. An integrated crosstalk model is proposed in Section VII to calculate the crosstalk noise voltage induced by virtually all near and far aggressors. The peak noise voltage is expressed in terms of the ratio of wire width to optimal wire width in Section VIII to prove that utilizing optimal wire for signal interconnects and twice of that for power and ground lines makes the worst case crosstalk noise voltage smaller than $0.25 V_{dd}$ at all generations of technology. Finally, the results are summarized in Section IX.

II. METHODOLOGY

Fig. 1 shows a cross-sectional view of four top metal levels in a GSI chip. Wires in the top two metal levels are relatively thick and wide, and have prominent inductive effects. Hence, each signal line has a nearby power/ground line to have a nearby return path. This is the configuration that has been used for global interconnects in state-of-the-art high-performance chips such as Intel's Itanium or Sun's MAJC microprocessors [11], [12].

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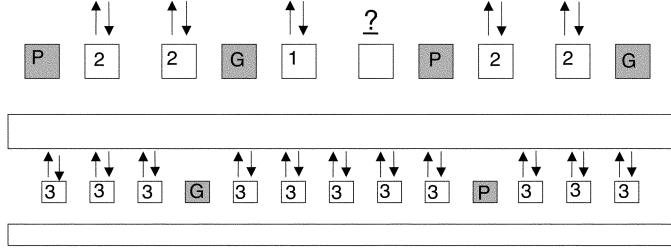


Fig. 1. Cross-sectional view of four top metal levels. Top two levels are relatively fat and due to inductive effects each signal line has a nearby power/ground line as a return path. The spaces between signal and ground lines are 0.45 times smaller than signal to signal spaces to reduce crosstalk and minimize worst case delay [7].

Wires in lower metal levels are more resistive, and, therefore, not every signal line has a nearby power/ground line.

A victim line on the top most level can be affected by three types of aggressors 1) a nearby aggressor; (2) far aggressors in the same metal level; and 3) far aggressors that are two metal levels below the victim line. The near aggressor is inductively and capacitively coupled to the victim line whereas far aggressors are only inductively coupled to the victim line. Aggressors that are within the same metal level as the victim line have the same inductance, capacitance, and resistance per unit length as the victim line does. Far aggressors in a lower metal level, however, have different resistance, inductance, and capacitance values compared with the victim line. Hence, the impact of different kinds of aggressors can be quite different. The mutual inductance between the victim and orthogonal lines is zero; therefore, they do not contribute to noise. One way of solving this complicated problem is to solve the set of differential equations described by

$$\frac{\partial^2}{\partial x^2}[V(x, t)] = [L][C]\frac{\partial^2}{\partial t^2}[V(x, t)] + [R][C]\frac{\partial}{\partial t}[V(x, t)] \quad (1)$$

where $[R]$, $[L]$ and $[C]$ are resistance, inductance and capacitance matrices, respectively. Since, different aggressors have different characteristics, a direct analytical solution for (1) may not be feasible. A numerical solution can also be very time consuming, and offers limited physical insight.

To find compact physical models for this problem, the near aggressor is ignored initially. Two cases are then solved. In the first case, a victim line is attacked by some aggressors that are identical to the victim. In the second case, a victim line is affected by aggressors that are not identical to the victim line. By using the superposition theorem, the total noise caused by all near and far aggressors is modeled.

III. IDENTICAL VICTIM AND AGGRESSOR LINES

In the case that far lines and a victim line are identical, far inductive noise is found by solving (1), where $[R]$ is substituted by scalar r , the loop resistance per unit length of each line. The loop resistance includes the resistance of return paths which are the power and ground lines. Since capacitance is a local effect, mutual capacitances between the far lines and the quiet line are negligible. The worst case crosstalk occurs when all far aggressors switch in phase, and therefore, the mutual capacitance be-

tween the far lines can be ignored, too. Hence, $[C]$ can be substituted by scalar c , the distributed self capacitance of the lines (Fig. 2).

By finding the eigenvectors of the inductance matrix, the set of differential equations described by (1) can be decoupled. For the case that all aggressors switch in-phase (the worst case for crosstalk), the following two modes of propagation describe the system:

$$V^- = \sum_{\text{All Aggressors}} \left(\frac{l_{vi}}{l_s} V_i \right) + \sqrt{\sum_{\text{All Aggressors}} \frac{l_{vi}^2}{l_s^2} V_i} \quad (2)$$

and

$$V^+ = \sum_{\text{All Aggressors}} \left(\frac{l_{vi}}{l_s} V_i \right) - \sqrt{\sum_{\text{All Aggressors}} \frac{l_{vi}^2}{l_s^2} V_i} \quad (3)$$

where l_{vi} is the mutual inductance between the victim line and the i th aggressor, l_s is the self inductance of lines, V_i is the voltage of the i th aggressor, and V_v is the voltage of the victim line. In the two-line case, the plus mode represents the aggressor and victim lines switching in the same direction, and the minus mode represents switching in opposite directions. The equivalent inductance and capacitance per unit length for each mode are given by

$$l^+ = l_s + \sqrt{\sum_{\text{All Aggressors}} l_{vi}^2}; \quad c^+ = c \quad (4)$$

and

$$l^- = l_s - \sqrt{\sum_{\text{All Aggressors}} l_{vi}^2}; \quad c^- = c. \quad (5)$$

The propagation speed for the plus and minus modes is given by

$$v = \frac{1}{\sqrt{lc}} \quad (6)$$

where l is the equivalent inductance per unit length corresponding to each mode. Voltage of each mode can be solved by either exact or low-loss approximate solutions for distributed RLC lines [5]. Low-loss approximation is used in this paper because it results in simple expressions that are insightful. The error is also small, especially for the peak noise voltage. The differential equation for a single RLC line in Laplace domain is [5]

$$\frac{\partial}{\partial x^2} V(x, s) = V(x, s) l c s^2 \left(1 + \frac{r}{sl} \right) \quad (7)$$

and the solution of (7) for an infinite long line is

$$V_{\text{inf}}(x, s) = V_{\text{in}}(s) \frac{Z(s)}{Z(s) + R_{\text{tr}}} e^{-xs\sqrt{lc}\sqrt{1+(r/sl)}} \quad (8)$$

where R_{tr} is the driver resistance, V_{in} is the input voltage, and $Z(s)$ is the lossy characteristic impedance defined as

$$Z(s) = Z_0 \sqrt{\frac{s + \frac{r}{l}}{s}} \quad (9)$$

where the loss-less characteristic impedance is $Z_0 = \sqrt{l/c}$.

Assuming that

$$\left| \frac{r}{l_s} \right| \ll 1 \quad (10)$$

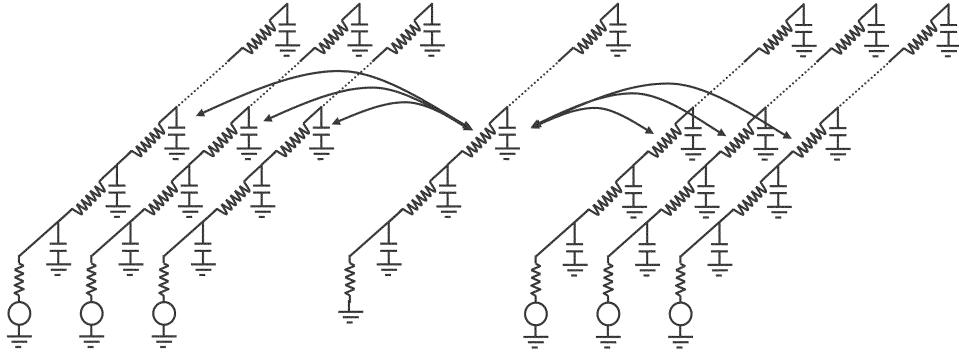


Fig. 2. Quiet victim line is attacked by some far aggressors. It has been assumed that there is no nearby aggressor and far lines are inductively coupled to the victim line. The resistance and capacitance matrices can be substituted by scalar resistance and capacitance values.

which is the low-loss approximation, (8) can be approximated by [13]

$$V_{\text{inf}}(x, s) = V_{\text{in}}(S) \frac{Z_0}{Z_0 + R_{\text{tr}}} e^{-x\sqrt{lc}(s+(r/2l))} \quad (11)$$

and for a step input, (11) in time domain can be written as

$$V_{\text{inf}}(x, t) = \frac{Z_0 V_{\text{dd}}}{Z_0 + R_{\text{tr}}} e^{-(rx/2Z_0)} u(t - x\sqrt{lc}) \quad (12)$$

which is the low-loss approximate solution for a single distributed RLC line. Note that even for lossy lines (10) is valid at high frequencies ($s = j\omega$), which means that the low-loss approximation accurately describes the voltage of the line for $t \approx x\sqrt{lc}$. As it will be shown, the peak noise occurs at a time close to the time-of-flight (ToF). The low-loss approximation can, therefore, accurately model the peak noise voltage. For a further accurate analysis, one can use the rigorous solution for a single RLC line.

Voltage of the victim line can be written in terms of the two modes as

$$V_v = \frac{(V^+ - V^-)}{\sqrt{\sum_{\text{All Aggressors}} \left(\frac{l_{vi}^2}{l_s^2}\right)}}. \quad (13)$$

As (4) and (5) show, the minus mode has a smaller equivalent inductance. Hence, the propagation speed of the minus mode is larger, and as (13) shows, an out-of-phase noise appears at the end of the victim line. Assuming that aggressors are excited by step inputs and using the low-loss approximation, the noise voltage at the end of a quiet victim line is

$$V_{\text{identical}}(t) = -\frac{\sum_{\text{All Aggressors}} l_{vi}}{\sqrt{\sum_{\text{All Aggressors}} l_{vi}^2}} \frac{Z_0}{R_{\text{tr}} + Z_0} V_{\text{F-in}} e^{-(r\ell/2Z_0)} \quad (14)$$

for

$$\sqrt{c(l - \sum_{\text{All Aggressors}} l_{vi})} \ell < t < \sqrt{c(l + \sum_{\text{All Aggressors}} l_{vi})} \ell$$

which is the time interval that the minus mode has arrived at the end of victim line and the plus mode has not arrived yet. For

$$t > \sqrt{c(l + \sum_{\text{All Aggressors}} l_{vi})} \ell$$

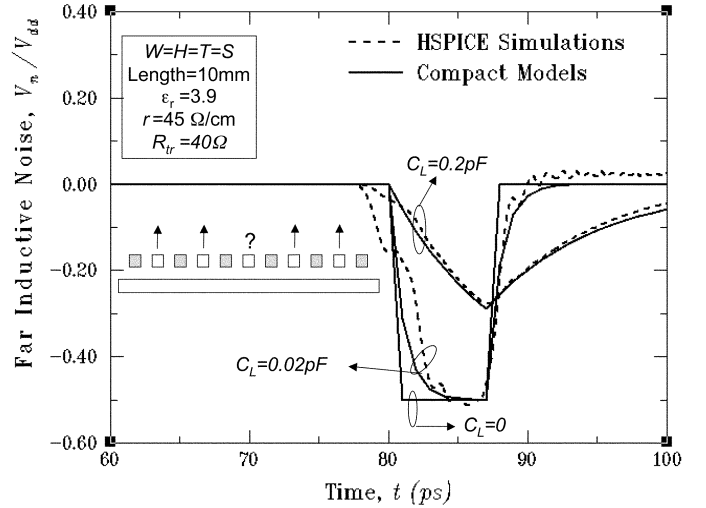


Fig. 3. Induced noise on the quiet line when all signal lines are shielded by two power/ground lines. HSPICE simulations are compared with compact models for different load capacitances. The input of the aggressors is a positive voltage, $V_{\text{dd}} u_o(t)$.

the plus and minus modes cancel impact of each other and the noise voltage can be ignored. $V_{\text{F-in}}$ in (14) is the input voltage of the aggressor lines and ℓ is the length of interconnects. If aggressors switch from logic 0 to 1, $V_{\text{F-in}}$ is $+V_{\text{dd}}$, and if they switch from logic 1 to 0 it is $-V_{\text{dd}}$. The noise duration is

$$t_n = \frac{\ell}{v^+} - \frac{\ell}{v^-} = (ToF) \sqrt{\sum_{\text{All Aggressors}} \left(\frac{l_{vi}}{l_s}\right)^2} \quad (15)$$

where ToF is the time-of-flight. In the case that there is a large capacitance at the end of the victim line, the load capacitance is charged through the characteristic impedance of the line and the noise voltage is

$$V_{\text{load}} = \begin{cases} V_{\text{open}}(1 - e^{-t/Z_0 C_L}) & t \leq t_n \\ V_{\text{open}}(1 - e^{-t_n/Z_0 C_L}) e^{-t/Z_0 C_L} & t > t_n \end{cases} \quad (16)$$

where V_{open} is given by (14) and $t = 0$ corresponds to ToF . As an example, the induced noise on a middle quiet line is plotted versus time in Fig. 3 when all signal lines are shielded from both sides by power/ground lines. All inductance and capacitance values that are used in compact models and HSPICE simulations are extracted by RAPHAEL [14]. The circuit shown in

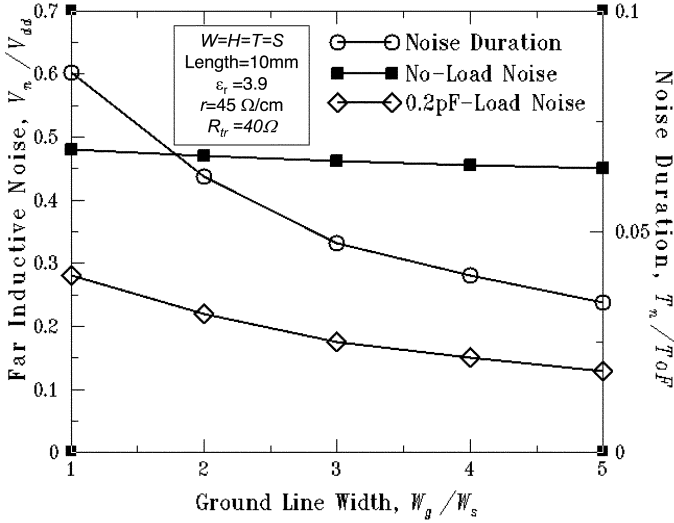


Fig. 4. Peak and duration of far inductive noise versus the ground line width for the structure shown in Fig. 2. Increasing ground line width reduces all mutual inductances approximately by the same ratio. The peak noise of an open-ended line is independent of ground line width.

Fig. 2 is used for HSPICE simulations wherein 1000 segments are in series to represent distributed RLC lines.

It is worthwhile to note that plus and minus modes do not completely cancel each other for $t > t_n$, and there is a small noise voltage for $t > t_n$, which can be easily seen in the curve associated with $C_L = 0.02$ pF in Fig. 3. The amplitude of this noise is, however, very small compared to the peak noise voltage because of which it is ignored in this analysis. One can easily model the level of this noise by taking into account the difference between the attenuations of the plus and minus modes. The negligible noise voltage can last several ToF periods because it has to discharge through the driver of the victim line that is connected to the other end of the line. The same behavior can be seen in the crosstalk of two adjacent RLC lines [5].

Equation (14) shows that the peak noise voltage of an open-ended line is independent of the absolute values of the inductive couplings. This means that if all mutual couplings are made smaller by the same factor, e.g., by making power/ground lines wider, the peak noise does not change. The reason is that the aggressor and victim lines are identical, and their natural frequencies are the same. Hence, the aggressors and the victim line *resonate*, and even a very weak coupling can cause a considerable noise voltage.

Fig. 4 shows noise voltage and duration versus ground line width for the structure shown in Fig. 3. Making ground lines wider and not changing other dimensions reduces all mutual inductances almost equally.

It should be noted that the low-loss approximation used in this analysis predicts the peak noise voltage accurately even for lossy lines as long as aggressors are driven by step inputs because (10) is always valid for fast transitions on a line [13]. For the finite rise time cases, the validity of low-loss approximation depends on the rise time of outputs of drivers, t_r , and the resistance and inductance per unit length of interconnects as

$$\frac{r}{\left(\frac{2}{t_r}\right)l} < 1. \quad (17)$$

For instance, for the 90- and 45-nm technology nodes, the International Technology Roadmap for Semiconductors (ITRS) projects on-chip clock frequencies of 4.2 and 15.0 GHz, respectively [16]. The signal rise time at the output of drivers is normally less than 10% of the clock cycle. For the 90-nm node, therefore, interconnects with a resistance per unit length of 527 Ω/cm ($W = T = 0.65$ μm) or smaller will satisfy (17). For the 45-nm node, however, interconnects with resistance per unit lengths smaller than 1583 Ω/cm ($W = T = 0.38$ μm) will satisfy (17). Thereby, low-loss approximation is valid for most global interconnects, and as technology advances, it becomes more and more accurate.

IV. NONIDENTICAL VICTIM AND AGGRESSOR LINES

Equations (14) and (15) do not hold if aggressors and a quiet line have different capacitance and inductance values. In this case, far aggressors can be modeled by the single low-loss RLC line model given by

$$V_f(x, t) = \frac{Z_{of}}{Z_{of} + R_{tr}} V_{F-in} e^{-(r_f l / 2Z_{of})} u(t - x\sqrt{l_f c_f}) \quad (18)$$

where l_f and c_f are the far lines' inductance and capacitance per unit length, respectively, Z_{of} is the far lines' characteristic impedance, and $u(t)$ is a unit step function. This is based on a loosely coupled assumption that the impact of the quiet line on the aggressors can be neglected [15]. If the coupling between the aggressors is not negligible, their common mode can be used. The differential equation for the victim line is given by

$$\frac{\partial^2 V^2(x, t)}{\partial x^2} = l_v c_v \frac{\partial^2 V(x, t)}{\partial t^2} + r_v c_v \frac{\partial V(x, t)}{\partial t} + \sum_{\text{All Aggressors}} l_{vi} c_f \frac{\partial^2 V_f(x, t)}{\partial t^2} \quad (19)$$

where r_v , l_v and c_v are resistance, inductance, and capacitance per unit length of the victim line, respectively. The voltage at the end of the victim line for $x\sqrt{l_v c_v} < t < x\sqrt{l_f c_f}$ is

$$V_{\text{nonidentical}}(t) = \frac{-2Z_{of} V_{F-in} \sum_{\text{All Aggressors}} l_{vi} c_f}{Z_{of} + R_{tr} (l_f c_f - l_v c_v)} \times \left[\frac{l\sqrt{l_f c_f} - t}{l\sqrt{l_f c_f} - l\sqrt{l_v c_v}} e^{-(r_v l / 2Z_{ov})} + \frac{t - l\sqrt{l_v c_v}}{l\sqrt{l_f c_f} - l\sqrt{l_v c_v}} \times e^{-1.15(r_f l / 2Z_{of})} \right] \quad (20)$$

and at all other times is approximately zero. In most cases, the two exponents inside the bracket are close to each other, and (20) can be approximated by

$$V_{\text{nonidentical}}(t) = \frac{-2Z_{of}}{Z_{of} + R_{tr}} V_{F-in} \frac{\sum_{\text{All Aggressors}} l_{vi} c_f}{(l_f c_f - l_v c_v)} \times \left[\exp\left(-\frac{r_v l}{2Z_{ov}}\right) \right]. \quad (21)$$

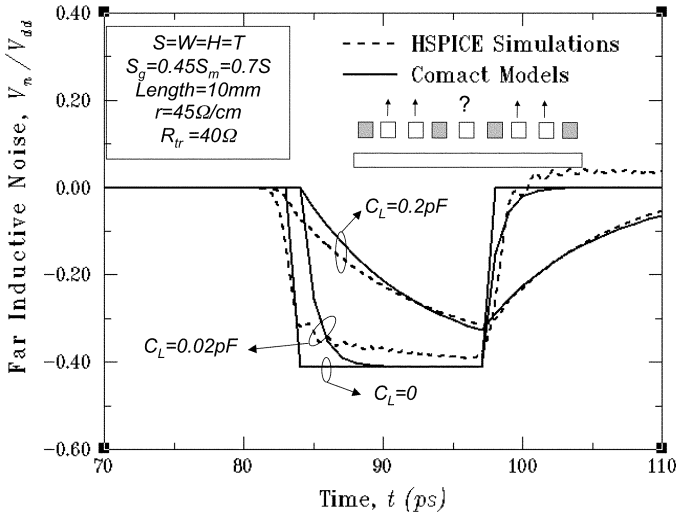


Fig. 5. Induced noise at the end of a quiet line for three different load capacitances. HSPICE simulations are compared with compact models. S_g and S_m are optimized so that the worst-case delay is minimized [7].

By substituting (21) in (16), the peak noise voltage can be found when there is a load capacitance. An example of this case is when a victim line that is shielded from both sides is attacked by aggressors that are shielded only from one side. The noise voltage at the end of the victim line is plotted versus time in Fig. 5 wherein HSPICE simulations verify compact expressions.

Unlike the previous case, the induced noise in the victim line travels either faster or slower than the signal in aggressors, and far and victim lines do not resonate. The peak noise of an open-ended line is, therefore, proportional to the total mutual inductance, and the noise duration is independent of the mutual couplings.

For most practical cases that the ratio of mutual inductance to self inductance is relatively small (e.g., less than 0.1) loosely coupled approximation is fairly accurate (typically less than 5% error) as long as aggressors and a victim line are not identical. Using the loosely coupled approximation for the identical victim and aggressor lines results in an impulse function in the solution. The reason is that for the identical lines, aggressor and victim lines resonate and ignoring the impact of the victim line on aggressors makes the solution unrealistic. Hence, the solutions that are presented for identical and nonidentical lines cannot be used interchangeably.

Another application for (21) is when a quiet line is attacked by far lines which are two metal levels below the victim line. Lines in lower metal levels usually have a smaller cross-sectional area and are more resistive. The number of signal lines between power/ground lines is typically larger than that of the top-most metal level. Having more than two signal lines between power/ground lines makes it more difficult to model far lines in lower metal levels because different signal lines have different inductance values based on their distance from power/ground lines. The worst case far inductive noise occurs when all aggressors switch simultaneously in the same direction because if one of them switches in an opposite direction it cancels the impact of others. Since far lines that are surrounded by power/ground

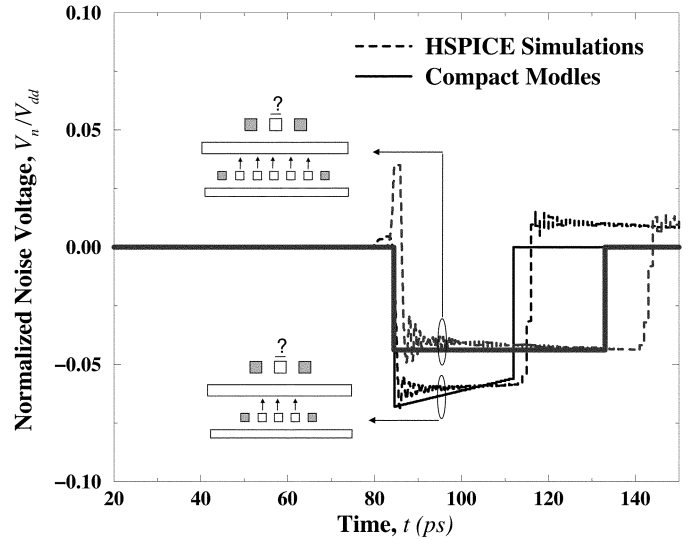


Fig. 6. Voltage at the end of a quiet victim line when it is affected by either three or five far aggressors that are two metal levels below the victim line. Line resistance for the two top levels is $45 \Omega/\text{cm}$ and for the lower metal levels is $90 \Omega/\text{cm}$.

lines are highly coupled, both inductively and capacitively, their voltages are close as they switch, and therefore with a good approximation, all of them can be modeled by a single equivalent line. The equivalent line's capacitance is equal to the total capacitance of the lines to lower and upper orthogonal lines and power/ground lines. The inductance and resistance of the equivalent line is the inductance and resistance of the lines in parallel.

The above mentioned method is verified against HSPICE simulations in Fig. 6 wherein a quiet victim line is attacked by either three or five interlevel far aggressors. Although there is a larger mutual coupling between the aggressors and the victim line in the five-aggressor case, the peak noise voltage for the five-aggressor case is smaller. The reason is that the $(l_v c_v - l_f c_f)$ term in (21) for the three-aggressor case is smaller than that of the five aggressor case. In both cases, the errors in peak and duration of noise are less than 10% and 18%, respectively. It should be noted that HSPICE simulations show a very narrow pulse with large amplitude for the five-aggressor case. This narrow pulse is not captured by the compact models due to approximating the five aggressors by an equivalent line. In practice, this ultra-narrow pulse (less than 2 ps wide) has no impact because a very small load capacitance can filter it out.

V. NOISE VOLTAGE-TIME INTEGRAL

Both peak and duration of noise are important because even a large noise voltage with a very small duration cannot cause false switching and it will be filtered out by the load capacitance. The noise voltage-time integral can be, therefore, defined as a figure of merit. Using (16), it can be shown that the noise voltage-time integral is

$$\int_0^{\infty} V_n(t) dt = V_{\text{open}} t_n \quad (22)$$

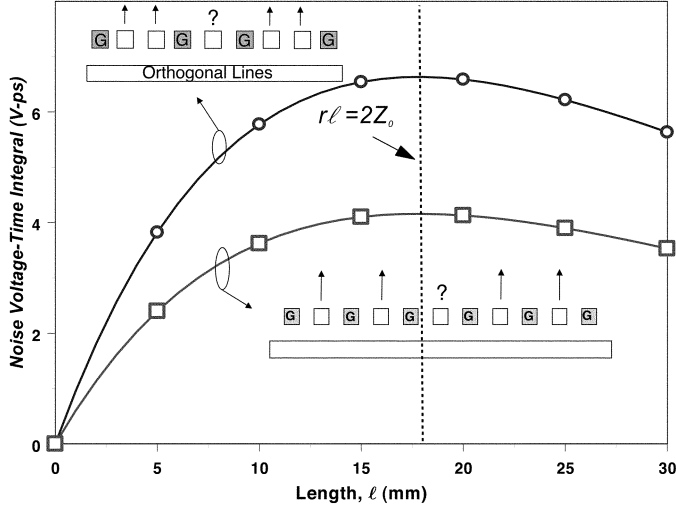


Fig. 7. Noise voltage-time integral versus interconnect length. V_{dd} is assumed to be 1 V. The value of this integral is independent of the load capacitance.

which is independent of the load capacitance. For both identical and nonidentical line cases (22), is equal to

$$\int_0^{\infty} V_n(t) dt = \frac{2Z_{0f}}{Z_{0f} + R_{tr}} \frac{\sum_{\text{All Aggressors}} l_{vi} c_f}{(\sqrt{l_f c_f} + \sqrt{l_v c_v})} V_{dd} \ell e^{-(r_v \ell / 2Z_{0v})}. \quad (23)$$

It should be noted that for the case that lines are identical parameters corresponding to the victim and far lines are equal. By taking the derivative of (23) with respect to interconnect length, the length at which the noise voltage-time integral attains its maximum can be identified. The noise voltage-time is maximized when interconnect resistance is equal to twice characteristic impedance:

$$r\ell = 2Z_{0v}. \quad (24)$$

It is therefore imperative to avoid interconnect lengths close to $2Z_0/r$ (Fig. 7). Knowing this fact can be especially useful for repeater insertion algorithms.

VI. NEAR AND FAR AGGRESSORS

When a victim line is affected by both near and far aggressors, total crosstalk can be found by using the superposition theorem. The Sections VI-A and B show how models that are derived in the previous sections can be used to find total crosstalk caused by near and far aggressors. First, the crosstalk induced by intralevel aggressors is modeled, and then, the impact of interlevel far lines is modeled.

A. Near and Intralevel Far Aggressors

Following the path illustrated in Fig. 8, crosstalk noise voltage for the case that near and intralevel far aggressors switch simultaneously can be calculated using superposition

theorem and the crosstalk model presented in Section III. In this manner, the peak and duration of noise can be written as

$$V_{\text{peak}} = V_{dd} \left[\left(\frac{\sum_{\text{All FarPairs}} l_{pi}}{\sqrt{\sum_{\text{All FarPairs}} l_{pi}^2}} + 1 \right) \frac{Z_{0p}}{\frac{R_{tr}}{2} + Z_{0p}} \times e^{-((r\ell/2)/2Z_{0p})} - \frac{Z_{dif}}{R_{tr} + Z_{dif}} e^{-(r\ell/2Z_{dif})} \right] \quad (25)$$

and

$$t_{\text{peak}} = T_o F_{\text{com}} \sqrt{\sum_{\text{All FarPairs}} \left(\frac{l_{pi}^2}{l_p^2} \right)} \quad (26)$$

where all variables are defined in Fig. 8. The models are verified against HSPICE simulations in Fig. 9 wherein the contributions of near and far aggressors are illustrated with different patterns.

B. Near and Interlevel Far Aggressors

The same methodology can be used for the far lines which are two metal levels below the victim line. The noise voltage when far lines switch and the near line is quiet can be found by the models derived in Section IV. The victim and near aggressor have equal voltages and their common mode can be used to find the noise caused by intralevel far lines as

$$V_{f\text{-interlevel}} = V_{\text{nonidentical}}(t, l_{vi} = l_{pi}, l_v = l_p, c_v = c_p, l_f = l_{eqv}, c_f = c_{eqv}). \quad (27)$$

To find the noise voltage when the near aggressor switches and far lines stay quiet, impact of far lines can be ignored because the inductances and capacitances of victim and far lines are different and they do not resonate. This makes the analysis simpler. The noise voltage caused by a near aggressor is

$$V_{\text{near}}(t) = \frac{Z_{\text{com}}}{R_{tr} + Z_{\text{com}}} V_{N\text{-in}} e^{-(r\ell/2Z_{\text{com}})} \times \left[u(t - \ell\sqrt{c_{\text{com}}l_{\text{com}}}) \right] - \frac{Z_{\text{dif}}}{R_{tr} + Z_{\text{dif}}} V_{N\text{-in}} e^{-(r\ell/2Z_{\text{dif}})} \times \left[u(t - \ell\sqrt{c_{\text{dif}}l_{\text{dif}}}) \right] \quad (28)$$

where

$$l_{\text{com}} = l_s + l_m \quad (29)$$

and

$$c_{\text{com}} = c_g + c_{\text{orth}}. \quad (30)$$

Total noise when both near and intralevel far aggressors switch is equal to the summation of (27) and (28), which is verified in Fig. 10.

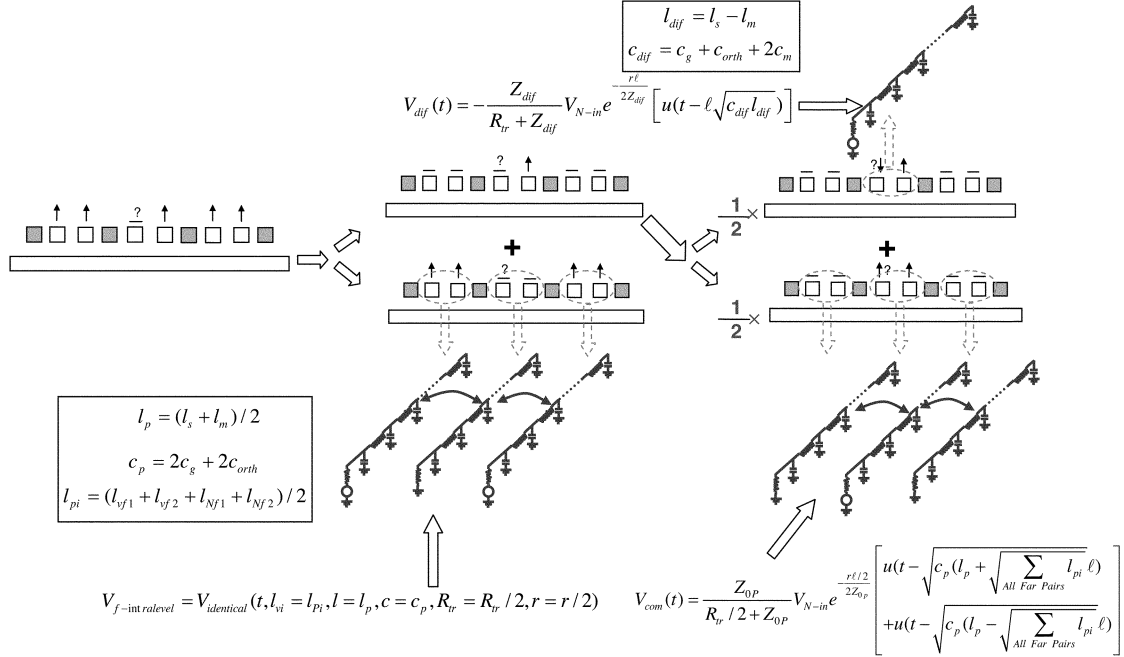


Fig. 8. Proposed methodology for modeling crosstalk induced by near and intralevel far aggressors using superposition theorem and models presented in Section III.

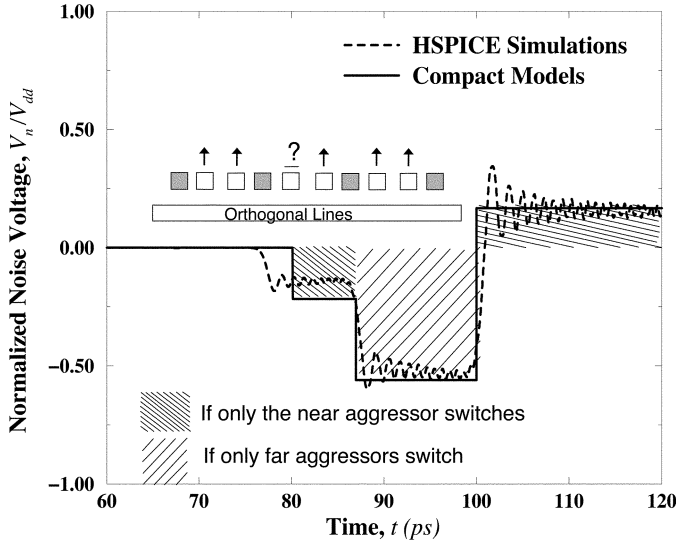


Fig. 9. Noise voltage at the end of a quiet victim line when all intralevel near and far aggressors switch simultaneously.

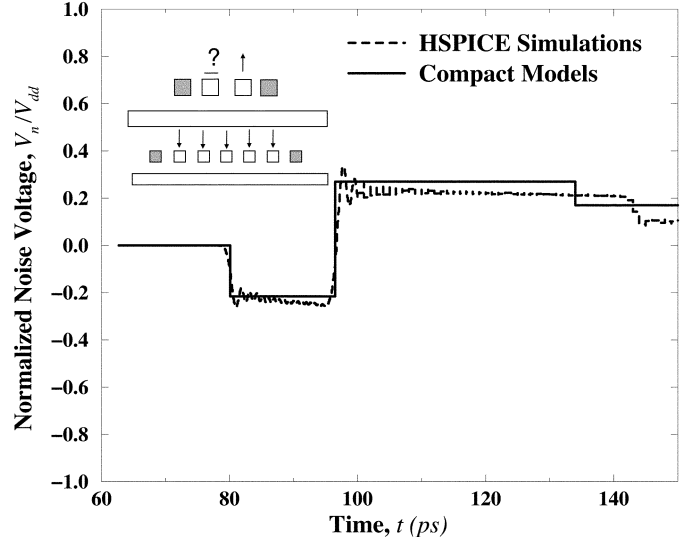


Fig. 10. Noise voltage at the end of quiet victim line when near and intralevel far aggressors switch simultaneously.

VII. INTEGRATED CROSSTALK MODEL

The results found in the previous section can be incorporated in an integrated expression for crosstalk caused by all near, intra and interlevel far aggressors given by

$$V_{\text{total}} = V_{f\text{-interlevel}}(t - t_{f\text{-interlevel}}) + [V_{\text{com}}(t - t_{\text{near}}) + V_{\text{dif}}(t - t_{\text{near}})] + V_{f\text{-intralevel}}(t - t_{f\text{-intralevel}}) \quad (31)$$

where $t_{f\text{-interlevel}}$, $t_{f\text{-intralevel}}$ and t_{near} are times at which different sets of aggressors switch. If there is a large load capacitance at the end of the victim line, the RC charge-up equation should be used for each time period that the open-ended noise voltage is constant to find the peak noise voltage.

The integrated model is compared against HSPICE simulations in Fig. 11 where noise at the end of a victim line is plotted versus time. Far aggressors switch anti-phase compared to the near aggressor. Intra-level far aggressors switch 20 ps (far noise duration in this example) later than other aggressors. It can be seen that the error in the peak noise voltage is less than 15%.

Fig. 11 shows that far aggressors can cause a prohibitively large crosstalk. The major way to decrease crosstalk is to avoid very small line resistance. For instance, for the case shown in Fig. 11, by increasing resistance per unit length from 45 Ω/cm to 270 Ω/cm , the peak crosstalk voltage reduces from 0.8 V_{dd} to 0.25 V_{dd} . Increasing line resistance, however, increases interconnect latency. Hence, there is a tradeoff between crosstalk

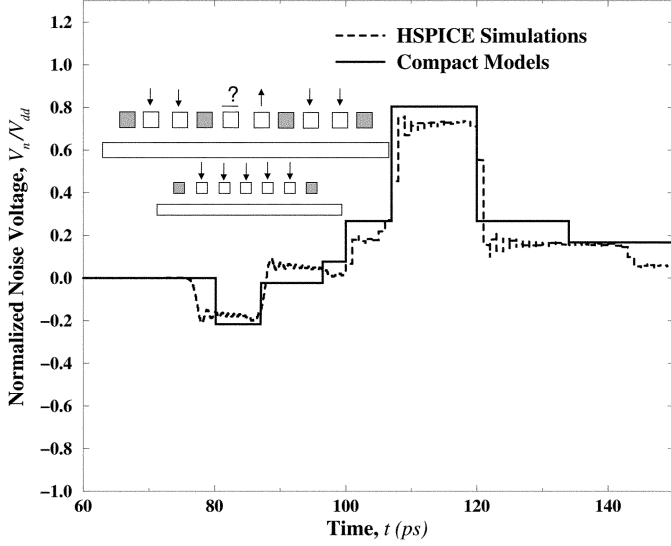


Fig. 11. Total noise caused by near, far intra and interlevel aggressors. Far Lines switch in the opposite direction and intralevel far aggressors switch 20 ps (the duration of intralevel noise in this example) after near and interlevel far aggressors. This shows the worst case scenario for crosstalk.

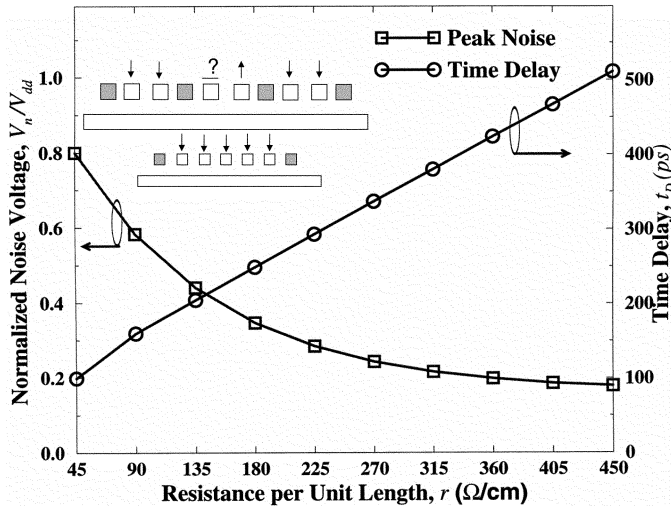


Fig. 12. Worst case noise voltage and interconnect latency versus resistance per unit length of interconnects in the top metal level for the structure shown in Fig. 13. It has been assumed that interconnects in the two lower metal levels have a resistance per unit length two times larger than that of the top two metal levels.

and latency. Fig. 12 has plotted crosstalk and latency versus line resistance for the same structure shown in Fig. 11.

Inserting repeaters is an alternative way to reduce crosstalk and avoid large latency. This is shown in Fig. 13 where the worst-case crosstalk and latency are plotted versus line resistance assuming that optimal repeaters are inserted [6]. Latency increases with line resistance more slowly compared to the latency of nonbuffered interconnects shown in Fig. 12. Hence, wiring density and crosstalk can both be improved by inserting repeaters with a tolerable increase in interconnect latency.

VIII. OPTIMAL WIRE WIDTH

It was illustrated in the previous section that designers can lower crosstalk and increase wiring density by using smaller wire dimensions at the price of larger interconnect latencies. Re-

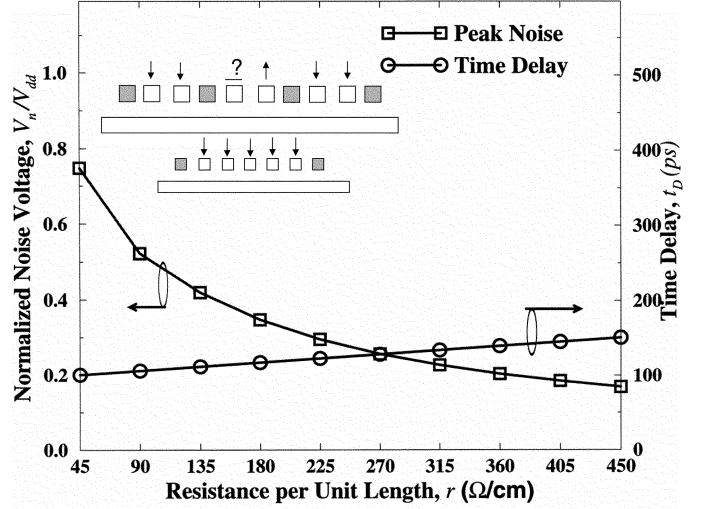


Fig. 13. Worst case noise voltage and interconnect latency versus resistance per unit length of interconnects in the top metal level when optimal repeaters are used. All parameters are the same as those in Fig. 14.

cently, an interconnect-centric methodology is proposed to optimize the width of global interconnects to maximize data flux density and minimize latency simultaneously [9], [10]. Data flux density is the product of interconnect bandwidth and reciprocal pitch, which represents the number of bits per second that can be transferred per unit width of interconnects. It was rigorously shown that the optimal wire width is independent of interconnect length and is equal to [8], [10]

$$W_{\text{opt}} = 2.53c_0 \sqrt{\frac{c_g \rho}{\varepsilon_r A_r} R_0 C_0} \quad (32)$$

where c_0 is the speed of light in free space, ρ is metal resistivity, A_r is the interconnect aspect ratio, and $R_0 C_0$ is the intrinsic delay of repeaters. The optimal wire width is in the shallow RLC region, where the difference between RC and RLC model latencies is only 10% [9], [10]. Using the optimal wire width, also offers the best tradeoff between energy dissipation and data flux density, requires a small repeater area for global interconnects (less than 1% of the chip area), and reduces via blockage considerably [9]. In this section, the compact models for multilevel interconnect crosstalk will be used to show that utilizing optimal wire width, also makes the crosstalk noise voltage small and constant in all generations of technology.

It is shown in the Appendix that the peak crosstalk voltage induced by all near and far aggressors can be written in terms of W/W_{opt} as

$$V_{\text{load}} = V_{\text{dd}} \left[0.39 \frac{\sum_{\text{All FarPairs}} l_{\text{pi}}}{\sqrt{\sum_{\text{All FarPairs}} l_{\text{pi}}^2}} + 0.1 + 0.78 \frac{\sum_{\text{All Aggressors}} l_{\text{vi}} c_{f-eq}}{(l_{f-eq} c_{f-eq} - l_p c_p)} \right] \times \left[1 - \exp\left(-3.39 \frac{W^2}{W_{\text{opt}}^2}\right) \right] \times \sqrt{\sum_{\text{All FarPairs}} \left(\frac{l_{\text{pi}}^2}{l_p^2} \right)}. \quad (33)$$

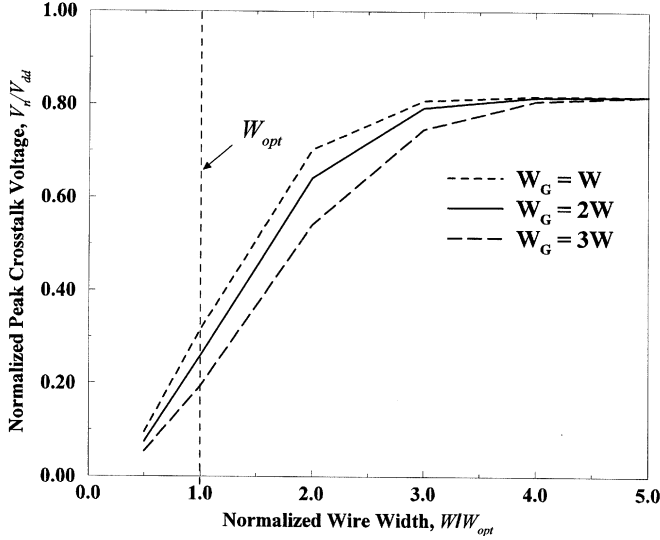


Fig. 14. Normalized peak crosstalk voltage versus normalized wire width for three power/ground line widths. It has been assumed that optimal repeaters are inserted.

The first bracket in (33) represents the open-ended noise voltage and is independent of wire width assuming that all cross-sectional dimensions scale proportionally. The second bracket represents the impact of input capacitance of repeaters. As wire width decreases, the length of each segment between two repeaters decreases; hence the noise duration decreases and the peak noise voltage becomes smaller.

Equation (33) proves that crosstalk remains constant in various technology generations if the ratio of wire width over the optimal wire width remains constant. Peak crosstalk voltage is plotted versus W/W_{opt} ratio in Fig. 14 for ground line widths of W , $2W$ and $3W$. It is evident that a W/W_{opt} of larger than 1 can result in a substantially larger peak crosstalk voltage. It also shows that using wider ground line widths can slightly lower crosstalk. Hence, by using the optimal wire width for signal lines and twice of that for power/ground lines, crosstalk will always be limited to $0.25 V_{dd}$.

The analysis presented in this section is independent of interconnect length because by optimal repeater insertion, the segment length between two repeaters is the same for interconnects with different lengths.

IX. CONCLUSION

For the first time, compact physical models were derived for total noise caused by virtually all near and far aggressors. Far lines that are two metal levels below a victim line were also considered. Far inductive noise was modeled for two basic cases that aggressors and a victim line are identical or nonidentical. For both cases it was shown that noise voltage–time integral was maximized when line resistance became equal to twice the characteristic impedance of the lines, which can be quite useful for repeater insertion algorithms. Having the solutions for identical and nonidentical lines and using superposition theorem, an integrated model was derived for total noise caused by all near and far aggressors. It was shown that the worst-case scenario

is when far aggressors switch antiphase compared to a near aggressor. It was also shown that crosstalk can be prohibitively large if lines have a small resistance. Hence, there is a tradeoff between latency and crosstalk. For instance, for 10-mm-long interconnects it is shown that the worst case crosstalk can be reduced from 0.80 to $0.25 V_{dd}$ by increasing line resistance from 45 to $270 \Omega \cdot \text{cm}$, which increases latency by 230% and 30% for nonbuffered and optimally buffered interconnects, respectively. Finally, it was shown that the worst-case peak crosstalk voltage is a function of the ratio of signal wire width to the optimal wire width, which maximizes data flux density-reciprocal latency product. In this way, it was proven that by using the optimal wire width for signal interconnects and twice of that for power and ground lines the worst-case peak crosstalk becomes constant and less than $0.25 V_{dd}$ for all generations of technology.

APPENDIX

The optimal number and output resistance of repeaters in the *RLC* regime are [6]

$$k_{opt} = \frac{0.95 R_{int}}{\sqrt{Z_{com} Z_{dif}}} \quad (34)$$

and

$$R_{tr} = \frac{R_0}{h_{opt}} = \frac{\sqrt{Z_{dif} Z_{com}}}{1.15} \quad (35)$$

respectively. A typical value for the optimal R_{tr} would be 35Ω for a dielectric constant of 3.9 and 50Ω for a dielectric constant of 2.5, which are projected for the 45-nm technology node by the ITRS [16]. By substituting (34) and (35) in (25), the peak noise voltage induced by intralevel interconnects, can be written as

$$\begin{aligned} V_{intralevel} &= V_{dd} \left[\left(\frac{\sum_{\text{All FarPairs}} l_{pi}}{\sqrt{\sum_{\text{All FarPairs}} l_{pi}^2}} + 1 \right) \frac{1}{\frac{1}{1.15} \sqrt{\frac{Z_{dif}}{Z_{com}}} + 1} \right. \\ &\quad \times e^{-0.525 \sqrt{(Z_{dif}/Z_{com})}} - \frac{1}{\frac{1}{1.15} \sqrt{\frac{Z_{com}}{Z_{dif}}} + 1} \\ &\quad \left. \times e^{-0.525 \sqrt{(Z_{com}/Z_{dif})}} \right], \quad (36) \end{aligned}$$

which is independent of resistance per unit length of interconnects, and is determined by the $\sqrt{Z_{com}/Z_{dif}}$ and the mutual inductances between far aggressors and the victim line. The ratio of the common and differential mode characteristic impedances is equal to [7]

$$\frac{Z_{com}}{Z_{dif}} = \sqrt{\left(1 + \frac{2c_m}{c_g}\right) \left(1 + \frac{2c_m}{c_g + c_{ortho}}\right)} \quad (37)$$

where c_m is the mutual capacitance between two near signal lines and c_g is the capacitance between a signal line and a nearby ground line, and c_{ortho} is the capacitance between a signal line and the orthogonal lines. For the optimal spacing case, $c_m = 0.45c_g$ [8], $\sqrt{Z_{com}/Z_{dif}}$ can be approximated by 1.28 for a

wide range of c_{ortho}/c_g ($0.3 < c_{ortho}/c_g$) with less than 4% error. In this manner, (36) can be rewritten as

$$V_{\text{intra-level}} = V_{\text{dd}} \left[0.39 \frac{\sum_{\text{All FarPairs}} l_{\text{pi}}}{\sqrt{\sum_{\text{All FarPairs}} l_{\text{Pi}}^2}} + 0.1 \right]. \quad (38)$$

The same approach can be used for the crosstalk caused by interlevel aggressors. By substituting (34) and (35) in (21), the peak open-ended noise caused by interlevel aggressors can be rewritten as

$$V_{\text{nonidentical}}(t) = 2 \frac{\sum_{\text{All Aggressors}} l_{\text{vi}} c_{f-eq}}{(l_{f-eq} c_{f-eq} - l_p c_p)} \times \frac{1}{\frac{1}{1.15} \sqrt{\frac{Z_{\text{dif}}}{Z_{\text{com}}}} + 1} e^{-0.525 \sqrt{(Z_{\text{dif}}/Z_{\text{com}})}} \quad (39)$$

which can be similarly approximated by

$$V_{\text{interlevel}}(t) = 0.78 \frac{\sum_{\text{All Aggressors}} l_{\text{vi}} c_{f-eq}}{(l_{f-eq} c_{f-eq} - l_p c_p)}. \quad (40)$$

The peak open-ended noise voltage is the summation of (38) and (40)

$$V_{\text{open}} = V_{\text{dd}} \left[0.39 \frac{\sum_{\text{All FarPairs}} l_{\text{pi}}}{\sqrt{\sum_{\text{All FarPairs}} l_{\text{Pi}}^2}} + 0.1 + 0.78 \frac{\sum_{\text{All Aggressors}} l_{\text{vi}} c_{f-eq}}{(l_{f-eq} c_{f-eq} - l_p c_p)} \right]. \quad (41)$$

To find the peak noise voltage, the impact of the load capacitance should be taken into account, too. The load capacitance is charged by the time constant of $Z_0 C_L$. The peak noise voltage is, therefore, equal to

$$V_{\text{load}} = V_{\text{open}} \left[1 - \exp\left(\frac{-t_n}{Z_0 C_L}\right) \right]. \quad (42)$$

The duration of noise pulse is given by (26) and can be written as

$$t_n = \frac{l_{\text{seg}} \sqrt{\epsilon_r}}{c_0} \sqrt{\sum_{\text{All FarPairs}} \left(\frac{l_{\text{pi}}^2}{l_p^2} \right)}. \quad (43)$$

By substituting (34) in (43), the noise duration is

$$t_n = \frac{1.05 \sqrt{\epsilon_r} Z_{\text{com}} Z_{\text{dif}}}{r c_0} \sqrt{\sum_{\text{All FarPairs}} \left(\frac{l_{\text{pi}}^2}{l_p^2} \right)}. \quad (44)$$

Using the equation for the optimal wire width, (32), the noise duration can be written in terms of W/W_{opt} :

$$t_n = 5R_0 C_0 \frac{W^2}{W_{\text{opt}}^2} \sqrt{\sum_{\text{All FarPairs}} \left(\frac{l_{\text{pi}}^2}{l_p^2} \right)}. \quad (45)$$

The last parameter in (42) that should be identified is the load capacitance, C_L . Assuming that optimal repeaters are inserted, the load capacitance would be the input capacitance of an optimal repeaters given by [6]

$$C_L = C_0 h_{\text{opt}} = \frac{1.15 R_0 C_0}{\sqrt{Z_{\text{dif}} Z_{\text{com}}}}. \quad (46)$$

A typical value for C_L is 98 fF at the 90-nm technology node, and 26 fF at the 45-nm technology node based on the ITRS projections [16]. By substituting, (41), (45) and (46) in (42), the peak noise voltage considering the load capacitance is

$$V_{\text{Vload}} = V_{\text{dd}} \left[0.39 \frac{\sum_{\text{All FarPairs}} l_{\text{pi}}}{\sqrt{\sum_{\text{All FarPairs}} l_{\text{Pi}}^2}} + 0.1 + 0.78 \frac{\sum_{\text{All Aggressors}} l_{\text{vi}} c_{f-eq}}{(l_{f-eq} c_{f-eq} - l_p c_p)} \right] \times \left[1 - \exp\left(-3.39 \frac{W^2}{W_{\text{opt}}^2}\right) \times \sqrt{\sum_{\text{All FarPairs}} \left(\frac{l_{\text{pi}}^2}{l_p^2} \right)} \right]. \quad (47)$$

REFERENCES

- [1] G. V. Kopcsay, B. Krauter, D. Widiger, A. Deutsch, B. J. Rubin, and H. H. Smith, "A comprehensive 2-D inductance modeling approach for VLSI interconnects: Frequency-dependent extraction and compact circuit model synthesis," *IEEE Trans. VLSI Syst.*, vol. 10, pp. 665–711, Dec. 2002.
- [2] M. W. Beattie and L. T. Pilleggie, "On-chip induction modeling: Basics and advanced methods," *IEEE Trans. VLSI Syst.*, vol. 10, pp. 712–729, Dec. 2002.
- [3] T. Sakurai, "Closed form expressions for interconnection delay, coupling and crosstalk in VLSIs," *IEEE Trans. Electron Devices*, vol. 40, pp. 118–124, Jan. 1993.
- [4] A. Deutsch *et al.*, "On-chip wiring design challenges for gigahertz operation," *Proc. IEEE*, vol. 89, pp. 529–554, Apr. 2001.
- [5] J. A. Davis and J. D. Meindl, "Compact distributed RLC interconnect models. II. Single line transient, time delay, and overshoot expressions," *IEEE Trans. Electron Devices*, vol. 47, pp. 2068–2087, Nov. 2000.
- [6] R. Venkatesan, J. A. Davis, and J. D. Meindl, "Compact distributed RLC interconnect models—Part IV: Unified models for time delay, crosstalk, and repeater insertion," *IEEE Trans. Electron Devices*, vol. 50, pp. 1094–1102, Apr. 2003.
- [7] A. Naemi, J. A. Davis, and J. D. Meindl, "Analytical models for coupled distributed RLC lines with ideal and nonideal return paths," in *IEDM Tech. Dig.*, Dec. 2001, pp. 689–692.
- [8] —, "Analysis and optimization of coplanar RLC lines for GSI," *IEEE Trans. Electron Devices*, pp. 985–994, June 2004.
- [9] A. Naemi, R. Venkatesan, and J. D. Meindl, "Optimal global interconnects for gigascale integration," *IEEE Trans. Electron Devices*, vol. 50, pp. 980–987, Apr. 2003.

- [10] A. Naeemi, J. A. Davis, and J. D. Meindl, "Optimal global interconnecting devices for GSI," in *IEDM Tech. Dig.*, Dec. 2002, pp. 319–322.
- [11] A. Kowalczyk *et al.*, "First-generation MAJC dual microprocessor," in *Proc. ISSCC*, 2001, pp. 236–237.
- [12] S. Rusu *et al.*, "The first IA-64 microprocessor," *IEEE J. Solid-State Circuits*, pp. 1539–1544, Nov. 2000.
- [13] M. Cases and D. M. Quinn, "Transient response of uniformly distributed RLC transmission lines," *IEEE Trans. Circuits Systems*, vol. CAS-27, Mar. 1980.
- [14] *RAPHAEL: Interconnect Analysis Program*. Sunnyvale, CA: TMA Inc., 1996.
- [15] D. B. Jarvis, "The effects of interconnections on high-speed logic circuits," *IEEE Trans. Electron. Comput.*, pp. 476–487, Oct. 1963.
- [16] "International Technology Roadmap for Semiconductors (ITRS) 2001," Semiconductor Industry Assoc., San Jose, CA.



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