

# A TICK BASED METHODOLOGY FOR RAPID PREDICTIVE CIRCUIT MODELING

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## ABSTRACT

The trend toward device miniaturization makes it necessary to scan a wide range of supply and threshold voltages and different types of FETs, so that optimal performance is obtained. Such a scan is best done by physically based models, so that predictive circuit modeling can be done to project and optimize circuit performance well into the next decade. Circuit simulators like HSPICE cannot be used for predictive modeling and thus a methodology is needed to use existing FET physical models to predict circuit performance. Such a methodology is proposed in this paper and verified against HSPICE. The proposed method works for a wide range of supply voltages, for a variety of FETs and avoids any numerical integration.

## 1. INTRODUCTION

The current trend toward device miniaturization makes it necessary to look at different supply and threshold voltages and different types of FETs for future generations, in order to identify the optimal configuration for a given application. The predictive capability depends both on the underlying FET models and the way these models are used to extract power and timing information. In this paper, the FET model proposed by Austin[1] is used. The model is transregional in nature, i.e. all regions of operation are modeled by maintaining continuity across regional boundaries while including lateral and vertical high field effects. This model was used successfully by Bhavnagarwala[2] to perform a minimum total power analysis. The model is entirely physical and avoids any parameter fitting. Therefore, the model is extremely useful for predicting the performance of technology generations over the next decade.

Predictive circuit modeling for near term generations can be done in a way similar to that in [3]. In fact, using our physical FET models, one can calculate some of the critical BSIM parameters physically. Due to lack of space, the expression for only one such parameter - DVT0( $V_T$  rolloff

coefficient), is given:

$$DVT0 = \frac{4}{\zeta} \left( 1 - \frac{\gamma \sqrt{2\phi_F} - \frac{qN_A}{\epsilon_{Si}\lambda^2}}{\phi_{bi} - 2\phi_F} \right)$$

where,

$$\zeta = \left[ 1 + \frac{C_{ox}d}{\epsilon_{Si}} \left( 1 + \left( \frac{\lambda\epsilon_{Si}}{C_{ox}} \right)^2 \right) \right] (1 + \exp(-\lambda L))$$

where  $\gamma$  is the body bias factor and  $\lambda$  is the Eigen solution of  $\tan(\lambda d) = C_{ox}/\lambda\epsilon_{Si}$ .

Predictive circuit modeling for long-term future generations cannot be done using the approach proposed in [3], since more than 90% of the BSIM parameters are not predicted but kept the same as that for a previous generation. For long-term predictive circuit modeling, one would consider a chain of inverters since worst-case delay of a critical path can be simulated by replacing complex CMOS gates by their worst-case inverters [4]. A number of methods, mostly analytical [1],[5],[6],[7], have been proposed to model the inverter delay. Either most of them are based on the alpha-power law proposed by Sakurai[8], which is unsuitable for predictive modeling since it makes use of fit parameters, or are valid only in a small range of supply voltages[1]. Also, there exists a class of FETs-the buried channel accumulation(BCA) FETs, which have five regions of operation [9]. Although deriving analytical equations for the delay is possible for inverters using such FETs, the derivation would be subject to numerous assumptions and thus the resulting equations would be valid only in a small range of supply voltages. A method is desired that is valid over a wide range of supply voltages, makes use of physical models and is applicable for a variety of FETs, so that power and area optimizations can be performed by scanning a wide design space. Such a simulation method is proposed in this paper.

The proposed method is called *tick* based, wherein a "tick" is a point in time. Since SPICE parameters are readily available for the surface channel inversion(SCI) device, a SCI FET is considered in this paper to validate the tick based methodology.

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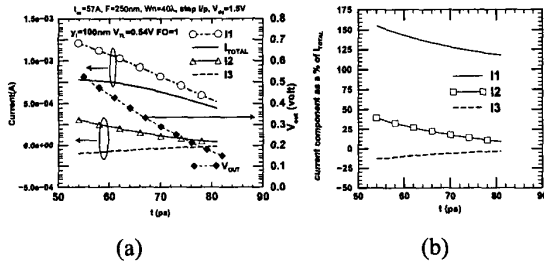


Fig. 1. (a) Various components of  $I_{linear}$ , (b) components of  $I_{linear}$  shown as a percentage of the total current

## 2. TICK BASED METHOD

Consider a critical path modeled by a chain of inverters. Assuming equal rise and fall times and a step input to the first stage, the delay of the critical path is [2]

$$T_{PD} = \frac{1}{f_{clk}} = \frac{n_{cp} T_{PDn} f_{ineff}}{b} \quad (1)$$

where  $n_{cp}$  is the number of gates in the critical path,  $f_{ineff}$  is the effective fan-in factor,  $b$  is the clock skew factor and  $T_{PDn}$  is the delay of the second or subsequent stages of the inverter chain. Since short-circuit power is less than 10% of total power in the 50nm generation [2], the short circuit current can be neglected while estimating delay and power to a first order. Thus  $T_{PDn}$  is just the discharge time through an nMOSFET. At the output of any stage, it is known that:

$$i = -C_L \frac{dV_{out}}{dt} \quad (2)$$

Integrating both sides,

$$\int_{V_{n-1}}^{V_n} dV_{out} = -\frac{1}{C_L} \int_{t_{n-1}}^{t_n} i dt \quad (3)$$

$n$  is the present tick and  $n-1$  is the previous tick.  $\Delta t (= t_n - t_{n-1})$ , the tick size, is made small enough to avoid computational errors. Typically this value is chosen to be 1% or less of the expected delay value. At each tick,  $\Delta V_T$ ,  $V_T$ ,  $V_{in}$ ,  $V_{DSAT}$  and  $V_{out}$  are evaluated.  $\Delta V_T$ , the threshold voltage rolloff, is dependent on  $V_d$  and thus needs to be evaluated at each tick.

The SCI device has three regions of operation - subthreshold, linear/non-saturated and saturated regions. The I-V equations for the three regions of operation are shown in Fig 2.

$V_{GS_n}$  is the input voltage at the present tick. This value is determined based on the input waveform. If the input is a step, then its value is  $V_{dd}$  for  $n \geq 0$ .  $V_{DS}$  is the same as  $V_{out}$ .  $V_{TO}$  is dependent on  $\Delta V_T$  which in turn depends on  $V_d$ . The value of  $\Delta V_T$  is found assuming  $V_d = V_{d,n-1}$ . If a

small enough tick size is chosen, then the error due to this assumption is extremely small. Lets first consider the subthreshold region of operation. The term involving  $V_{DS}$  can be neglected for most part of the output transition. Denoting the time-independent term in the I-V equation as  $K$ , we have:

$$I_d = K \cdot \exp \left\{ \frac{\beta}{\eta} \left[ V_{GS_n} - V_{TO} - \frac{\eta}{\beta} \right] \right\} \quad (4)$$

Using eqn (3) we have,

$$V_{out_n} - V_{out_{n-1}} = -\frac{1}{C_L} K \cdot \exp \left\{ \frac{\beta}{\eta} \left[ V_{GS_n} - V_{TO} - \frac{\eta}{\beta} \right] \right\} \Delta t \quad (5)$$

$V_{out}|_{n=0} = V_{dd}$  for a falling output. Using this initial condition and the above equation,  $V_{out}$  can be evaluated at each  $n$ , until  $V_{out}$  has reached 10% of the maximum value.

If  $V_{dd}$  is so low that the device always operates in the subthreshold region, then the delay can be found using analytical methods. It can be easily shown that the propagation delay in this case, assuming  $V_{dd} \gg \frac{3kT}{q}$ , is :

$$T_{PD} = \frac{C_L V_{DD}}{I_{ON}} \left( 1 - \frac{\eta}{\beta V_{DD}} \right) \quad (6)$$

Next, consider the linear/non-saturated region of operation. In this region, the I-V equation can be rewritten as a sum of three components:  $I_{linear} = I1 + I2 + I3$ , where,

$$\begin{aligned} I1 &= \kappa (V_{GS_n} - V_{TO}) V_{DS} \\ I2 &= \kappa \left\{ -\frac{1}{2} V_{DS}^2 \right\} \\ I3 &= \kappa \left\{ \frac{4}{3} \phi_F \frac{Q_{BO}}{C_{OX}} \left[ \left( 1 + \frac{V_{DS}}{2|\phi_F|} \right)^{3/2} - \left( 1 + \frac{3V_{DS}}{2\phi_F} \right) \right] \right\} \end{aligned}$$

where,

$$\kappa = \frac{WC_{ox}\mu_0}{L \left( 1 + \frac{V_d}{LE_c} \right) (1 + \theta(V_{GS_n} - V_T))}$$

Normally,  $I3$  contributes very little to the overall current. Thus this part can be evaluated using the previously calculated  $V_{DS}$  value ( $=V_{d,n-1}$ ). Fig 1(a) shows  $V_{out}$  and the various components of  $I_{linear}$ . The three components  $I1$ ,  $I2$ ,  $I3$  and  $V_{out}$  are plotted w.r.t. time. To get a better idea of how large  $I3$  is w.r.t.  $I_{linear}$ , the same curves are plotted as a % of the total current. This is shown in Fig 1(b).  $I3$  is seen to be less than 10% of  $I_{total}$  almost all throughout the decay period. Thus  $I3$  can be made time independent. The I-V equation can now be re-written as:

$$I_d = \kappa \left\{ (V_G - V_{TO}) V_{out} - \frac{1}{2} V_{out}^2 + k_5 \right\} \quad (7)$$

Subthreshold	$I_d = \frac{W\mu_0 C_{ox}}{Lm} \left[ \frac{1}{2\theta} \left( \sqrt{1 + \frac{4\eta\theta}{\beta}} - 1 \right) \right]^2 \left\{ 1 - \exp \left[ -\frac{\beta m}{\eta} V_{DS} \right] \right\} \exp \left\{ \frac{\beta}{\eta} \left[ V_{GS_n} - V_{TO} - \frac{\eta}{\beta} \right] \right\}$
Linear/Non-saturated	$I_d = \frac{WC_{ox}\mu_0}{L(1+\frac{V_d}{V_{TC}})(1+\theta(V_{GS_n}-V_T))} \left\{ (V_{GS_n} - V_{TO}) V_{DS} - \frac{1}{2} V_{DS}^2 \right\} + \frac{WC_{ox}\mu_0}{L(1+\frac{V_d}{V_{TC}})(1+\theta(V_{GS_n}-V_T))} \left\{ \frac{4}{3} \phi_F \frac{Q_{BO}}{C_{ox}} \left[ \left( 1 + \frac{V_{DS}}{2 \phi_F } \right)^{3/2} - \left( 1 + \frac{3}{2} \frac{V_{DS}}{2 \phi_F } \right) \right] \right\}$
Saturated	$I_d = \frac{WC_{ox}\mu_0}{L(1+\theta(V_{GS}-V_T))} \left[ \frac{1}{(1+\frac{V_{DSAT}}{V_{TC}}} \left\{ (V_{GS} - V_{TO}) V_{DSAT} - \frac{1}{2} V_{DSAT}^2 + \frac{4}{3} \phi_F \frac{Q_{BO}}{C_{ox}} \left[ \left( 1 + \frac{V_{DSAT}}{2 \phi_F } \right)^{3/2} - \left( 1 + \frac{3}{2} \frac{V_{DSAT}}{2 \phi_F } \right) \right] \right\} \right] + \frac{1}{m} \left[ \frac{1}{2\theta} \left( \sqrt{1 + \frac{4\eta\theta}{\beta}} - 1 \right) \right]^2 \left\{ 1 - \exp \left[ -\frac{\beta m}{\eta} (V_{DS} - V_{DSAT}) \right] \right\}$

Fig. 2. I-V equations for the SCI FET[1].

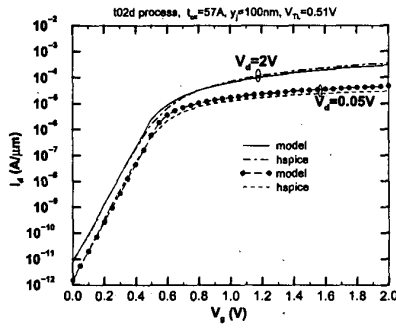


Fig. 3. I-V curves from transregional FET model and HSPICE for TSMC 0.25μm CMOS process

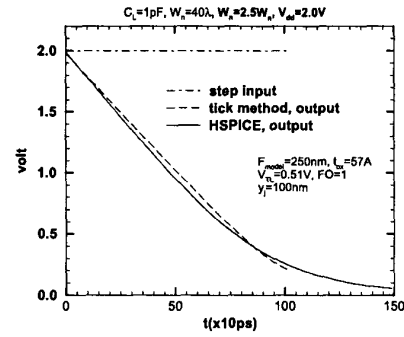


Fig. 4. Transient waveforms at the first stage of inverter chain

where  $k_5 = 13/\kappa$ .

To evaluate  $V_{out_n}$  we use eqn (3).

$$\int_{V_{out_{n-1}}}^{V_{out_n}} \frac{dV_{out}}{\left\{ (V_G - V_{TO}) V_{out} - \frac{1}{2} V_{out}^2 + k_5 \right\}} = \frac{-\kappa}{C_L} \Delta t \quad (8)$$

$$\left[ \frac{\tan^{-1} \left\{ \frac{-V_{out} + k_4}{\sqrt{2k_5 + k_4^2}} \right\}}{-2 \frac{\sqrt{2k_5 + k_4^2}}{\sqrt{2k_5 + k_4^2}}} \right]_{V_{out_{n-1}}}^{V_{out_n}} = \frac{-\kappa}{C_L} \Delta t \quad (9)$$

where  $k_4 = V_G - V_{TO}$ . The above expression gives us an analytical expression for  $V_{out_n}$ . Now consider the saturated region of operation.

$V_{DSAT} = f(V_{G_n})$  and is a known quantity.  $V_{TO}$  is evaluated with  $V_d = V_{d_{n-1}}$ . Thus the I-V equation in this region can be re-written as:

$$I_D = k_2 - k_1 \cdot \exp \left[ -\frac{\beta m}{\eta} (V_{out} - V_{DSAT_n}) \right] \quad (10)$$

Using eqn (3), we have,

$$\left[ \frac{\ln \left( k_2 - k_1 \cdot \exp \left\{ -\frac{\beta m}{\eta} (V_{out} - V_{DSAT_n}) \right\} \right)}{\frac{\beta m}{\eta} k_2} + \frac{(V_{out} - V_{DSAT_n})}{\frac{\beta m}{\eta} k_2} \right]_{V_{out_{n-1}}}^{V_{out_n}} = -\frac{\Delta t}{C_L} \quad (11)$$

The above expression gives us an analytical expression for  $V_{out_n}$ .

### 3. HSPICE VERIFICATION

TSMC 0.25μm process was selected and the SPICE parameters were obtained from MOSIS[10]. To take care of non-uniform substrate doping, one parameter in the TRM was adjusted by around 10% and the resulting I-V match is shown in Fig 3. Waveforms at the first and second stage of an inverter chain are plotted and compared to the HSPICE output. The results of these are shown in Figs 4 and 5. It can be seen that the transient curves of the tick based method

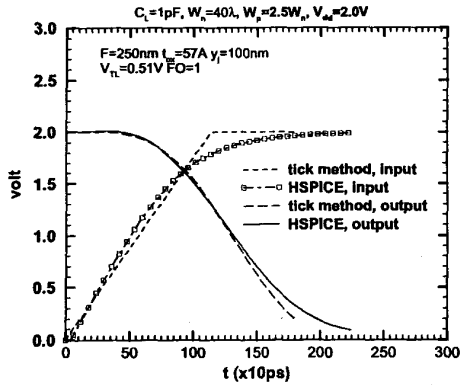


Fig. 5. Transient waveforms at the second stage of inverter chain

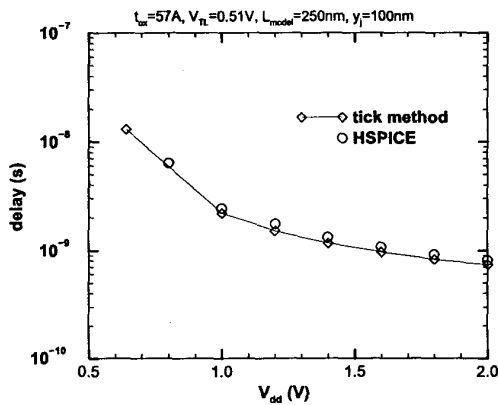


Fig. 6. Delay of second stage of inverter chain: comparison between model and HSPICE

and HSPICE match very closely. Next, delay of the second stage of the inverter chain is plotted, for varying  $V_{dd}$ . This is to make sure that the assumptions made in the tick based method are valid for a wide range of  $V_{dd}$ . The plot is shown in Fig 6. A very close match is seen between the methodology and HSPICE. The tick-based method runs more than 10X faster than a comparable HSPICE simulation. The speed-up is because of the fact that numerical integration is avoided and most calculations are kept analytical.

#### 4. CONCLUSION

The tick-based methodology is an extremely useful method to easily use physically based, transregional models to predict delay and power-frequency performance of future technology. The method is valid over a wide range of supply voltages and for a variety of FETs. Numerical integration is avoided and thus more than 10X speed improvement over HSPICE is obtained.

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