

LOW-POWER CIRCUIT ADVANTAGES OF THE SCALED ACCUMULATION FET

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ABSTRACT

The trend toward higher clock frequencies has resulted in FETs being compared for their performance at the highest frequencies. Traditionally, the buried channel(BC) FET is considered to have more short channel effects than the normal surface channel inversion(SCI) FET and thus the BC FET is used only when absolutely needed. The same, more severe short channel effects behavior has been assumed for moderate to high- V_T FETs, which find use in ultra low-power applications. However, a careful investigation both at the transistor and circuit level, reveals that the BC FET is better than the SCI FET for moderate speed, ultra low-power applications.

1. INTRODUCTION

The trend toward higher clock frequencies is driving FET device engineers to design FETs that can operate at the highest frequencies. Thus performance of the surface channel inversion(SCI) FET and the buried channel(BC) FET have been compared with the highest frequency in mind and the SCI FET has always won over the BC FET [1]. There are many applications that require moderate speed and very low standby power - like implantable medical devices, wearable wrist watch computers and self-powered devices. It has always been assumed that since the SCI FET can outperform the BC FET at the higher frequencies, the same should be true for moderate frequencies. But a careful investigation reveals otherwise.

The BC FET belongs to a more general class of FETs - the accumulation FETs(AFET). The other type of AFET is the surface channel accumulation(SCA) FET. AFETs use a p+ poly for NMOS and have a thin counter-doped(i.e. N-type) layer in the channel region, Fig 1. The doping of the counter-doped layer is an effective way of controlling V_T of the AFET, Fig 2. It can be seen that for V_T below 0.9V, the AFET is a Buried Channel Accumulation(BCA) FET. Since the applications under consideration use low V_{DD} (so that dynamic power($P_{dynamic}$) is kept low), the V_T range of interest is well below 0.9V and thus all AFETs considered in this paper are the BCA type.

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2. FET AND CIRCUIT MODELING

Compact FET analytical models derived in [2] and [3] are used. The models are transregional in nature - i.e. all regions of operation are modeled by maintaining continuity across regional boundaries while including vertical and lateral high field effects. The models are entirely physically based - i.e. they have no fitting parameters and thus can be used for predicting technology over the next decade. Verification of the models with both experimental data and simulations is given in [2],[3]. The models are verified with 2D numerical simulations(using device simulator MEDICI) for the 50nm(L_{eff}) generation, Figs 3 and 4. A very good match between the FET models and numerical simulations is seen.

The models given in [2],[3] were slightly modified to include velocity overshoot, which is taken care of by modifying μ_{eff} (effective mobility including vertical field effect) as[4]:

$$\frac{\mu_{eff}}{1 + \frac{E(x)}{E_c}} \rightarrow \frac{\mu_{eff}}{1 + \frac{E(x)}{E_c}} + \frac{\lambda_{VO}}{L} \quad (1)$$

where λ_{VO} is the velocity overshoot factor. Using experimental data in [5], an analytical expression for λ_{VO} can be obtained as [4]: $\lambda_{VO} = 91 \ln [0.16\mu_{eff} - 14]$.

Circuit modeling is done by using the tick-based methodology [6]. The methodology uses the FET models to estimate power-frequency performance of a chain of inverters. A chain of inverters is considered for comparing the power-frequency performance of the FETs since the worst case delay of a critical path can be simulated by replacing the complex CMOS gates with their worst-case inverters[7]. The tick based method is applicable over a wide range of supply voltages and thus is extremely reliable when different FETs are compared over a wide frequency range.

3. SOURCE FOR BETTER BEHAVIOR

The BCA FET exhibits an increasing long-channel threshold voltage(V_{TL}) with decreasing channel doping, Fig 2 and the SCI FET exhibits an increasing V_{TL} with increasing channel doping. The increased doping in the SCI FET results in a smaller depletion depth(d) and a larger subthresh-

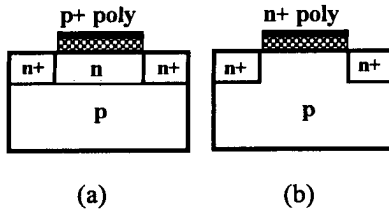


Fig. 1. (a) Accumulation FET and (b) Inversion FET structures

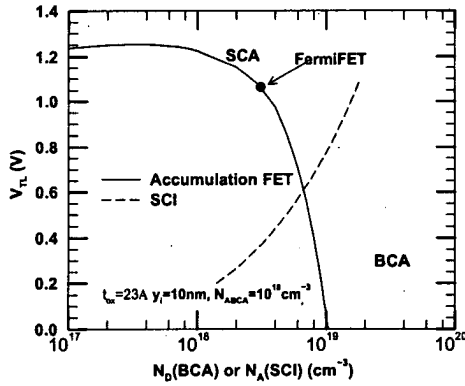


Fig. 2. V_T control of Accumulation and SCI FETs

old slope(S). When S and d are plotted against V_{TL} for the BCA and SCI FETs, Fig 5, it can be seen that at around a V_{TL} of 0.4V, S of the BCA FET becomes better than that of the SCI FET. This is because, while S_{SCI} increases with increasing V_{TL} , S_{BCA} decreases with increasing V_{TL} . Although S_{BCA} is better than S_{SCI} at intermediate and high V_{TL} , the actual performance advantage(i.e. drive current) is dependent on rolloff. Rolloff in SCI is low since the substrate doping(= channel doping) is high and thus minimizes charge sharing. In the BCA FET, rolloff can be minimized by keeping the substrate doping high and by proper halo design. Very low rolloff for $V_T = 0.18V$, $0.1\mu m$ gate length BCA PMOS has been reported in [8]. Thus given an SCI FET and a BCA FET with the same t_{ox} and Source/Drain junction depth(y_j), the BCA FET can outperform the SCI FET at intermediate or relatively high V_{TL} .

As proof of the above argument, $I_{on} - I_{off}$ curves are plotted for the BCA and SCI FETs, Fig 6. The FETs have varying V_{DD} along the x-axis while the threshold voltage is kept the same. There exists a crossover in the BCA and SCI curves, which indicates that there exists a region of operation where the BCA FET is better than the SCI device - this is the low I_{on} region, where $I_{on} < 5\mu A/\mu m$. Thus the BCA FET should perform better than the SCI FET in applications requiring moderate speed and ultra-low power.

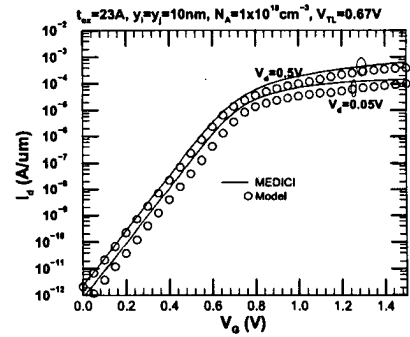


Fig. 3. Transregional BCA FET model vs Numerical Simulation(MEDICI)

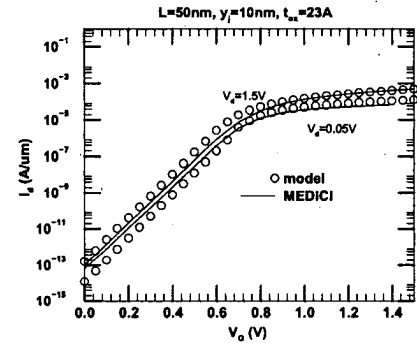


Fig. 4. Transregional SCI FET model vs Numerical Simulation(MEDICI)

4. ADDITIONAL BENEFITS

In addition to a better S, there are a few other significant performance benefits for the BCA FET. Since a higher V_{TL} means a lower channel doping for the BCA FET, one can expect a higher concentration dependent mobility for this FET than for the SCI FET. Also, if the BCA FET operates in the buried-channel regime, the electron mobility is much higher than in the surface-channel regime. This gives an additional increase in drive current.

The BCA FETs have a lower gate and drain capacitance. This is because, when the device operates in the BC regime, $1/C_G = 1/C_{ox} + t_c/\epsilon_{si}$ where t_c is the location of the channel w.r.t the oxide-semiconductor interface. The drain capacitance is less[9] since the p-n junction is only at the bottom(for $y_j = y_i$ (counter-doped layer depth)), rather than both at the bottom and sidewall as in an SCI FET.

In a BCA FET, electron density at the semiconductor-oxide interface is less than that in an inversion channel when the same gate voltage is applied. Thus the barrier for electrons to tunnel in a BCA FET is higher than in a SCI FET. Tunneling models used were similar to those in [10]. When

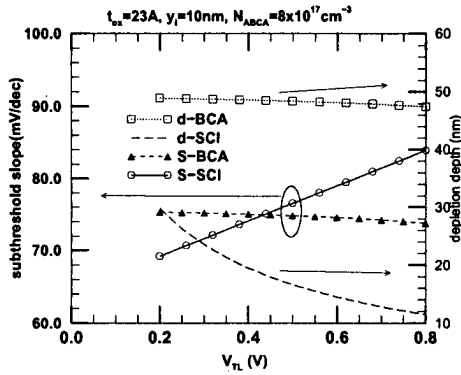


Fig. 5. Long channel subthreshold slope(S) and depletion depth(d) of BCA and SCI FETs

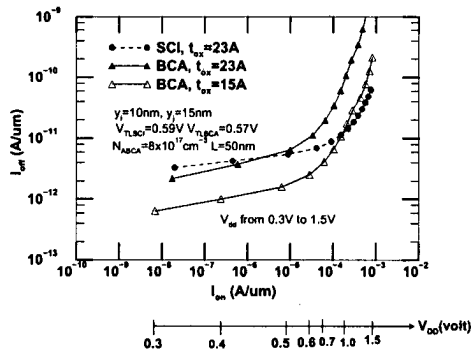


Fig. 6. $I_{ON} - I_{OFF}$ for BCA and SCI FETs

tunneling current density is plotted w.r.t gate voltage for a 15A gate oxide, Fig 7, it can be seen that the BCA FET has J_{TUNNEL} many orders of magnitude less than that of the SCI FET. Thus for ultra-low power applications with a few pW of standby power, the SCI FET would have to use a 23A [11] thick oxide whereas the BCA FET could use a 15A oxide - this means a higher drive current for the BCA FET.

In an SCI FET, at higher V_{TL} the channel doping is higher. This would cause band to band tunneling (BTBT) at the drain-channel region (assuming the halo region is well-designed to avoid any BTBT). Measured NMOS BTBT leakage [12] indicates that the SCI FET is not suitable for ultra-low power operation, since a substrate doping that gives a BTBT comparable to subthreshold leakage current, results in a few hundred pW/um standby current. In a BCA FET, the channel is counter-doped and no BTBT can occur here.

5. DESIGN PLANE

To visualize the performance benefits of the BCA FET, one needs a design plane wherein it can be identified clearly which of the two FETs-BCA or SCI, is better. A suitable design space is the $V_{DD} - V_{TL}$ plane. The boundaries of

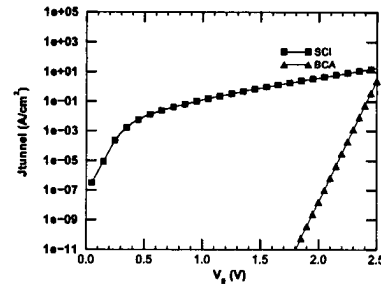


Fig. 7. Tunneling comparison between AFET and SCI FET for $t_{ox} = 15A$

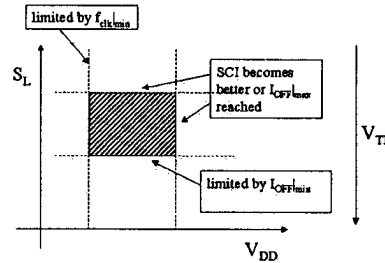


Fig. 8. Design Plane for the Accumulation FET

the design space where the BCA FET is better than the SCI FET can be determined as shown in Fig 8. The criterion for better FET performance can be one of: (A) a better I_{ON} for the same I_{OFF} , or (B) a better $P_{dynamic}$ for the same P_{static} and f_{clk} .

Fig 9 shows the design space generated using conditions A and B. The grid resolution is 0.02V along both the x and y axes. It can be seen that the BCA FET performs better than the SCI FET in a very small region when condition (A) is used. However since the capacitances of the BCA FET are better than that of the SCI FET, this region expands when condition (B) is used (since $P_{dynamic} \propto C_L$ and $f_{clk} \propto 1/C_L$). The design space using condition (B) is the superset of that using condition A.

To get an idea about the frequencies and power levels where each of the two FETs- BCA and SCI is better, a chain of inverters using either the BCA or SCI FET was simulated using the tick based methodology [6]. Two cases were considered - a high V_{TL} case and a low V_{TL} case, Fig 10. In both cases P_{static} is kept constant for varying f_{clk} by slightly increasing V_{TL} as V_{DD} is increased. The high V_{TL} case shows that the BCA FET chain operates better than the SCI FET chain over a wide range of f_{clk} . Because of the high V_{TL} , the maximum clock frequency is limited to around 1GHz. The low V_{TL} case shows that the BCA FET chain performs worse than the SCI FET chain for frequencies well above 1GHz.

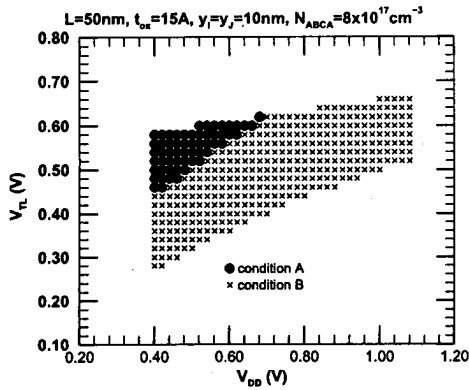


Fig. 9. Design plane generated using condition A and B

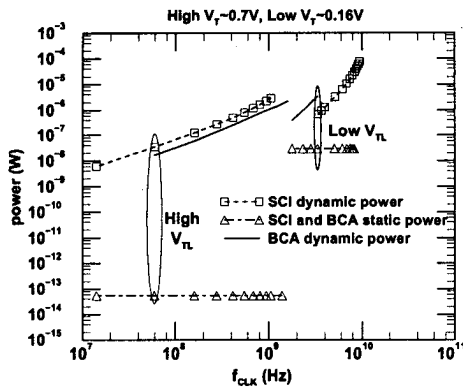


Fig. 10. P – f_{CLK} performance comparison of BCA and SCI FETs

6. CONCLUSION

BCA and SCI FETs have been compared both at the FET and circuit level. Due to a lower subthreshold slope at moderate to high V_T , the BCA FET is better than the SCI FET in this range of V_T . In addition the BCA FET has very low oxide tunneling, no BTBT and lower gate and drain capacitances when compared to the SCI FET. At $L_{eff} = 50\text{nm}$, a BCA FET inverter chain has a lower dynamic power than a SCI FET chain up to a frequency of 1GHz, with a few tenths of a pW standby power. Thus, the BCA FET is better than the SCI FET for moderate speed, ultra-low power applications.

7. REFERENCES

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