SCALED ACCUMULATION FETS FOR ULTRA-LOW POWER LOGIC

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ABSTRACT

Ultra-low power systems require very low standby power and operate at moderate speeds. Traditionally, the normal surface channel inversion(SCI) FET would be considered better for such applications when compared to the buried channel(BC) FET, since the BC FET has always shown more short channel effects in past research. But, past comparisons between the two FETs have been done with the highest frequency in mind and the same conclusion need not hold true for moderate speed, ultra-low power applications. Due to a better subthreshold slope and negligible band to band tunneling leakage at the drain-halo and drain-channel region, the BC FET is better suited for such applications.

I. INTRODUCTION

The emphasis on high frequency operation of digital logic has resulted in FETs being compared at their highest frequencies, for a given technology. The surface channel inversion(SCI) FET has always won over the buried channel(BC) FET in past comparisons[1] and the same behavior has been assumed for low power operation. This assumption holds good most of the time, as long as the same FETs are used for low power applications as for high performance applications. Such was the case in most of the older technologies, where the leakage current was a few pA/um. But present day high performance technology has a subthreshold leakage current of a few nA/um, which would be too high for ultra-low power applications. Such applications include implantable medical devices, wearable wrist watch computers, self-powered devices, etc., and require a very low standby power but only a moderate speed. This necessitates the need for moderate to high V_T FETs(to keep P_{static} low). ITRS 2001 [2] projects the leakage current of low standby power(LSTP) systems to be 1pA/um(50nm L_{eff} generation) and the V_T to be 0.52V.

The BC FET belongs to a more general class of FETs - the accumulation FETs, which use a p+ poly for NMOS and have a thin counter doped(i.e. N-type) layer in the channel region, Fig. 1. Conduction occurs in this region and thus the term "accumulation", as opposed to "inversion". The expression "BCA"(buried channel accumulation) FET is more appropriate than "BC" FET and will be used in the rest of

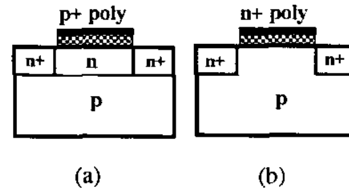

Fig. 1. (a)Accumulation NFET and (b)Inversion NFET structures

this paper. Threshold voltage control for BCA FETs is done by varying the implant doping, Fig. 2, while that of the SCI FET by varying the channel doping.

II. FET AND CIRCUIT MODELING

Compact FET analytical models derived in [3] and [4] are used. The models are transregional in nature - i.e. all regions of operation are modeled by maintaining continuity across regional boundaries while including vertical and lateral high field effects. The models are entirely physically based - i.e. they have no fitting parameters and thus can be used for predicting technology over the next decade. Verification of the models with both experimental data and simulations is given in [3],[4]. The models are verified with 2D numerical simulations(using device simulator MEDICI[5]) for the 50nm(L_{eff}) generation, Figs. 3 and 4. A very good match between the FET models and numerical simulations is achieved.

The models given in [3],[4] were slightly modified to include velocity overshoot, which is taken care of by modifying μ_{eff}(effective mobility including degradation due to vertical field) as[6]:

$$\frac{\mu_{eff}}{1+\frac{E(x)}{E_c}} \rightarrow \frac{\mu_{eff}}{1+\frac{E(x)}{E_c}} + \frac{\lambda_{VO}}{L} \qquad (1)$$

where λ_{VO} is the velocity overshoot factor. Using experimental data in [7], an analytical expression for λ_{VO} can be obtained as [6]: $\lambda_{VO} = 91\ln[0.16\mu_{eff} - 14] \times 10^{-6}$.

Band to band tunneling(BTBT) current at the drain junction becomes important at high channel and halo doping.

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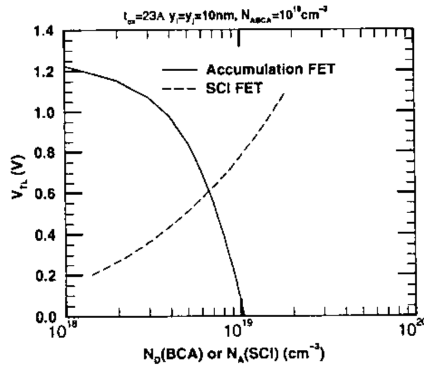

Fig. 2. V_T control of accumulation and inversion NFETs

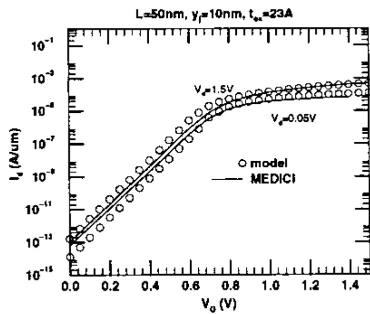

Fig. 3. Transregional SCI FET model vs numerical simulation(MEDICI)

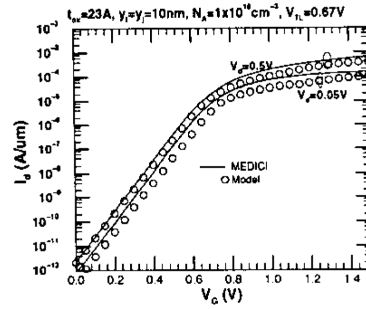

Fig. 4. Transregional BCA FET model vs numerical simulation(MEDICI)

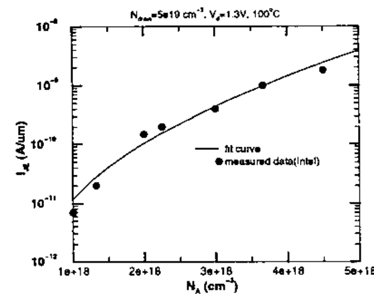

Fig. 5. BTBT leakage model vs measured data from [8]

Assuming a triangular barrier, the tunneling current density can be found as[9]:

$$J = \frac{\sqrt{2m^*}q^3EV}{4\pi^2\hbar^2E_g^{1/2}}\exp\left(-\frac{4\sqrt{2m^*}E_g^{1/2}}{3qE\hbar}\right) \quad (2)$$

E depends on the drain and substrate(i.e. channel and halo) doping in the SCI FET. This model is fit to measured data in [8] and shown in Fig. 5, where we see a good match between the model and measurements. The model also matches well with the data in [10].

Circuit modeling is done by using a tick-based methodology [11]. The methodology uses the FET models to estimate power-frequency performance of a chain of inverters. A chain of inverters is considered for comparing the power-frequency performance of the FETs since the worst case delay of a critical path can be simulated by replacing the complex CMOS gates with their worst-case inverters[12]. The tick based method is applicable over a wide range of supply voltages and thus is extremely reliable when different FETs are compared over a wide frequency range.

III. SOURCE FOR BETTER BEHAVIOR

The SCI FET exhibits increasing channel doping with increasing long-channel threshold voltage(V_{TL})(i.e. decreasing I_{OFF}), Fig. 2. The increased doping in the SCI FET results in a smaller depletion depth(d) and thus a larger subthreshold slope(S)($\propto \frac{1}{d}$). Thus S_{SCI} increases with decreasing I_{OFF}, Fig. 6 (for the case without BTBT leakage). For the BCA FET, V_{TL} increases as channel doping is reduced, Fig. 2; the reduced channel doping makes the conducting channel come closer to the oxide-semiconductor interface. So S_{BCA} reduces with decreasing I_{OFF}.

Comparing S-I_{OFF} curves of BCA and SCI FETs(without BTBT leakage), Fig. 6, it can be seen that at around an I_{OFF} of 0.1pA/um, S of the BCA FET becomes better than that of the SCI FET. Although S_{BCA} is better than S_{SCI} at intermediate and high V_{TL}, the actual performance advantage(i.e. drive current) is dependent on rolloff. Rolloff in SCI is low since the substrate doping(= channel doping) is high and thus minimizes charge sharing. In the BCA FET, rolloff can be minimized by keeping the substrate doping high and by proper halo design. Very low rolloff for $V_T = 0.18$V, 0.1μm gate length BCA PMOS has been reported in [13].

As proof of the above argument, I_{ON} vs I_{OFF} curves are plotted for the BCA and SCI FETs, Fig. 7. V_{DD} varies along

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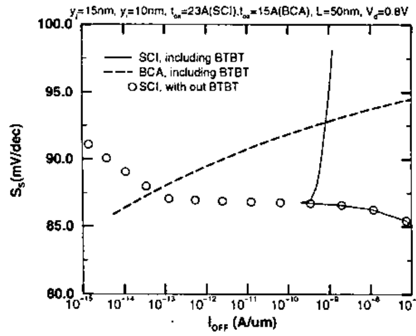

Fig. 6. Short channel subthreshold slope(S_S) vs I_{OFF} for BCA and SCI FETs

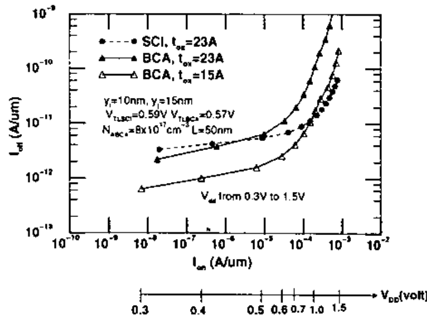

Fig. 7. $I_{ON} - I_{OFF}$ for BCA and SCI FETs

the x-axis while the threshold voltage is kept constant. There exists a crossover in the BCA and SCI curves, which indicates that there exists a region of operation where the BCA FET is better than the SCI device - this is the low I_{ON} region, where $I_{ON} < 10\mu A/\mu m$ and I_{OFF} is a few pA/um. Thus the BCA FET should perform better than the SCI FET in applications requiring moderate speed and ultra-low power.

Since the SCI FET design necessitates increased channel doping for reduced I_{OFF}, BTBT leakage at the drain-channel and drain-halo region becomes important. In the BCA FET, only the channel(i.e. implant) doping is varied to control I_{OFF}; the substrate/halo profiles are designed so as to avoid any BTBT leakage. Thus the BCA FET shows negligible BTBT leakage. When BTBT leakage is included in the I_{OFF} calculation for the SCI FET, we get an L-shaped curve, Fig. 6. This is because of the fact that at low V_{TL}, leakage is dominated by subthreshold current, whereas at high values of V_{TL}, BTBT leakage is the dominant leakage mechanism. Because of the combined effect of subthreshold leakage and BTBT leakage, the SCI FET exhibits a minimum I_{OFF} of around 100pA/um, which is too high for ultra low power applications. Thus, because of a superior subthreshold slope and negligible BTBT leakage, the BCA FET is better suited for ultra-low power, moderate speed applications.

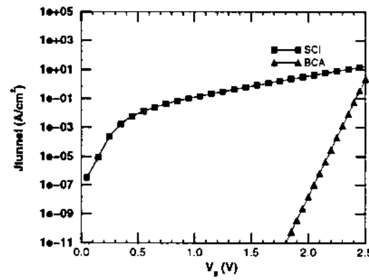

Fig. 8. Tunneling comparison between AFET and SCI FET for $t_{ox} = 15A$

IV. ADDITIONAL BENEFITS

In addition to a better S, there are a few other significant performance benefits for the BCA FET. Since a higher V_{TL} means a lower channel doping for the BCA FET, one can expect increasing concentration dependent mobility for this FET with increasing V_T. This gives an additional increase in drive current.

The BCA FETs have a lower gate and drain capacitance, for the same drain current(compared to the SCI FET). This is because, when the device operates in the BC regime, $1/C_G = 1/C_{ox} + t_c/\epsilon_{Si}$ where t_c is the location of the channel w.r.t the oxide-semiconductor interface. The drain capacitance is less[14] since the p-n junction is only at the bottom(for $y_j = y_i$(counter doped layer depth)), rather than both at the bottom and sidewall as in an SCI FET.

In a BCA FET, electron density at the semiconductor-oxide interface is less than that in an inversion channel when the same gate voltage is applied. E_B, the barrier for electrons to tunnel through the oxide, is higher in a BCA FET than in a SCI FET. Tunneling models used were similar to those in [15]. When tunneling current density is plotted w.r.t gate voltage for a 15A gate oxide, Fig. 8, it can be seen that the BCA FET has J_{TUNNEL} many orders of magnitude less than that of the SCI FET. Thus for ultra-low power applications with a few pW of standby power, the SCI FET would have to use a 23A[16] thick oxide whereas the BCA FET could use a 15A oxide - this means a higher drive current for the BCA FET. The advantage of using a 15A oxide for the BCA FET is shown in Fig. 7.

V. DESIGN PLANE

To visualize the performance benefits of the BCA FET, one needs a design plane wherein it can be identified clearly which of the two FETs-BCA or SCI, is better. A suitable design space is the $V_{DD} - V_{TL}$ plane. The boundaries of the design space where the BCA FET is better than the SCI

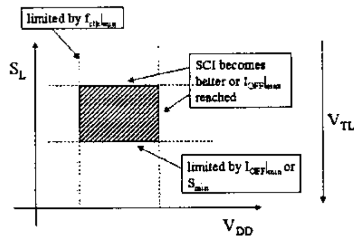

Fig. 9. Design plane for the accumulation FET

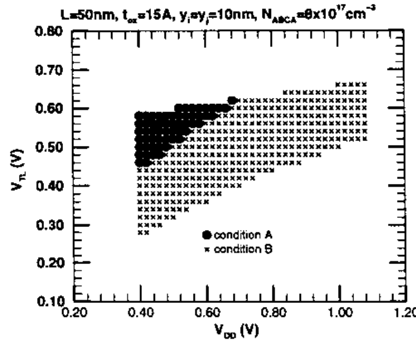

Fig. 10. Design plane generated using conditions A and B

FET can be determined as shown in Fig. 9. The criterion for better FET performance can be one of: (A)a better I_{ON} for the same I_{OFF}, or (B)a better $P_{dynamic}$ for the same P_{static} and f_{clk}.

Fig. 10 shows the design space generated using conditions A and B. BTBT leakage is not included in this simulation. The grid resolution is 0.02V along both the x and y axes. It can be seen that the BCA FET performs better than the SCI FET in a very small region when condition A is used. However since the capacitances of the BCA FET are better than that of the SCI FET, this region expands when condition B is used(since $P_{dynamic} \propto C_L$ and $f_{clk} \propto 1/C_L$). The design space using condition B is the superset of that using condition A.

VI. POWER-FREQUENCY PERFORMANCE

To get an idea about the frequencies and power levels where each of the two FETs- BCA and SCI is better, a chain of inverters using either the BCA or SCI FET was simulated using the tick based methodology[11]. Two cases were considered - a high V_{TL} case and a low V_{TL} case; $P - f_{clk}$ curves are plotted in Fig. 11. Power values plotted are per-gate values.

In the high V_{TL} case, halo-doped FETs were considered. The SCI FET doping profile was similar to that of the well-tempered MOSFET proposed in [10]. Comparing

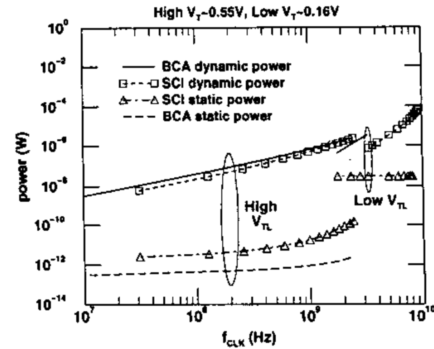

Fig. 11. $P - f_{CLK}$ performance comparison of BCA and SCI FETs

the $P - f_{clk}$ curves for this case. We see that for almost the same dynamic power, the SCI FET chain has a static power an order of magnitude greater than that of the BCA FET chain. At lower clock frequencies(i.e. lower V_{dd}), this difference decreases - this is because while at high f_{clk} BTBT leakage is the dominant leakage mechanism in the SCI FET, at lower f_{clk}, subthreshold leakage is the dominant leakage mechanism. We see that at frequencies above 500MHz, the standby power of the SCI FET inverter chain is tens of PW - the SCI FET is unable to achieve ITRS recommended standby power(for LSTP systems) at these frequencies and this is because of BTBT leakage.

In the low V_{TL} case, uniformly doped SCI and BCA FETs are considered. P_{static} is kept the same for varying f_{clk} by slightly increasing V_{TL} as V_{DD} is increased. The low V_{TL} case shows that the BCA FET chain performs worse than the SCI FET chain for frequencies well above 1GHz.

VII. CONCLUSION

BCA and SCI FETs have been compared both at the FET and circuit level. Due to a lower subthreshold slope at moderate to high V_T, the BCA FET is better than the SCI FET in this range of V_T. In addition the BCA FET has very low oxide tunneling, no BTBT leakage and lower gate and drain capacitances when compared to the SCI FET. At $L_{EFF} = 50$nm and pW standby power, a BCA FET inverter chain performs better than a SCI FET chain - the BCA FET chain has a static power 10-100 times lower than that of the SCI FET chain, for almost the same dynamic power. Thus, the BCA FET is better than the SCI FET for moderate speed, ultra-low power applications.

VIII. ACKNOWLEDGMENTS

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