Hierarchical Matrix of Limits

	Theoretical	Practical
5. System		
4. Circuit		
3. Device		
2. Material		
1. Fundamental		

Fig. 1. Hierarchical matrix of limits on GSI.

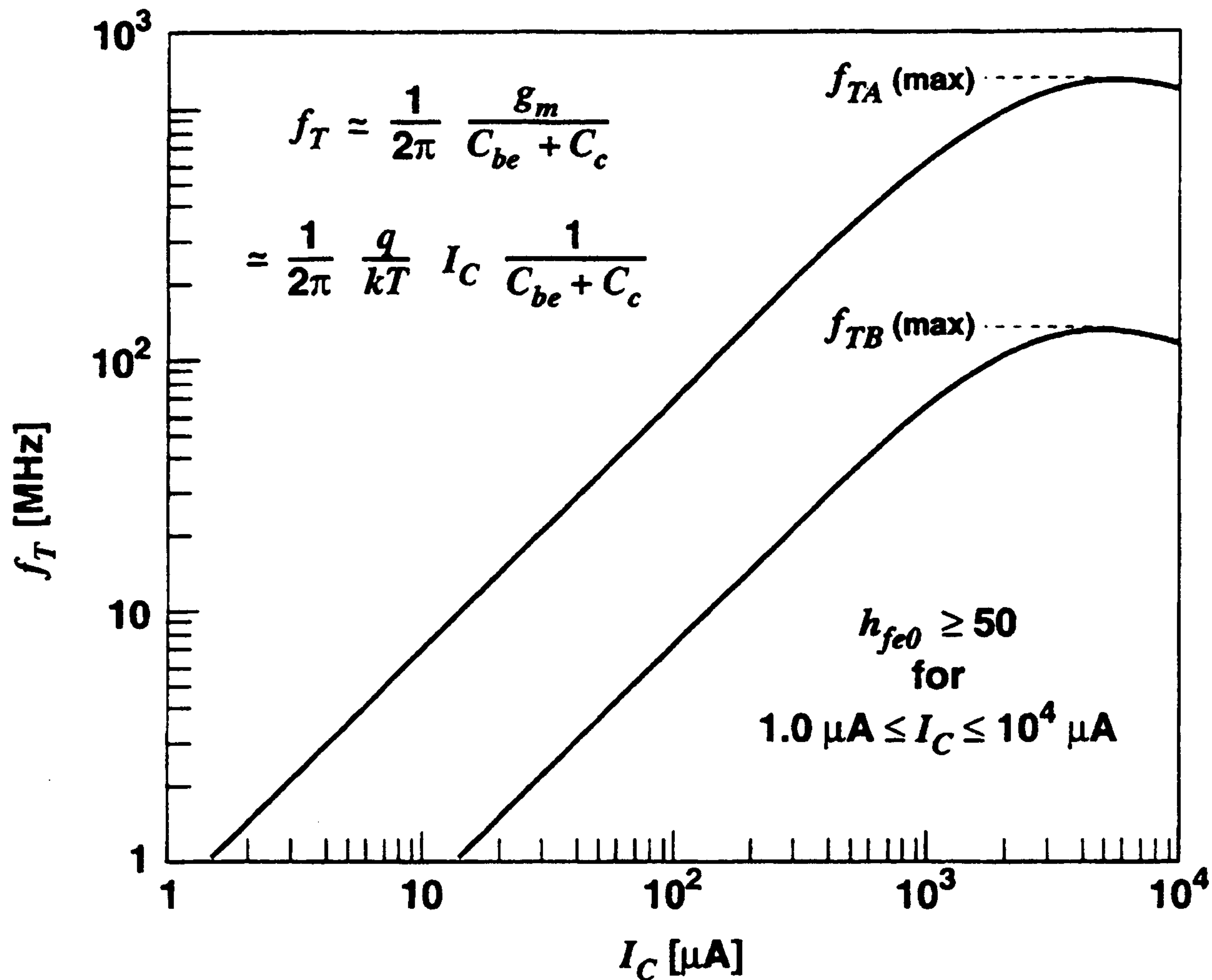


Fig. 2. Transistor gain-bandwidth product versus quiescent collector current. $V_{CE} = 3.0$ V for transistors A and B [7].

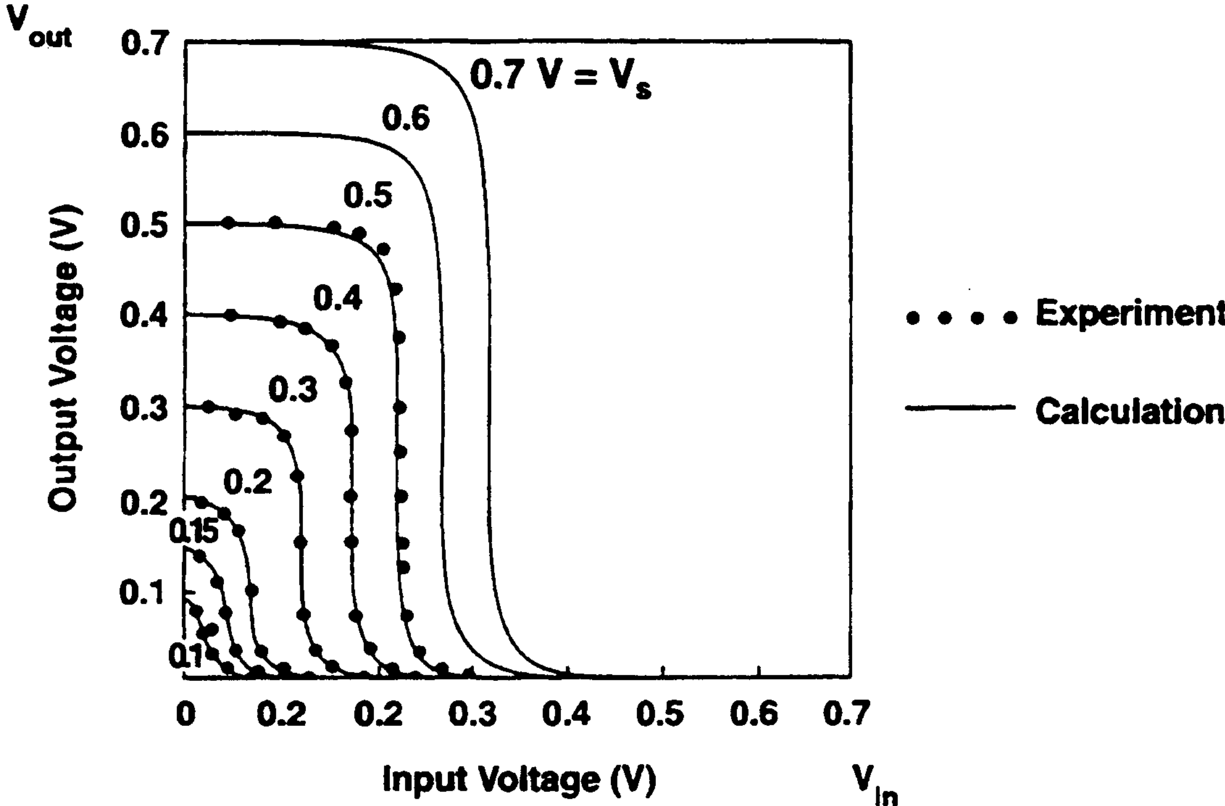


Fig. 3. Static CMOS inverter transfer characteristic [14].

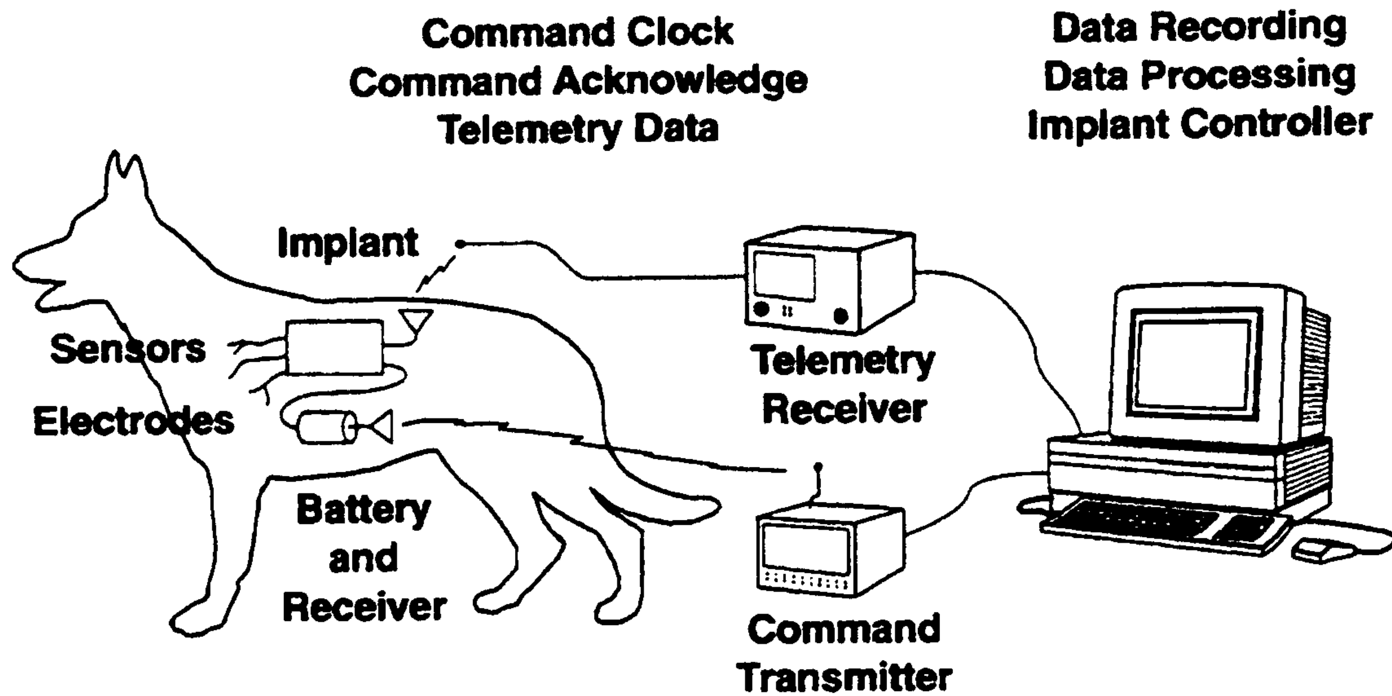
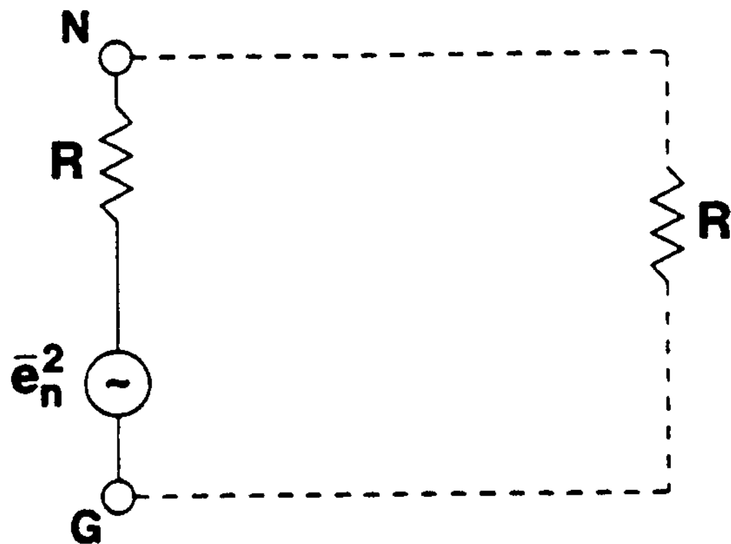


Fig. 4. Implantable telemetry system [16].

A Fundamental Limit from Thermodynamics



$$\bar{e}_n^2 = 4kTRB$$

$$P_{AVAIL} = \bar{e}_n^2/4R$$

$$P_{AVAIL} = kTB$$

Fig. 5. Model for derivation of fundamental limit from thermodynamics.

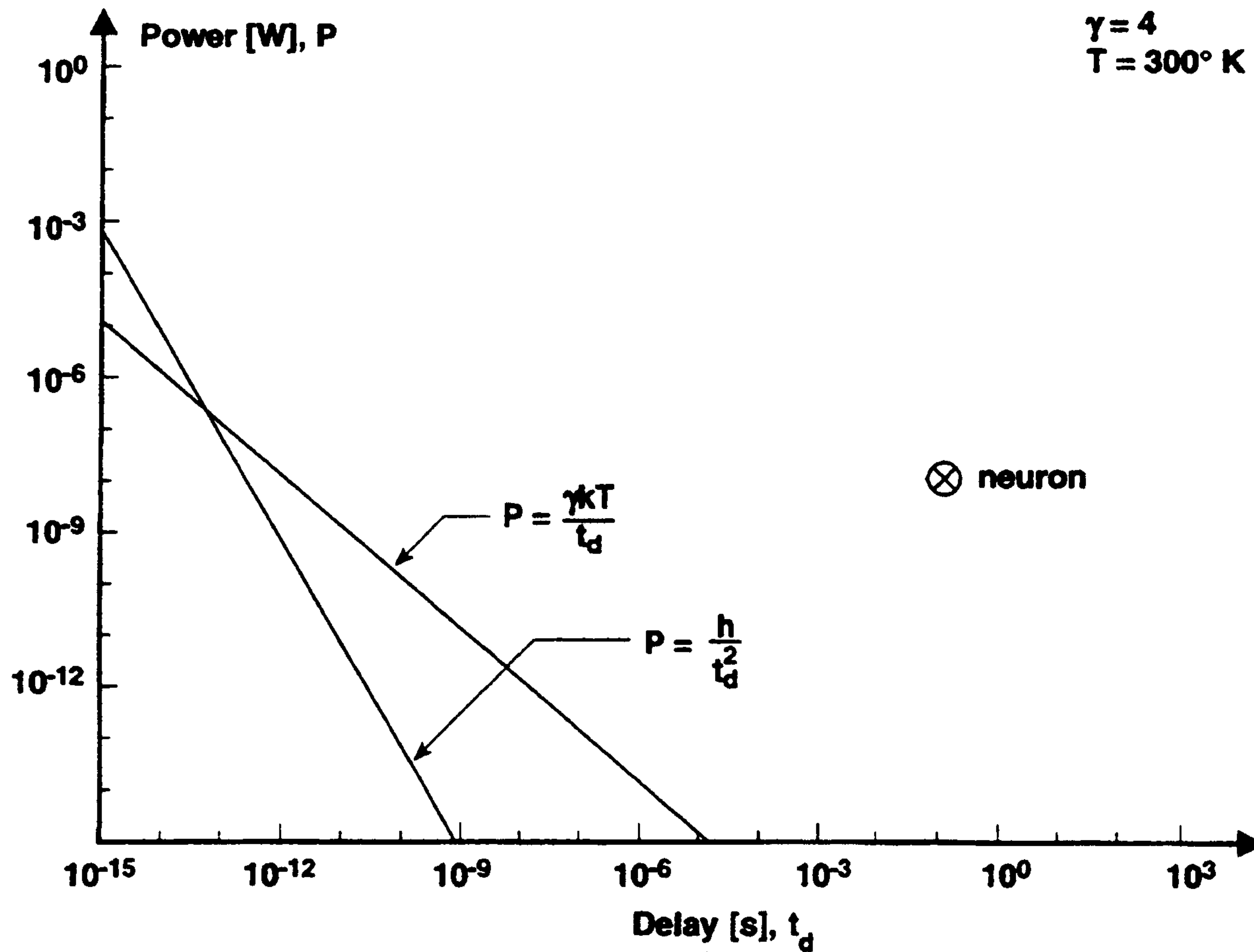


Fig. 6. Average power transfer P during a switching transition versus transition interval t_d for fundamental limits derived from thermodynamics and quantum mechanics.

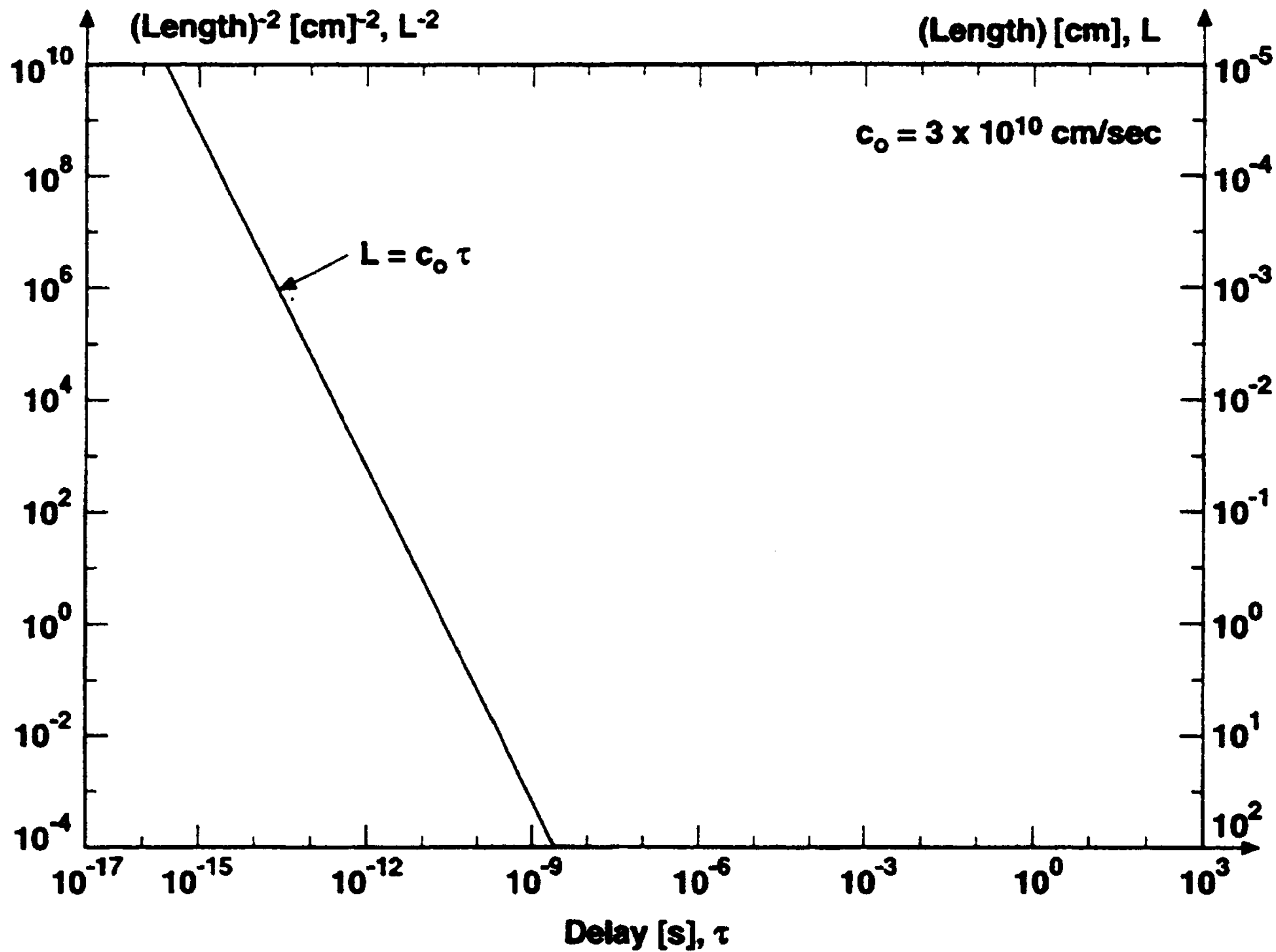


Fig. 7. Square of reciprocal length $(1/L)^2$ of an interconnect versus interconnect circuit response time τ for the fundamental limit from electromagnetics.

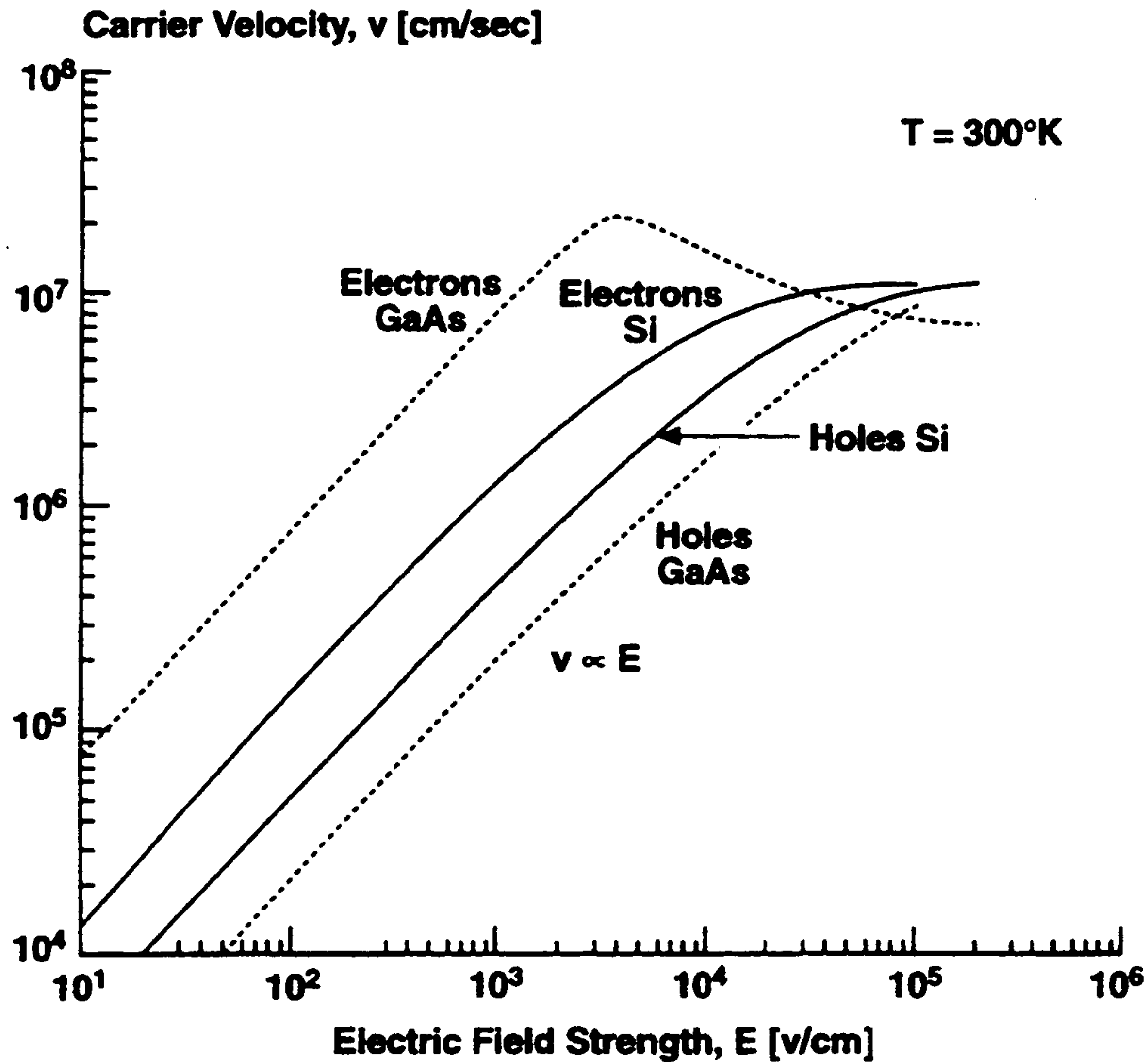


Fig. 8. Carrier velocity versus electric field strength $\mathcal{E}$ for electrons and holes in Si and GaAs.

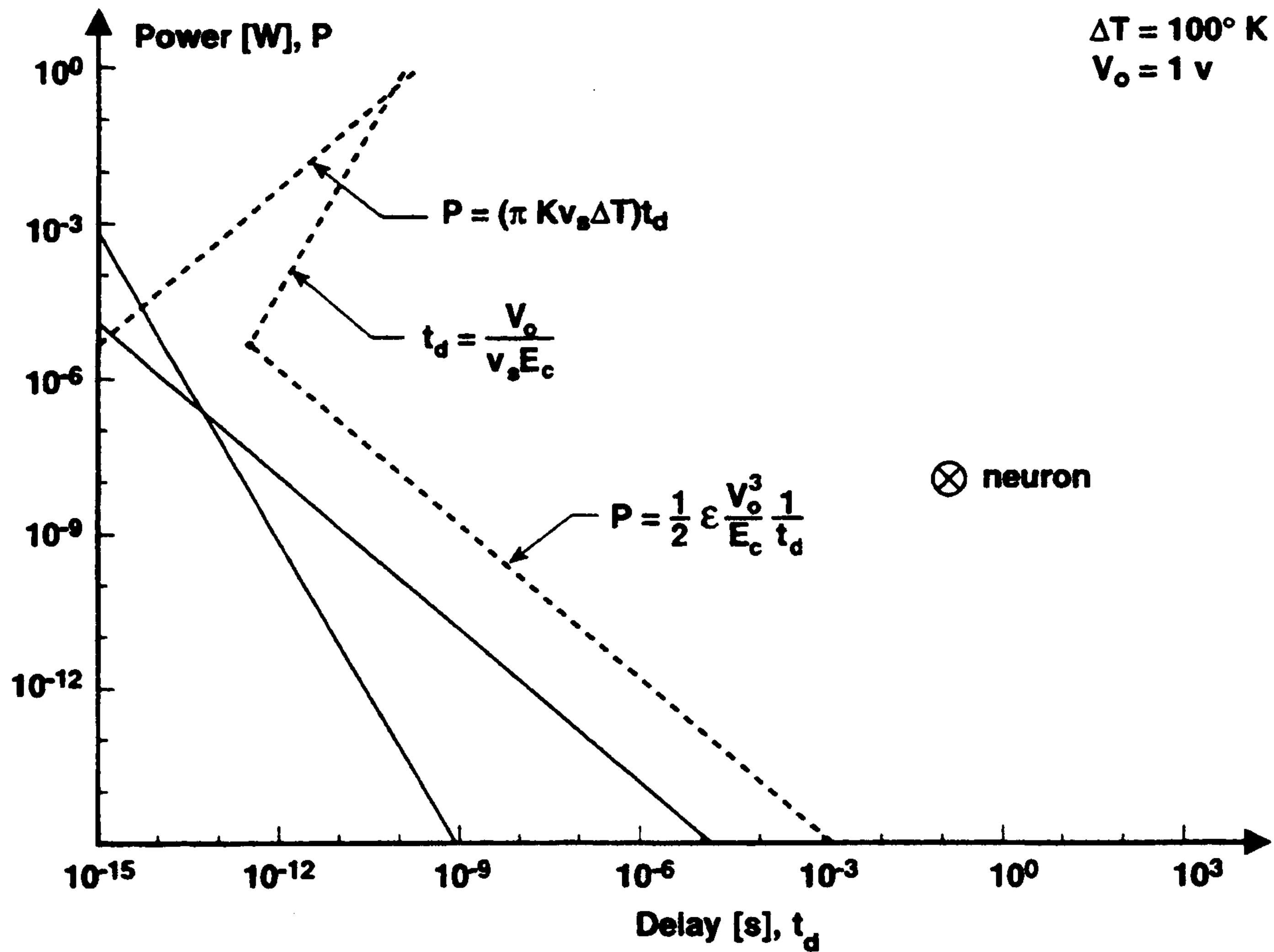
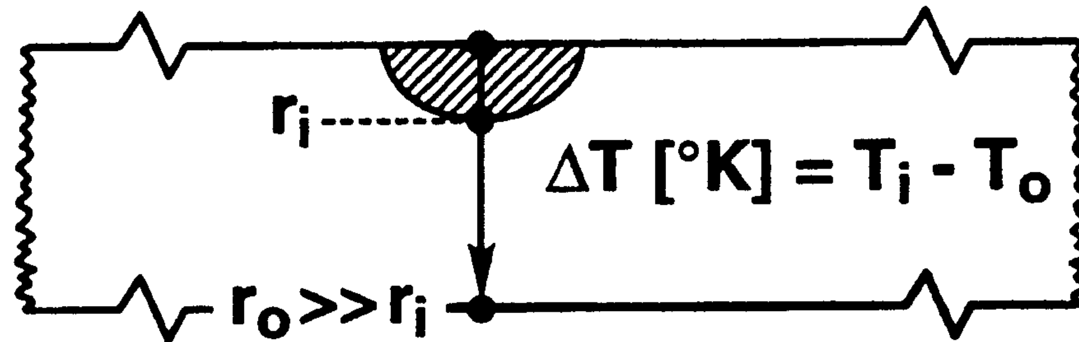


Fig. 9. P versus t_d for fundamental limits and Si material limits based on energy storage, transit time, and heat removal.



$$\frac{t_s}{P_s} = \frac{1}{\pi K v_s \Delta T}$$

Fig. 10. Model for derivation of material limit based on heat conduction.

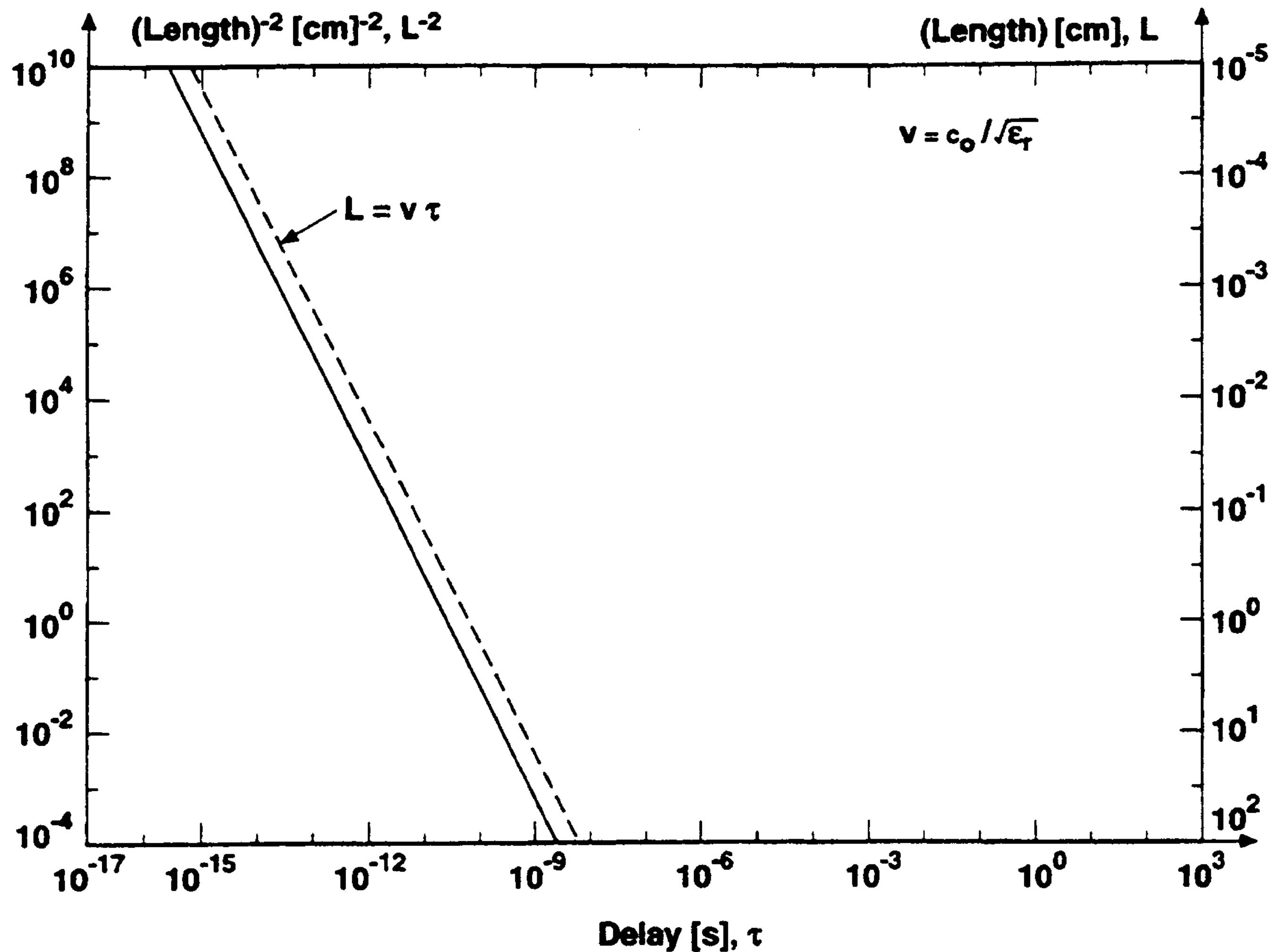
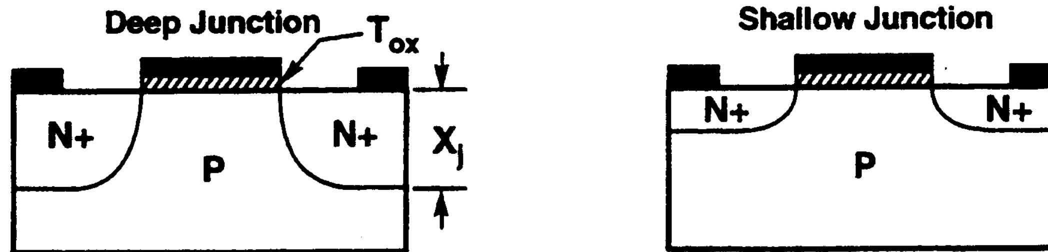
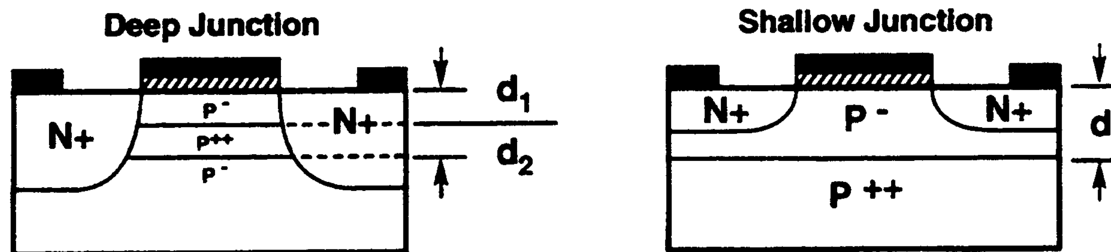


Fig. 11. $(1/L)^2$ versus τ for fundamental limit and material limit with polymer dielectric replacing free space. Both limits are based on the velocity of electromagnetic waves.

Uniformly Doped Bulk MOSFET



Low Impurity Channel Bulk MOSFET



SOI MOSFET

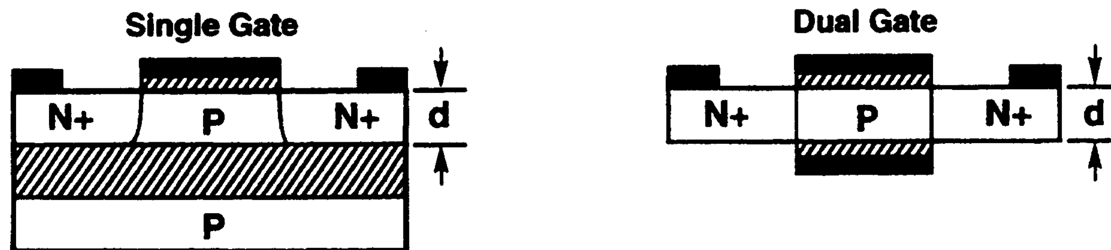


Fig. 12. MOSFET structures.

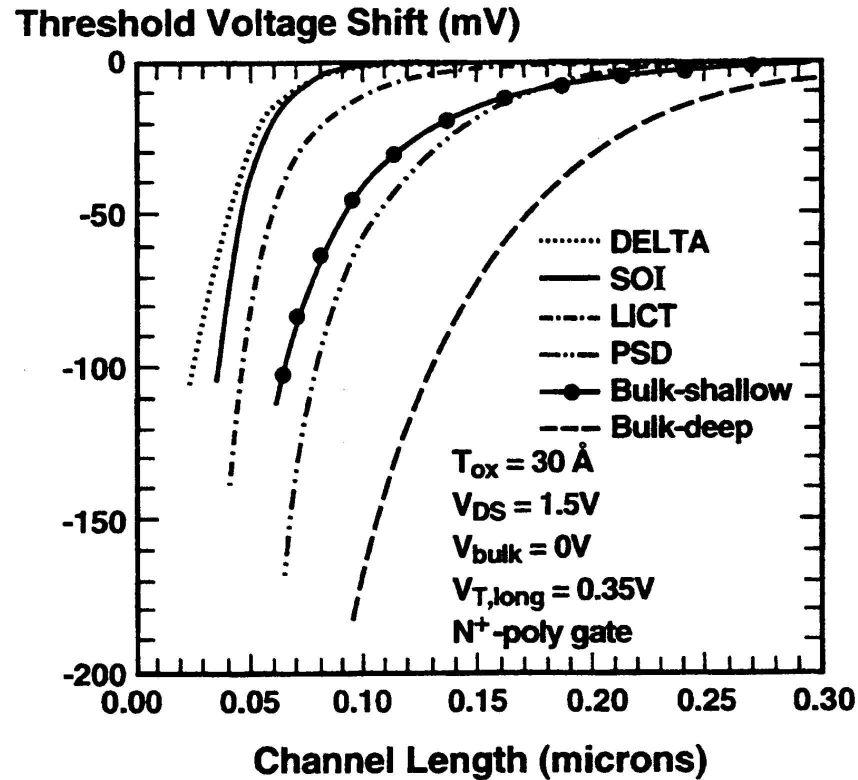


Fig. 13. Short channel threshold voltage versus channel length for the Si devices shown in Fig. 12. Device parameters at 300 K are: 1) Deep-junction bulk MOSFET: $N_A = 8.6 \times 10^{17}$cm^3, Junction depth = 1000 Å [29]. 2) Shallow-junction bulk MOSFET: $N_A = 8.6 \times 10^{17}$cm^3 Junction depth = 50 Å. 3) PSD or low impurity channel deep junction MOSFET: $N_A = 10^{16}$cm^3, $N_A^{++} = 5\times 10^{18}$ cm^3, $N_A^{+} = 5 \times 10^{17}$ cm^3, d = 218 Å, Junction depth = 500Å [29]. 4) LICT or low impurity channel shallow junction MOSFET: $N_A = 5 \times 10^{16}$ cm^{-3}, $N_A = 5 \times 10^{18}$ cm^3, d = 318 Å, Junction depth = 50 Å. 5) SOI single gate MOSFET: $N_A = 5 \times 10^{18}$ cm^{-3}, d = 55 Å. 6) Delta or SOI dual gate MOSFET: $N_A = 5 \times 10^{18}$ cm^{-3} d = 109 Å.

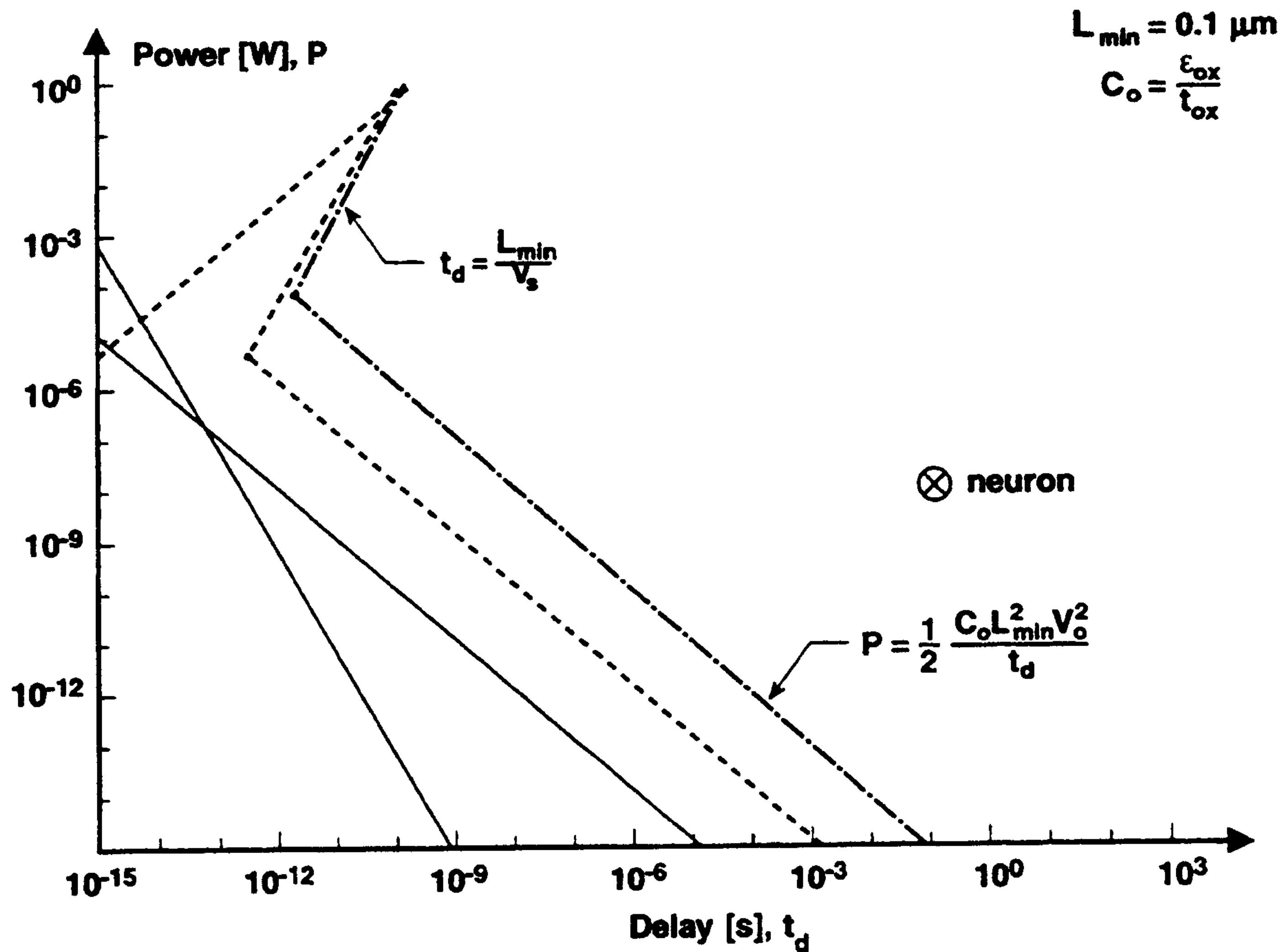


Fig. 14. *P* versus t_d for fundamental limits, Si material limits and MOSFET device limits derived from gate energy storage and channel transit time.

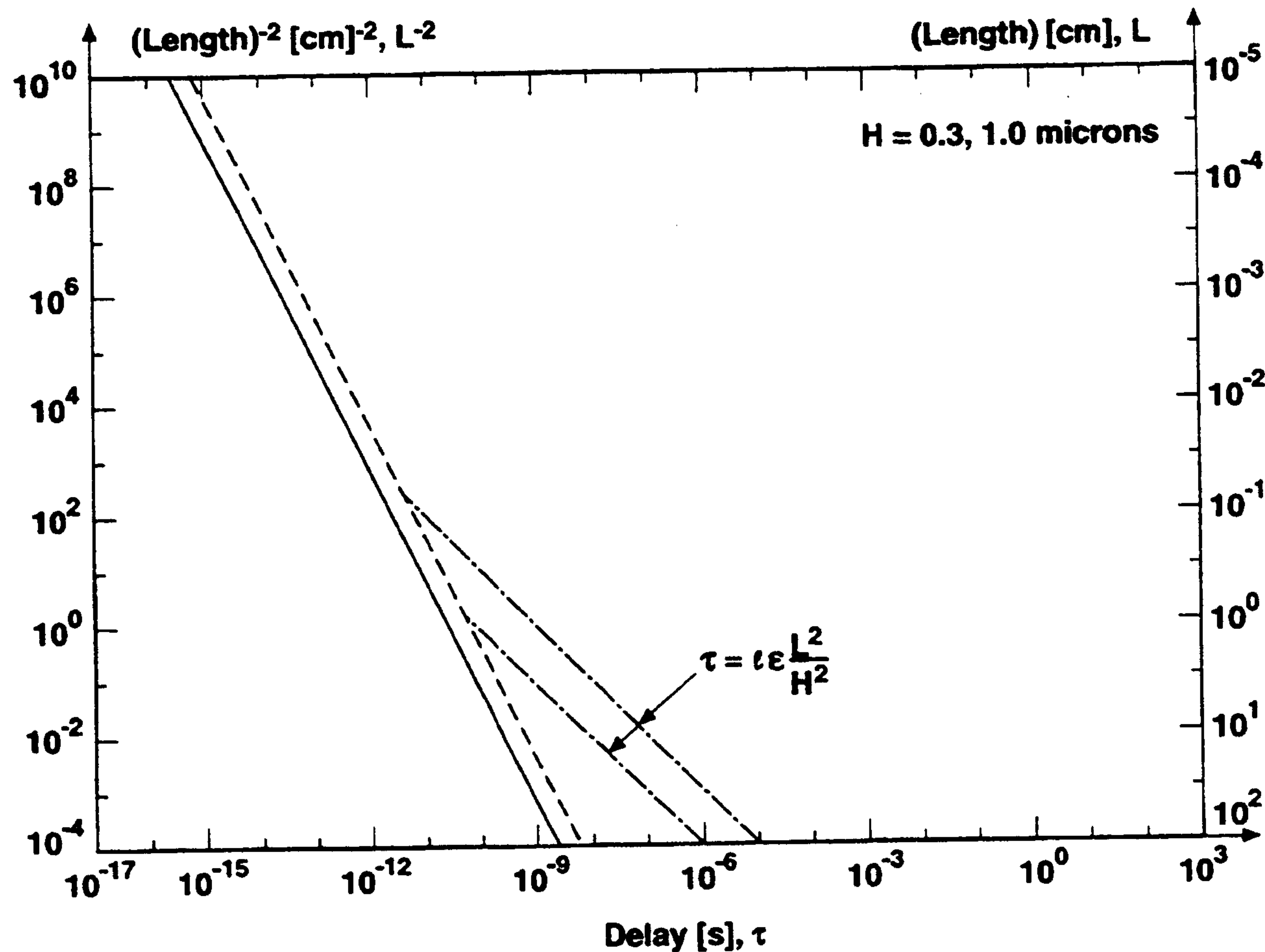


Fig. 15. $(1/L)^2$ versus τ for fundamental limit, material limit and device limits on interconnects for a polymer-copper technology. Device limits represent the response time of a distributed resistance-capacitance network.

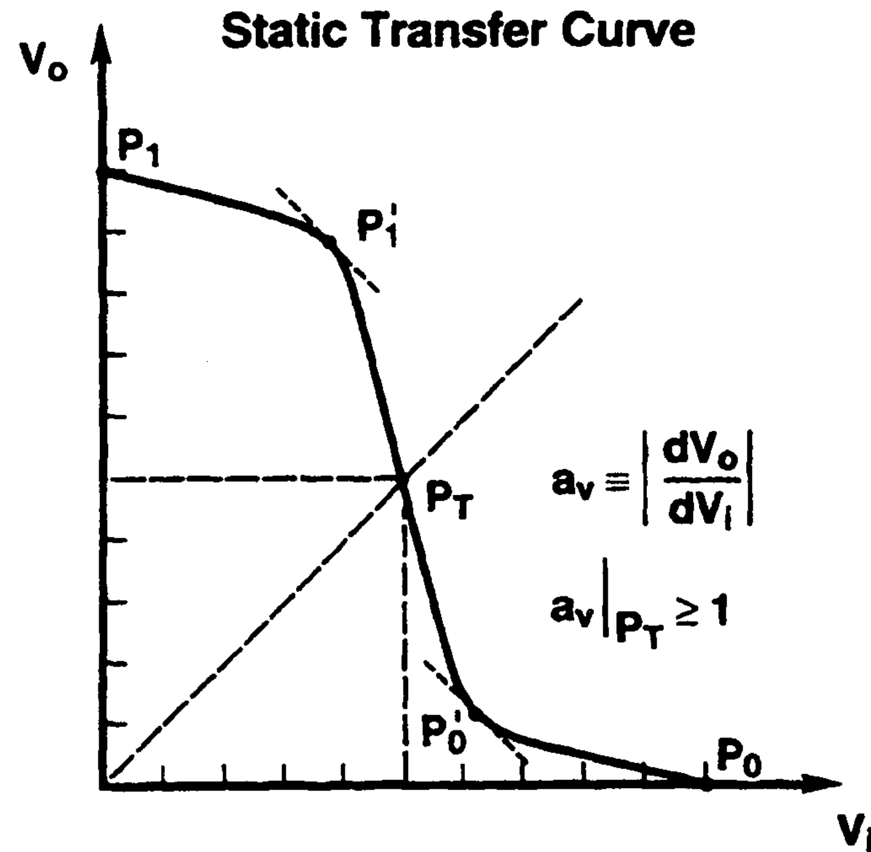


Fig. 16. Static transfer characteristic of a nonideal CMOS inverter.

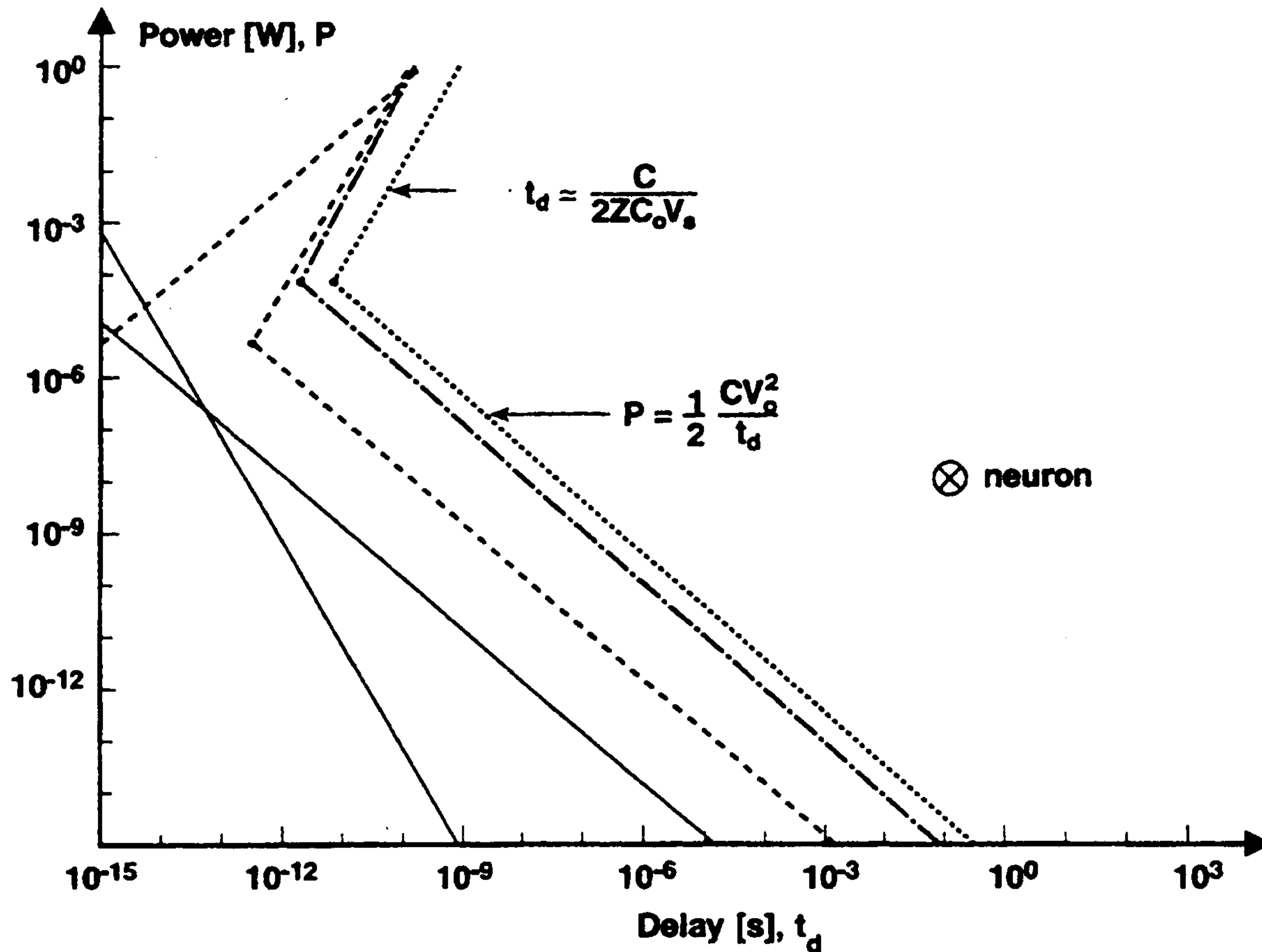


Fig. 17. P versus t_d for fundamental, Si material, MOSFET and CMOS circuit limits. Circuit limits are derived from switching energy and intrinsic gate delay analyses.

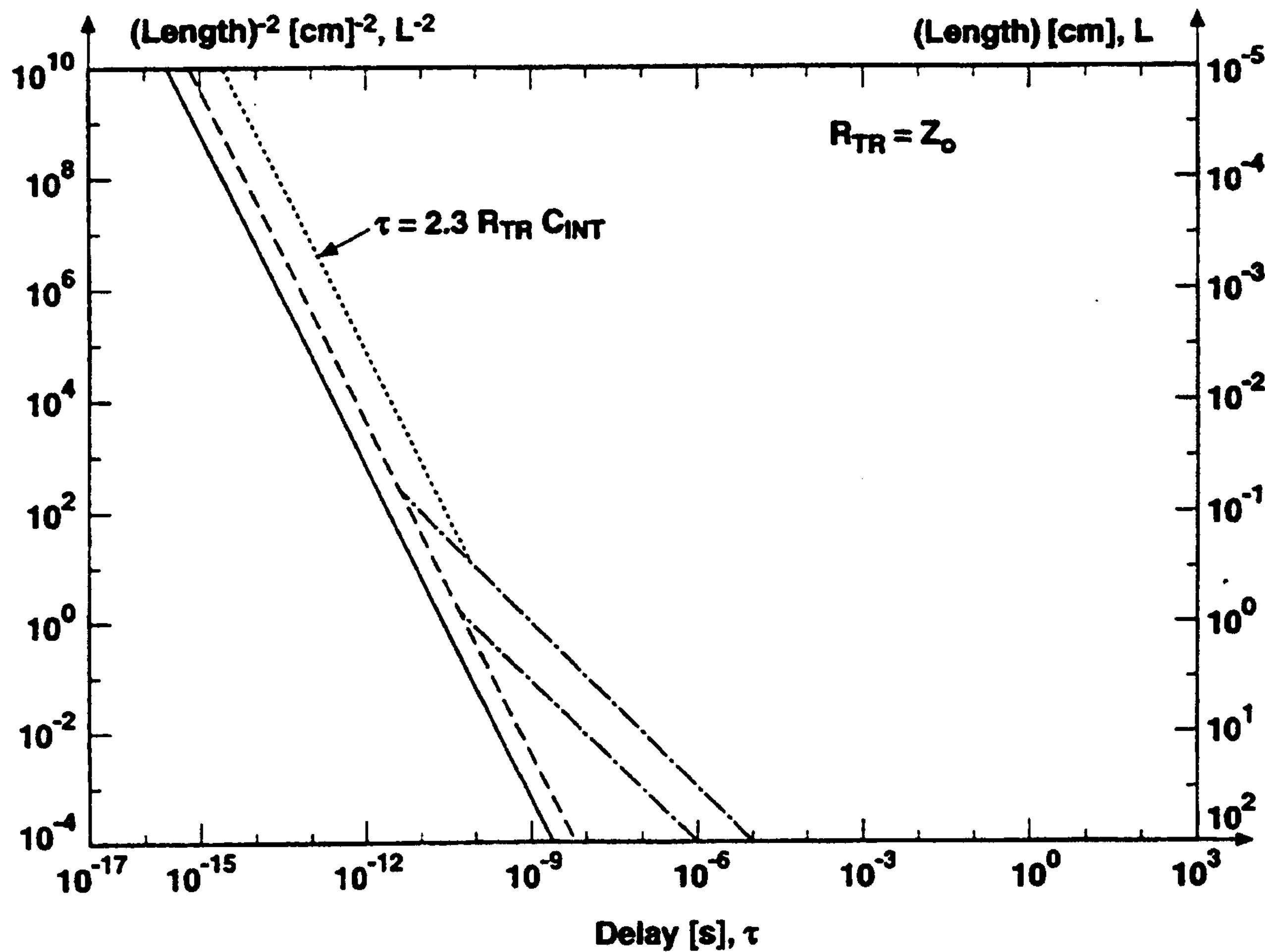


Fig. 18. $(1/L)^2$ versus τ for fundamental, material, device, and circuit limits on interconnects. Circuit limits represent the response time of a circuit consisting of a MOSFET driving a lumped interconnect capacitance.

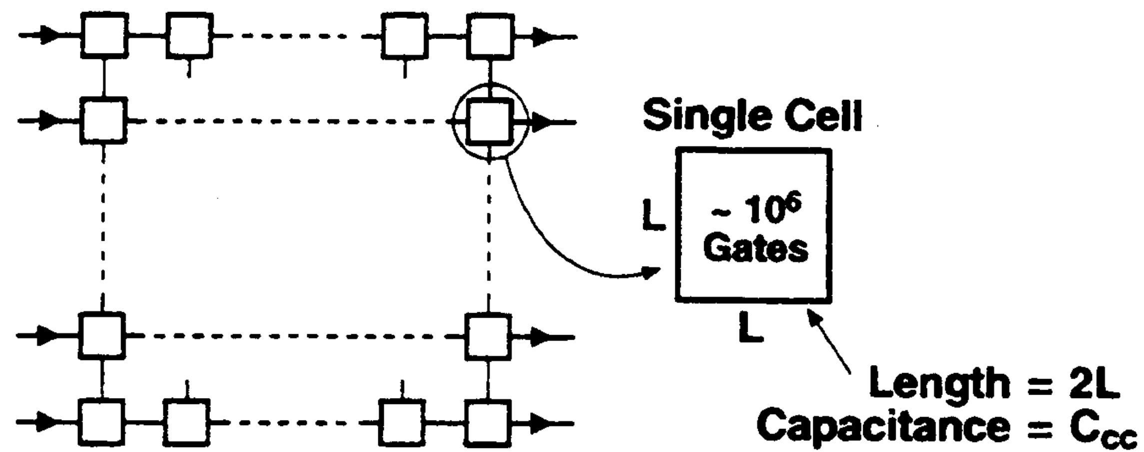
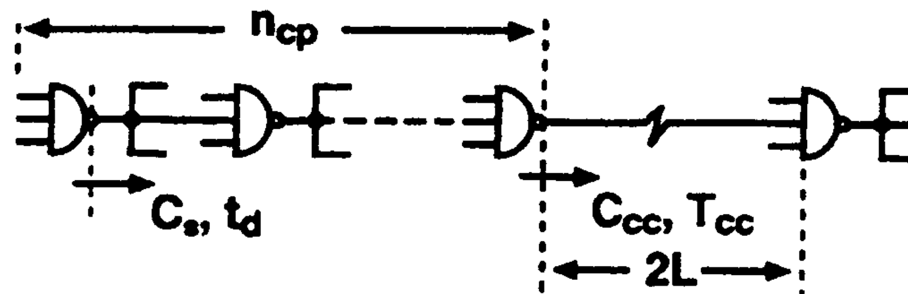


Fig. 19. Systolic array system block diagram.

System Switching Energy Limit



$$P_S t_{ds} = a C_s \left[1 + \frac{C_{cc}}{n_{cp} C_s} \right] V_o^2$$

Fig. 20. Critical path used to define the system switching energy limit.

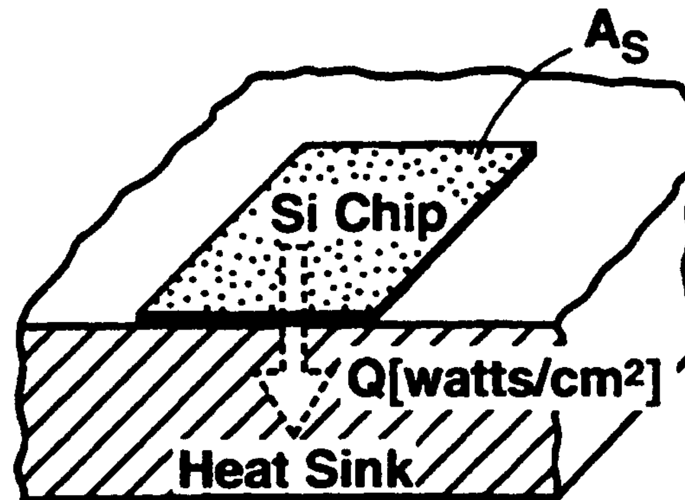


Fig. 21. System heat removal limit based on packaging.

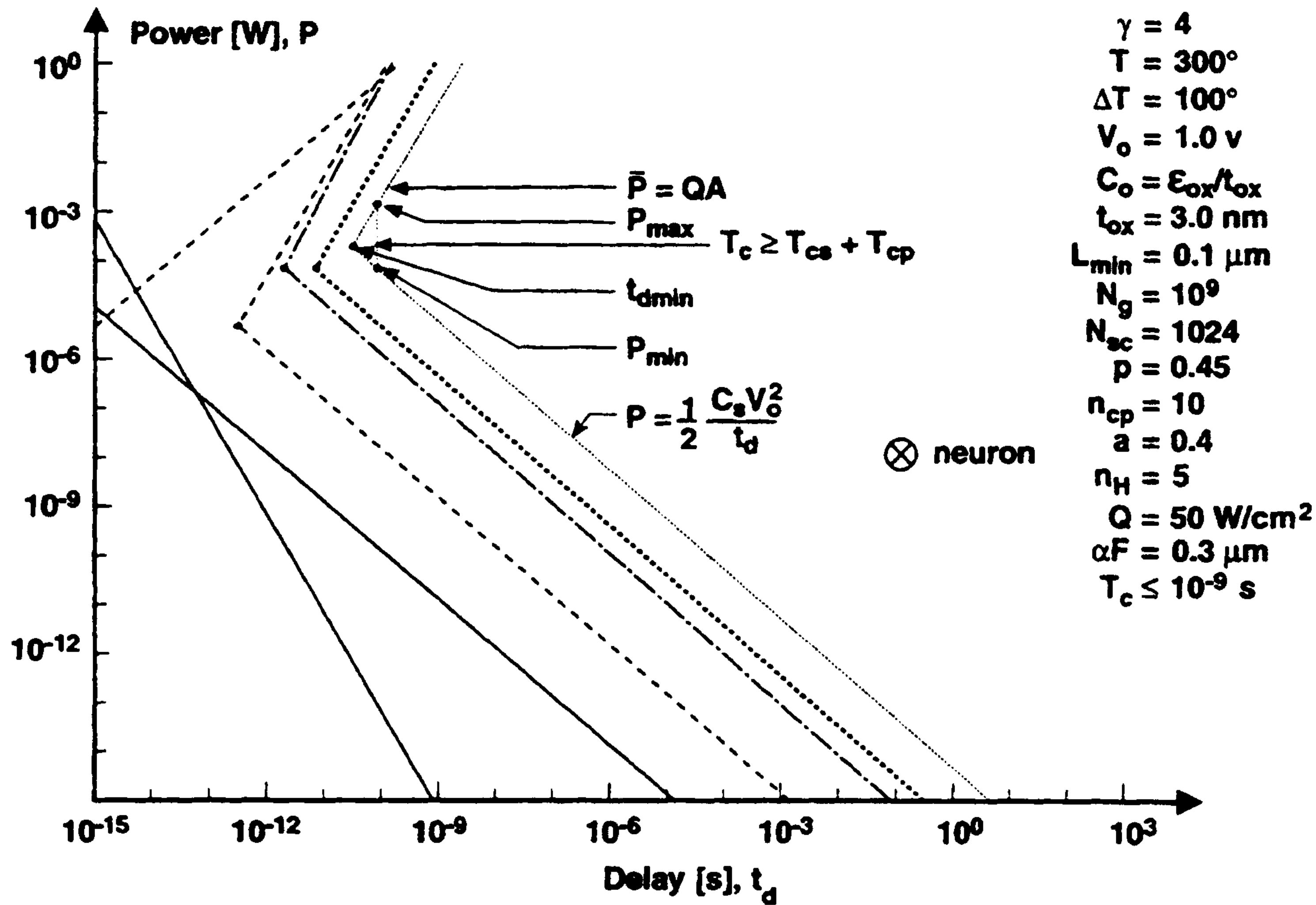


Fig. 22. P versus t_d for fundamental, material, device, circuit, and system limits. System limits are imposed by switching energy ($Pt_d = \frac{1}{2}C_s V_o^2$), heat removal ($\overline{P} \leq QA$), and cycle time ($T_c \geq T_{cs} + T_{cp}$) requirements.

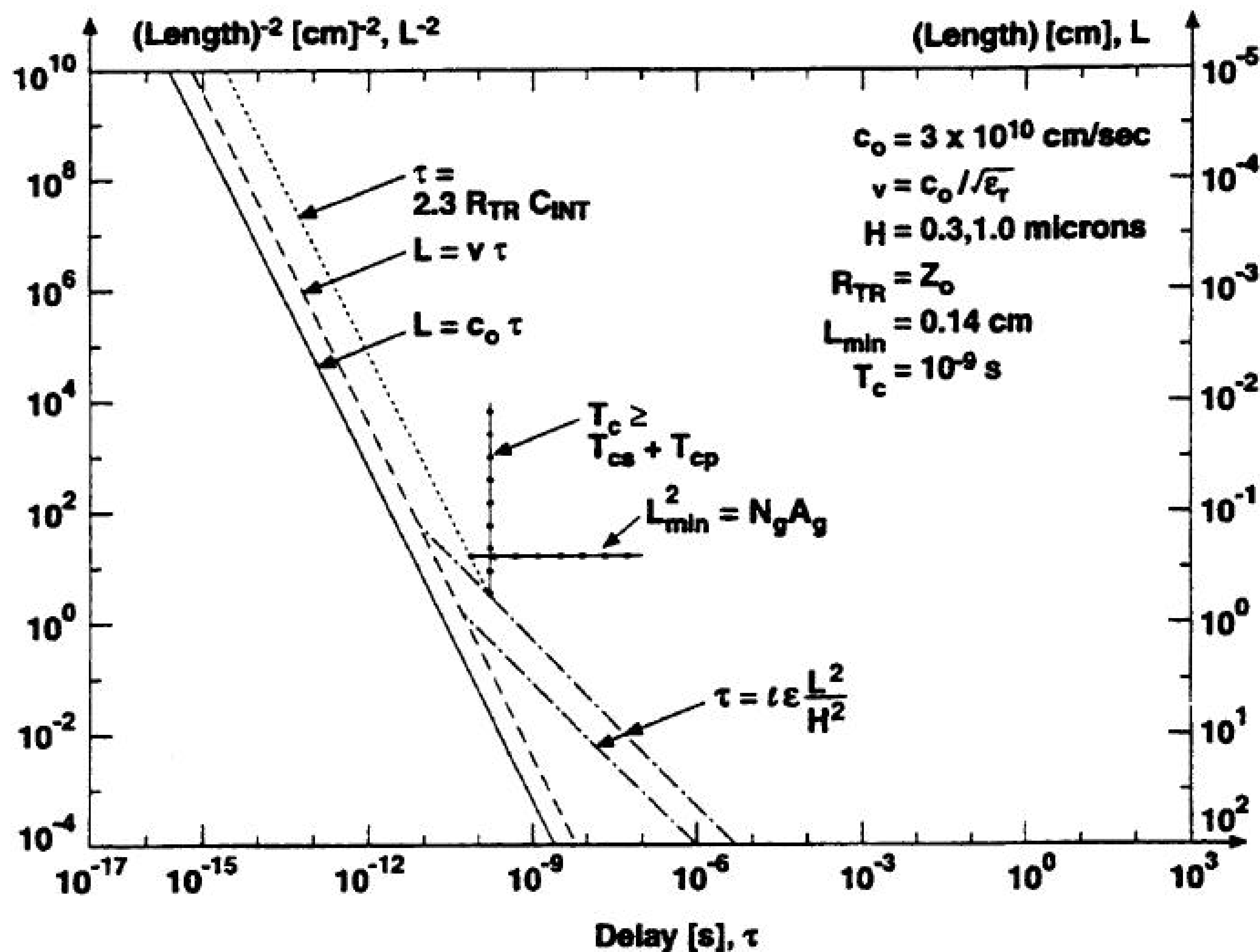
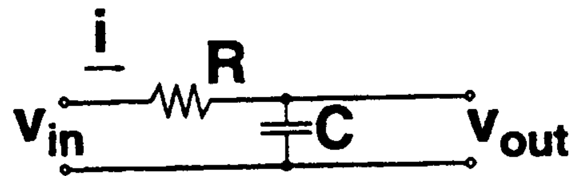
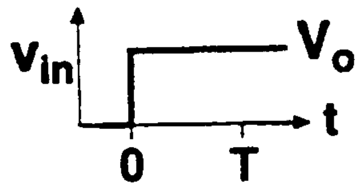


Fig. 23. $(1/L)^2$ versus τ for all levels of the hierarchy. System limits are imposed by global interconnect response time designated by $T_c \geq T_{cs} + T_{cp}$ and length designated by $L_{\min}^2 = N_g A_g$.

Quasi-Adiabatic Switching

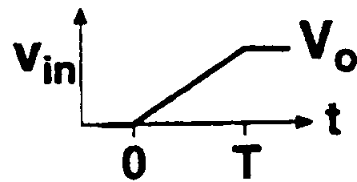


$$E = \frac{1}{2} C V_o^2$$



$$E = \frac{1}{2} C V_o^2 \left[\frac{2RC}{T}\right]$$

$$T >> 2RC$$



$$E = \int_0^\infty i^2 R \, dt$$

Fig. 24. Quasi-adiabatic switching.

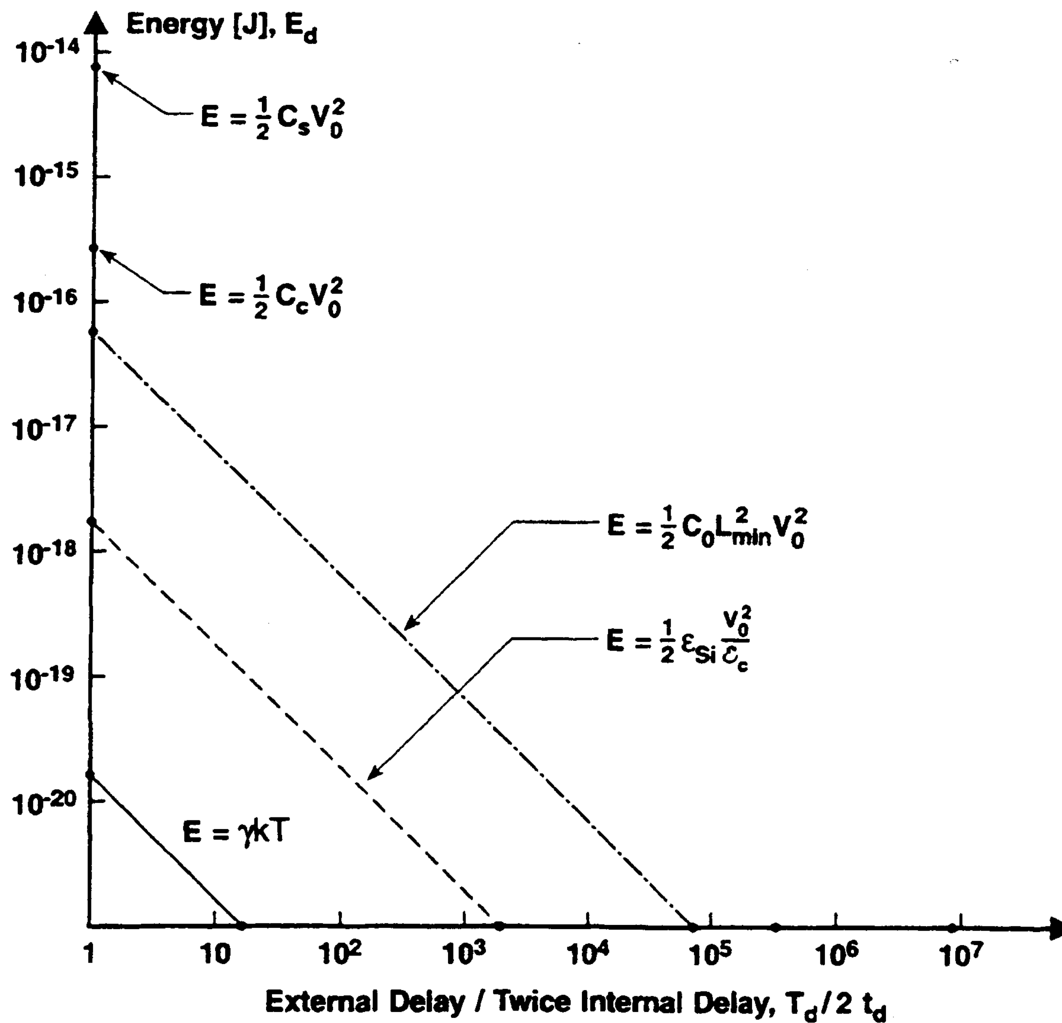


Fig. 25. Energy dissipation E_d during a switching transition versus the ratio of twice internal transition time $2t_d$ to external transition time T_d.

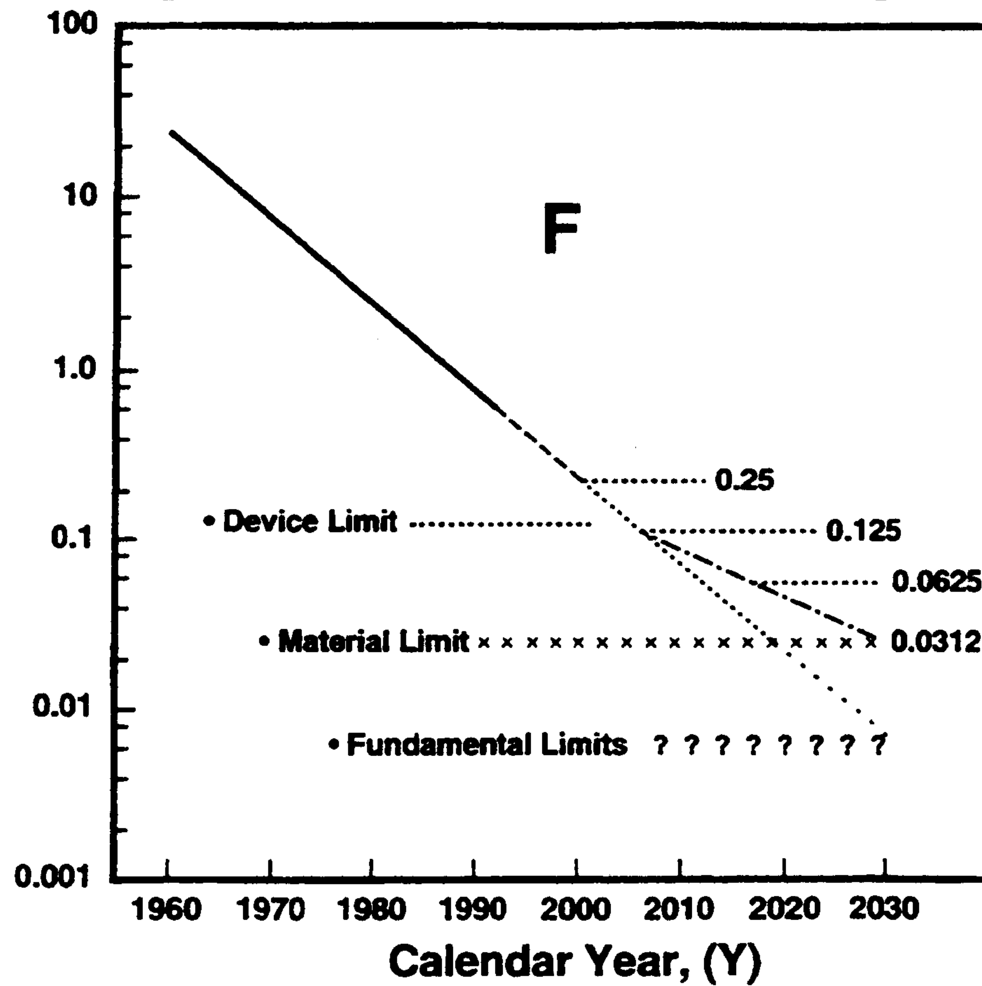


Fig. 26. Average minimum feature size F versus calendar year Y.

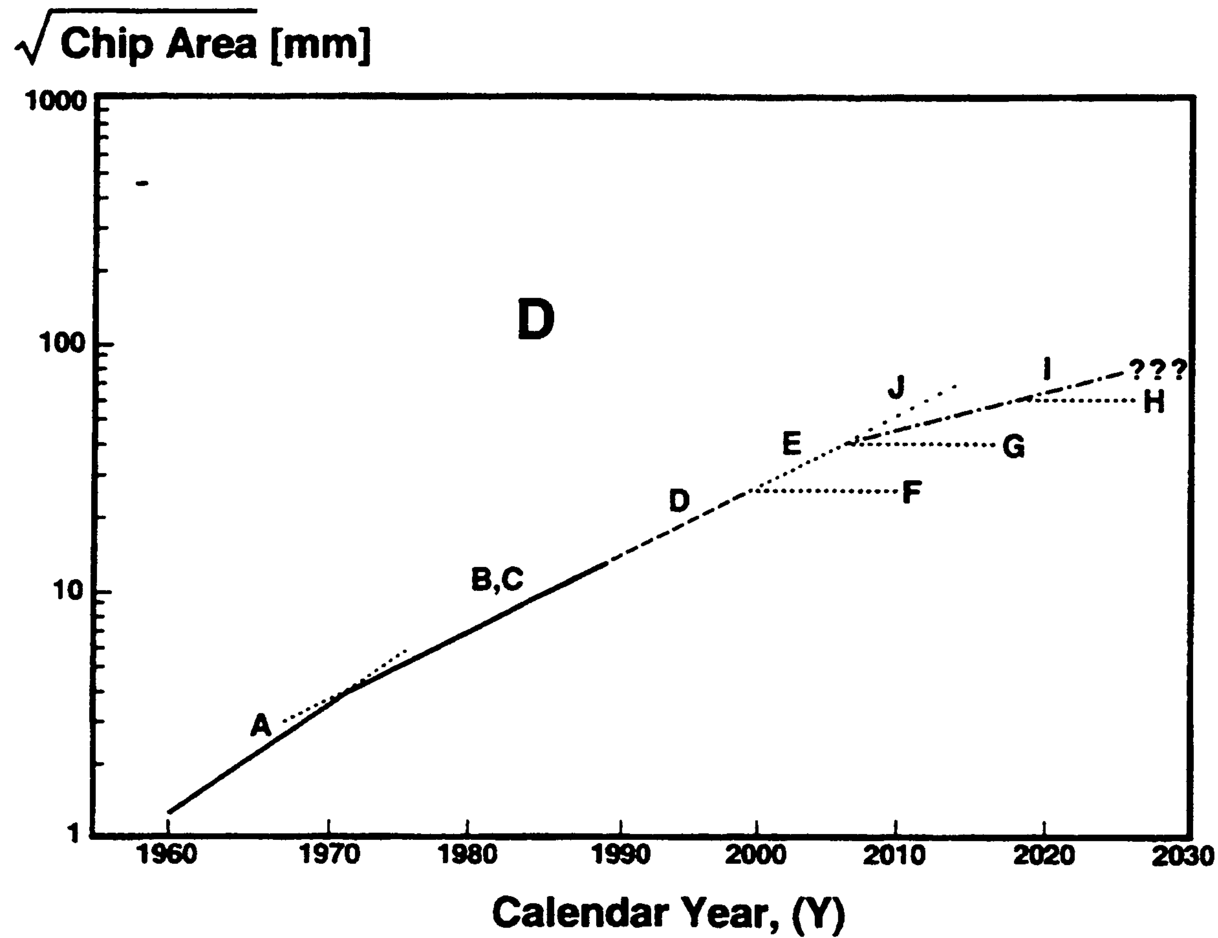


Fig. 27. Square root of die area D versus calendar year Y. $\sqrt{\text{die area}} = D$.

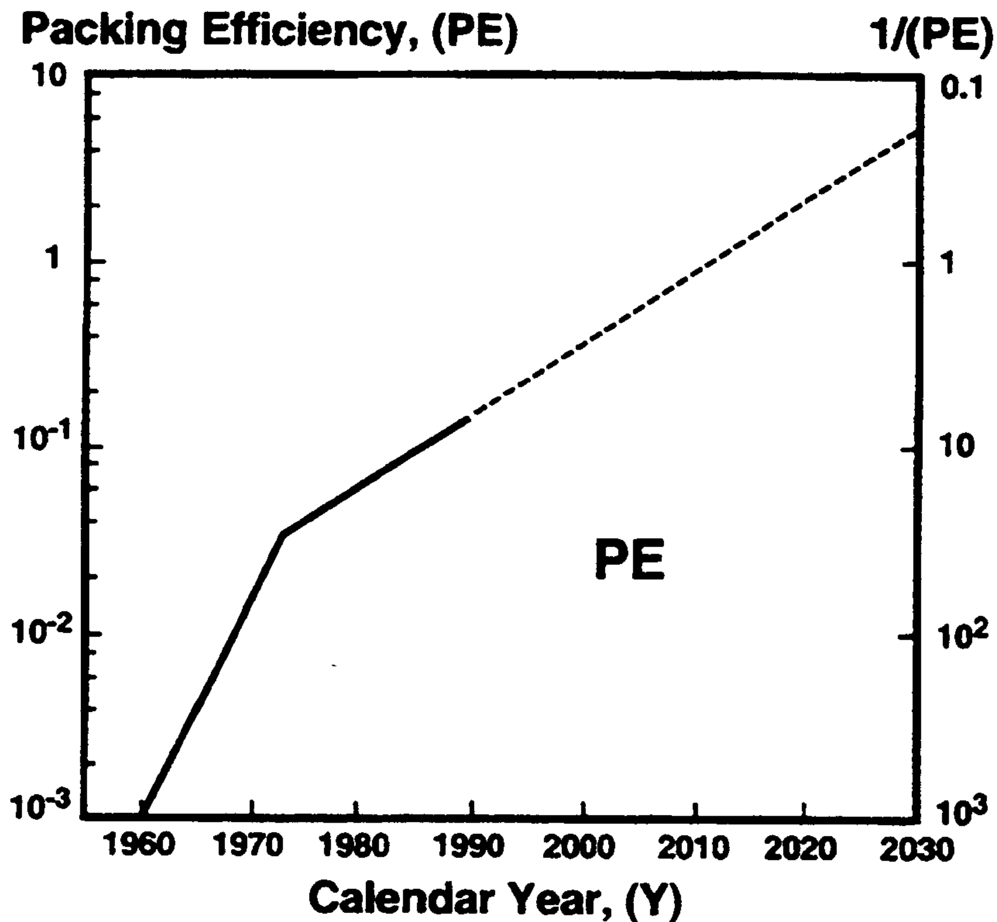


Fig. 28. Packing efficiency PE versus calendar year Y. Note that packing efficiency is defined as the number of transistors per minimum feature area.

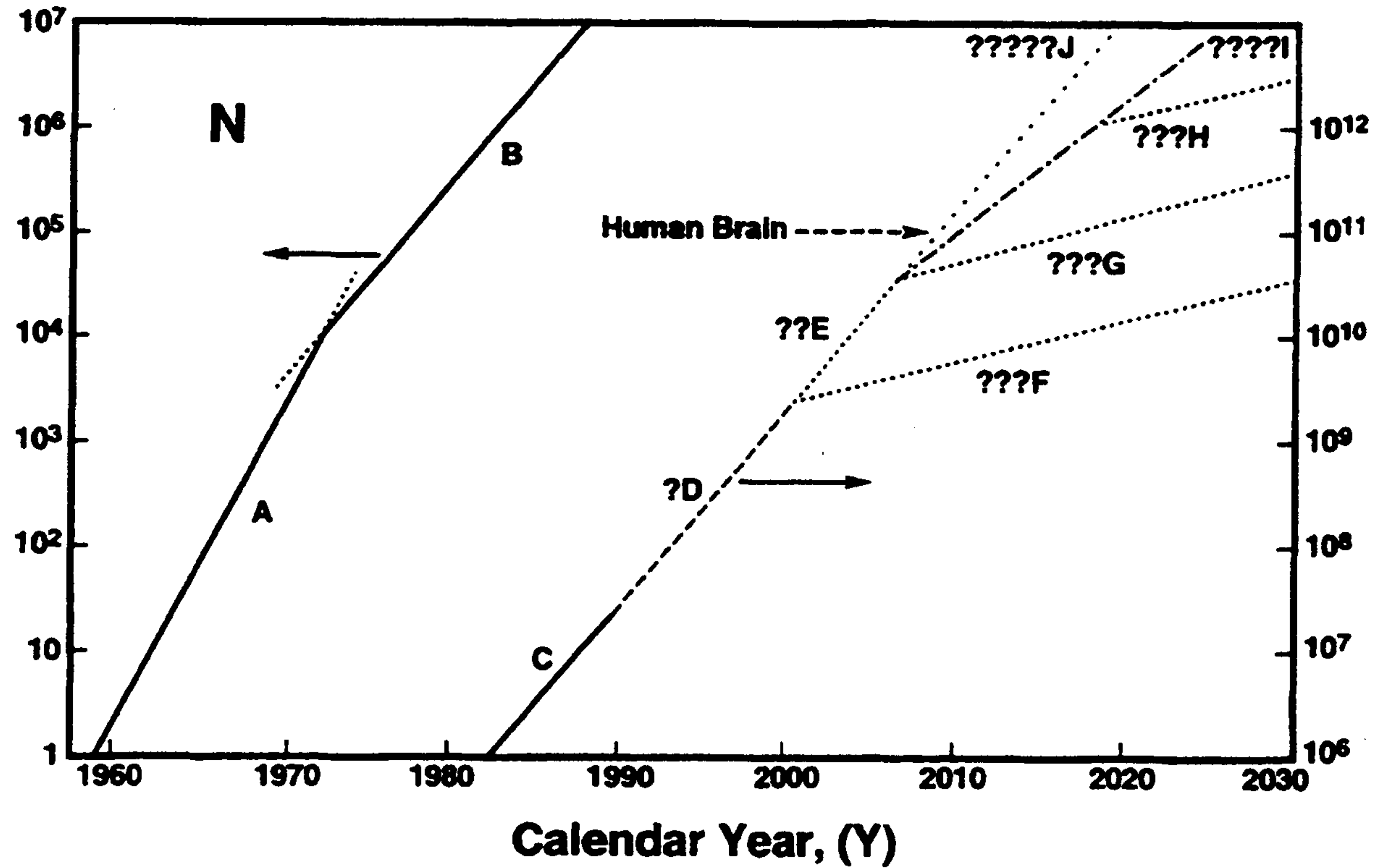


Fig. 29. Number of transistors per chip N versus calendar year Y.

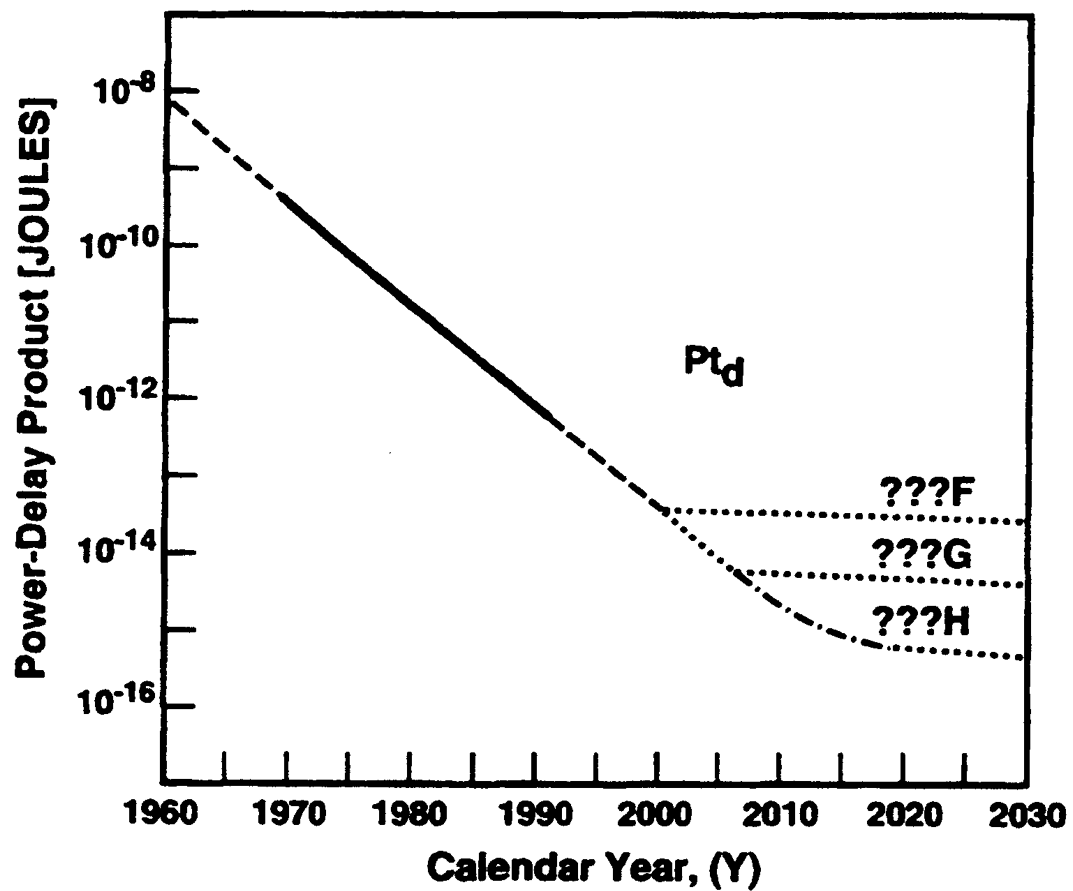


Fig. 30. System level power-delay product Pt_d versus calendar year Y.

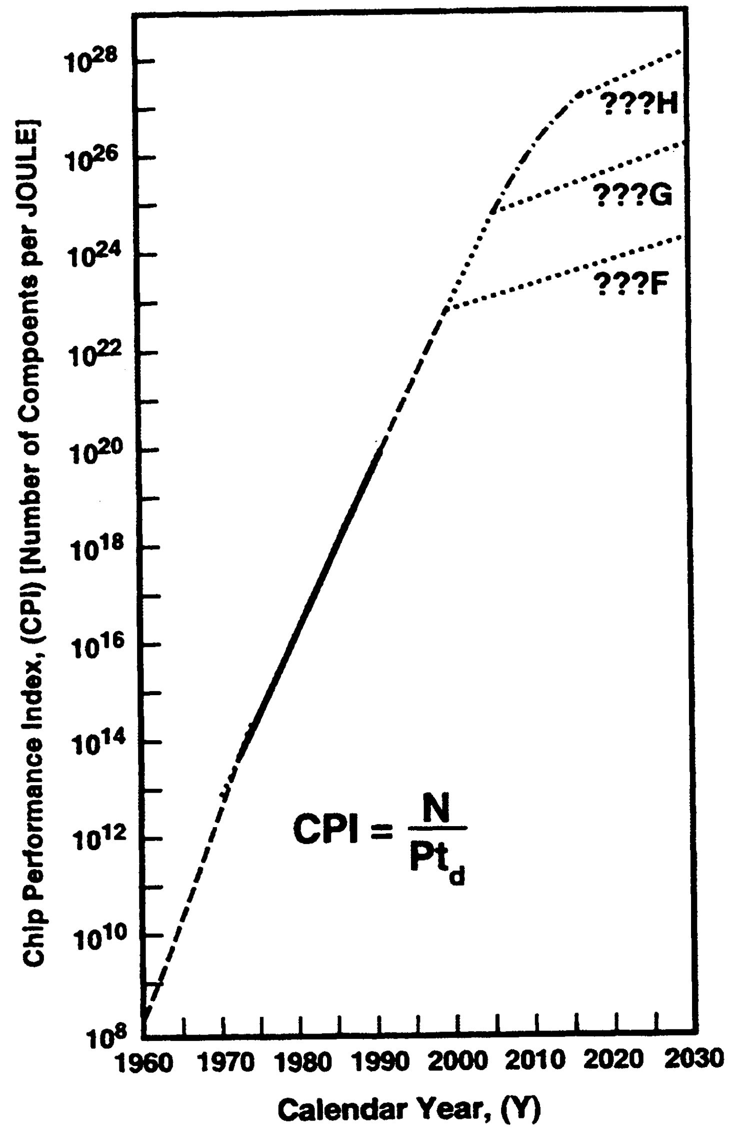


Fig. 31. Chip performance index $CPI = N/Pt_d$ versus calendar year Y.