Sea of Leads (SoL) Characterization and Design for Compatibility with Board-Level Optical Waveguide Interconnection

Muhannad S. Bakir, Hollie A. Reed*, Anthony V. Mule',
Paul A. Kohl*, Kevin P. Martin, and James D. Meindl

School of Electrical and Computer Engineering, *School of Chemical Engineering
Microelectronics Research Center; Georgia Institute of Technology
Tel: (404) 894-9457; e-mail: mbakir@ece.gatech.edu

Abstract – Sea of leads (SoL) is a novel ultra-high-density compliant wafer-level packaging technology. The x-y-z compliant input/output (I/O) leads are batch fabricated by simply extending wafer-level batch fabrication of on-chip multilevel interconnect networks. Two-port microwave measurements reveal that the leads exhibit an insertion-loss of less than 0.4dB in the 0.1-45GHz frequency range. In addition, worst-case insertion-loss of signal propagation into and out of the package is 1.15dB at 45GHz. Because the compliant leads are short, their electrical parasitics are minimal. A mixed-signal system-on-a-chip (SoC) requires packages that are compatible with optical interconnect technology. Physical design rules describing SoL design compatibility with board-level optical signal distribution via waveguides are derived.

I. Introduction

A key interconnection level that will be severely challenged by gigascale integration (GSI) is the chip-to-module interconnection that integrates the packaged chip into the system. A gigascale system-on-a-chip (SoC) demands the development of new and cost effective integrated input/output (I/O) interconnect solutions that use high-performance integrated electrical, optical, and RF approaches to meet all of the I/O requirements of the 50 to 35nm International Technology Roadmap for Semiconductors (ITRS) technology nodes [1]. Meeting these challenges is essential for the semiconductor industry to transcend known limits on interconnects that would otherwise decelerate or halt the historical rate of progress toward GSI and beyond. In general, power, clock, and signal I/O functions will be met by the selective integration of fine pitch electrical (<30μm pitch area array), optical, and RF I/O interconnect technologies. These high-density integrated I/O interconnects will be especially important for novel 3D structures as well as for high current (>400A) and high bandwidth (>40 Tbs) applications. To investigate the above issues, focus must be given to overcoming long-range and fundamental barriers in chip-to-module interconnects by advancing fine-pitch compliant interconnections, optoelectronic and RF interconnections, and wafer-level testing and burn-in.

Sea of Leads (SoL) is a novel ultra high-density packaging technology designed to meet future chip-to-module interconnection needs. Unlike conventional packaging, SoL simply extends wafer-level batch fabrication of multilevel interconnect networks to include the chip's I/O leads. In fact, through a series of massively parallel process steps following back-end processing, dice across the wafer are monolithically packaged with x-y-z compliant leads. SoL I/O density has been shown to exceed 10^4/cm^2 and may potentially provide package I/O pitches equal to the pitches of the top most global wiring level. SoL packages may be mounted on substrates with significantly higher coefficient of thermal expansion (CTE) than the chip without the need for underfill due to the compliant package interconnects [2]. In addition, z-axis compliance allows reliable electrical contact to be attained between non-planar wafer and probe card surfaces during wafer-level testing and burn-in. As a result, key opportunities of wafer-level processing and testing of SoL packages include reduced cost of packaging, testing, and burn-in. In addition, the need for underfill is eliminated.

First, this paper describes SoL fabrication and demonstrates SoL's process integration with an existing front-end-of-the-line (FEOL) and back-end-of-the-line (BEOL) processes. Section III presents two-port microwave measurements of a SoL package in the 0.1-45GHz frequency range and highlights some of the key opportunities of performance enhancement SoL offers a mixed-signal SoC. Section IV examines SoL design compatibility with board-level optical signal distribution. Physical models are derived to illustrate design compatibility issues. Finally, Section V is the conclusion.

II. FEOL, BEOL, and SoL Process Integration

The compliant sea of I/O chip interconnects, which are essentially microelectromechanical systems (MEMS), are fabricated through a series of monolithic process steps on the surface of a low modulus polymer with embedded air-gaps rendering the wafer ready for wafer-level testing and burn-in as shown in Fig. 1. SoL's complete fabrication process is schematically illustrated in Fig. 2. The air-gaps provide high z-axis compliance, potentially up to 50μm as approximately required for wafer-level burn-in [3]. Fig. 3 is an SEM micrograph illustrating a section of a fabricated SoL package with $12x10^3$ x-y-z compliant interconnects distributed across a single cm^2. Processing $12x10^3$ leads per cm^2 on a 300mm wafer translates into fabricating more than *8x10*^{6} chip I/O leads through a sequence of massively parallel process steps. The leads are oriented normal to the chip's contours of expansion for a higher degree of

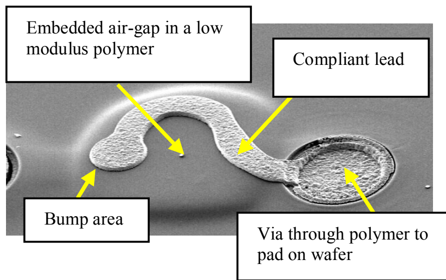

Fig. 1: SEM micrograph of a compliant lead fabricated above a highly compressible air-gap.

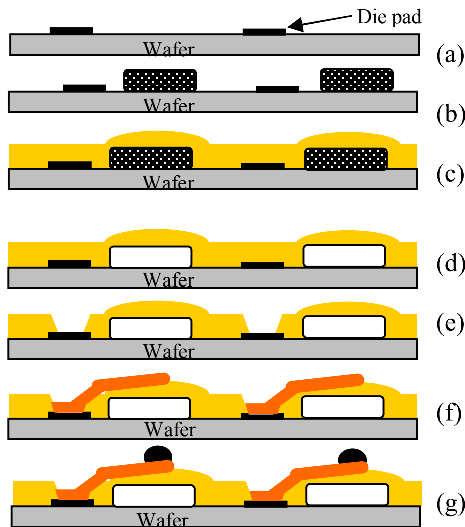

Fig. 2: SoL fabrication process (a) wafer with FEOL and BEOL processes complete: die-pads are fabricated (b) SoL packaging immediately follows BEOL processing: application and patterning of sacrificial polymer film (c) deposition of overcoat polymer to encapsulate the sacrificial polymer layer (d) the wafer is placed in a furnace with appropriate temperature profile (<250°C maximum temperature) to decompose the sacrificial polymer leaving behind hollow air-gaps (e) vias are etched in the overcoat polymer to expose the die pads (f) the compliant leads are plated after proper seed layer deposition and resist patterning (g) fabrication of package bumps.

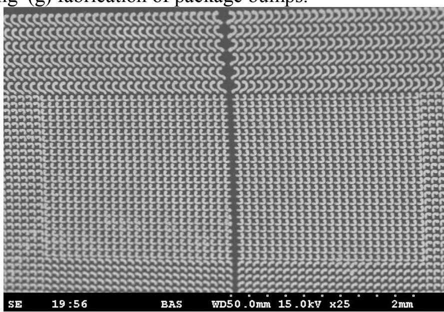

Fig. 3: SEM micrograph showing 53µm long leads on an 80x80µm square lattice and 106µm long leads on an 80x160µm rectangular lattice distributed at the package's inner and outer regions, respectively. This distribution maximized the package I/O density yielding a package with 12,000 x-y-z compliant leads distributed across a single cm^2.

compliance. In addition, the package I/O density is increased through the design of larger, more compliant leads at the chip edges and smaller, less compliant leads at the chip's inner regions. Dice across a wafer with complete front-end and back-end processing have been packaged with SoL at wafer-level and Fig. 4 is a chip micrograph illustrating one of the packaged dice. This figure illustrates the process compatibility between FEOL, BEOL, and SoL.

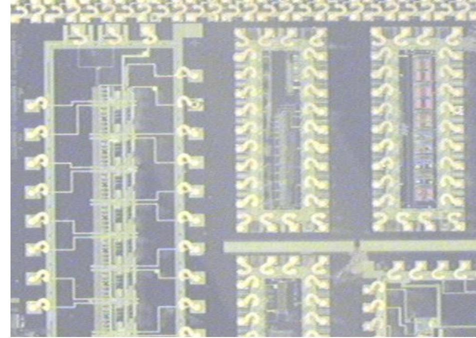
Fig. 4: Chip micrograph illustrating a packaged die with SoL at wafer-level. This demonstrates FEOL, BEOL, and SoL process compatibility.

III. SoL Electrical Characterization and Opportunities of Performance Enhancements for a SoC

Due to the short compliant leads, SoL packages exhibit high electrical performance. Using a HP8510C network analyzer with 150µm pitch ground-signal-ground (GSG) coplanar probes, two-port measurements of the SoL package shown in Fig. 3 were made at wafer-level. Fig. 5 is a plot of the insertion-loss and return-loss of the large leads located at the die's edge. In this measurement, both the leads and the polymer were each 15µm thick. Next, GSG two-port measurements were performed on a pair of leads connected by a 100µm long copper (Cu) trace fabricated on the wafer's passivation layer (silicon-nitride). As shown in Fig. 6, this measurement characterized GSG signal propagation through the aggregate physical path that is composed of a compliant lead, polymer via, on-chip Cu trace, back up a second polymer via, and finally through the second lead. In this measurement, the compliant leads were 10µm thick, the polymer was 15µm thick, and the Cu trace was 1µm thick. The width of all interconnect structures was approximately 20µm.The measurement was made for both the large and small compliant leads shown in Fig. 3 and the results for both sets of data are shown in Fig. 7. The total physical length of the measured electrical path, including the on-chip Cu trace, is approximately 330µm for the large lead pair and 210µm for the small lead pair. The performance of the small and the large compliant leads is identical up to 7GHz, and thereafter, the smaller leads exhibit better performance. These results do not include the effects of solder bumps. However, it is expected that the solder bumps compliant with SoL dimensions will add minimal parasitics.

A particularly disruptive aspect of SoL is the set of performance enhancement opportunities it offers a mixed-signal SoC. With an I/O density exceeding 10^4 leads per cm^2, SoL can enhance power distribution, increase I/O bandwidth, satisfy 3D structure I/O demands, suppresses simultaneous switching noise, and improve isolation in a

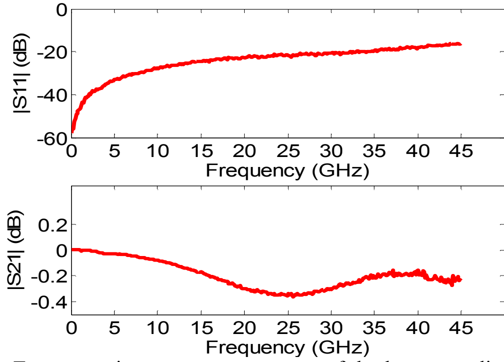

Fig. 5: Two-port microwave measurements of the large compliant leads located at the chip edge (see Fig. 3). In this measurement, both the leads and the polymer were each 15µm thick. Air-gaps were not fabricated.

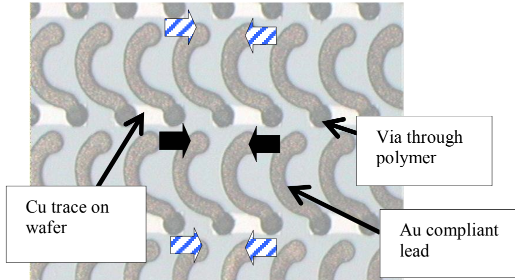

Fig. 6: Two-port microwave ground-signal-ground (GSG) probe setup used to characterize GSG signal propagation through the aggregate physical path that is composed of a compliant lead, polymer via, on-chip copper trace, back up a second polymer via, and finally though the second lead. The leads are gold (Au) plated. The solid arrows refer to the signal probes and the stripe arrows refer to the ground probes.

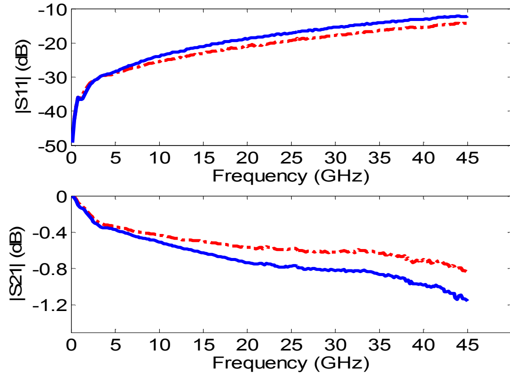

Fig. 7: Two-port microwave measurements of both the large and small compliant leads pairs shown in Fig. 3. The solid line refers to the measurements of the large lead pair and the dashed lined refers to the measurements of the small lead pair. In this measurement, the compliant leads were 10µm thick, the polymer was 15µm thick, and the Cu trace was 1µm thick. No embedded air-gaps were fabricated.

mixed-signal system. Separate power distribution networks for analog and digital macro cells in a mixed-signal system are potentially possible with SoL. In addition, SoL technology can be used to route critical global interconnects off-chip and onto the substrate to achieve a time of flight global clock frequency [4]. SoL can also facilitate the distribution of high current (hundreds of amps) and multi-GHz chip-to-board signals as projected by the ITRS for the 35nm technology node high-performance systems [1]. If $8\text{x}10^3$ leads are devoted to signal distribution, then the package shown in Fig. 3 can potentially achieve an aggregate electrical bandwidth of 40Tb/s-cm^2 when operated at 5GHz.

IV. Compatibility Analysis between SoL and Board-Level Optical Waveguide Interconnection

Distributing a multi-GHz electrical signal through on-chip interconnects requires very careful analysis due to the RLC parasitics in long global interconnects that contribute to power losses and signal degradation. One potential approach of overcoming such issues is through the use of board-level optical signal distribution via waveguide interconnections [5] with diffractive preferential-order focusing volume waveguide grating couplers [6]. The idea is that an optical signal can be routed on the board to the point where it can be directly out coupled and focused onto a chip-level detector as shown in Fig. 8. While it is possible to design the grating coupler to meet the physical dimension requirements of the package [5, 6], this section briefly describes how the SoL package can be designed to be compatible with a waveguide grating coupler.

The first compatibility challenge with the proposed optical distribution scheme is waveguide routability between the sea of I/O interconnections as abrupt bends may contribute to significant power losses. Even if the waveguide is routed to a point directly below the detector, there are still some compatibility issues to be resolved. The photo-sensitive package polymer must be transparent to the wavelength of the optical signal. In addition, because of the air-polymer interface (see Fig. 8), ray refraction causes a shift in focal point. One way to reconverge the beam onto the detector is to alter the thickness of the package overcoat polymer. The range of polymer thickness required to reconverge the optical beam can be expressed as

$$t_{poly} = \frac{L \pm d - \left(t_{sep} - t_{waveguide+coupler}\right)\left(\dfrac{1}{\tan\theta_1} + \dfrac{1}{\tan\theta_2}\right)}{\tan\beta_1 + \tan\beta_2} \qquad (1)$$

where $t_{waveguide+coupler}$ is the thickness of the optical waveguide and coupler combined, θ_1 and θ_2 are the angles at which the guided wave diffracts, d is the largest tolerated beam width at the detector, and L is the coupler length. The physical separation between the coupler and the package polymer surface is t_{sep}-$t_{waveguide+coupler}$, where t_{sep} is

$$t_{sep} = t_{pwb_wires} + t_{solder} + t_{lead}\,, \qquad (2)$$

where t_{pwb_wires} is the thickness of the PWB interconnects, t_{solder} is the thickness of the solder bumps, and t_{lead} is thickness of the package leads as shown in Fig. 8. Finally,

$$\beta_i = \sin^{-1}\left(\frac{\cos(\theta_i)}{n_{poly}}\right),\ \text{i=1,2}\,, \qquad (3)$$

where n_{poly} is the polymer's index of refraction at the appropriate wavelength. The polymer thickness is also

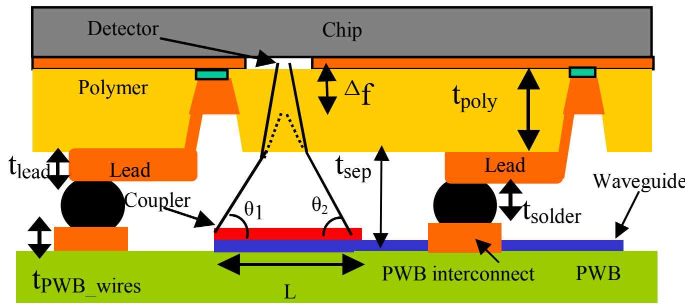

Fig. 8: A schematic representation of the proposed optical distribution in [5]. This paper analyzes the design and compatibility of SoL packages with the proposed optical distribution.

constrained by the electrical vias that must posses sloped sidewalls to provide reliable seed layer coverage for good plating. As the polymer thickness increases, the via opening at the top increases, which reduces the net planer polymer surface area available to fabricate the compliant leads. Fig. 9 summarizes the change in focal point and the necessary polymer thickness to reconverge the optical beam as a function of various physical parameters. While a shorter coupler reduces the shift in focal point, the coupling efficiency is an exponential function of the coupler length [6] and thus, the coupler cannot be too short as poor coupling efficiency results.

It is interesting to note that t_{sep} influences both the electrical and optical interconnection performance. For example, Eqn. (2) shows that in order to increase t_{sep} and thus enhance optical compatibility as shown in Fig. 9, the thickness of one or more of the electrical interconnects must be increased. In general, thicker electrical interconnects yield shorter signal propagation delay. In addition, increasing the thickness of the package leads was noted to enhance the microwave characteristics. However, increasing bump thickness generally degrades its electrical performance. Thus, either increasing the lead thickness and/or the PWB interconnect thickness would increase t_{sep} without potential side effects. Another potential method of increasing the coupler-package separation is the fabrication of embedded air-gaps under each lead as illustrated in Fig. 1. If 15μm air-gaps are fabricated, the new coupler-to-polymer separation will increase by 10-15μm (depending on overcoat step coverage), which decreases the shift in focal point. In addition, it is also possible to reduce the magnitude of ray-refraction by modifying the package structure by either etching full or partial optical vias in the package polymer, although its consequences on the package reliability are unknown.

V. Conclusion

Sea of Leads (SoL) is a novel ultra-high-density compliant wafer-level packaging technology. The insertion-loss of ground-signal-ground path into and out of the package is found to be less than 1.2dB at 45GHz.

L=150μm, $\theta_1=\theta_2=45°$, d=10μm, via sidewall ∠=75°				
t_{sep} (μm)	30	40	50	60
Δf (μm)	36.8	26.4	15.9	5.45
t_{poly} (μm)	81.8	61.4	40.9	20.45
Effective via diameter (μm) at polymer's surface	61.8	50.9	39.9	29.0
L=200μm, $\theta_1=\theta_2=45°$, d=10μm, via sidewall ∠=75°				
t_{sep} (μm)	30	40	50	60
Δf (μm)	63.0	52.5	42.0	31.0
t_{poly} (μm)	133.0	112.5	92.1	71.6
Effective via diameter (μm) at polymer's surface	89.3	78.3	67.3	56.4

Fig. 9: Table summarizing the compatibility between SoL and board level optical signal distribution as a function of coupler length and package polymer-board separation, t_{sep}. The above results indicate that Δf and t_{poly} decrease as t_{sep} increases. In addition, shorter couplers reduce the necessary polymer thickness to reconverge the optical beam and thus yield smaller via openings. The via diameter on the mask is assumed to be equal to 18μm. The value of t_{poly} calculated in the table is equal to the lower limit of the range described by Eqn. (1).

Because a mixed-signal system-on-a-chip integrates electrical as well as optical components, a preliminary compatibility analysis between SoL and board-level optical signal interconnection using waveguides indicates that package-coupler separation influences the shift in focal-point due to ray refraction. Increasing lead thickness as well as fabricating embedded air-gaps within the package polymer layer reduce the magnitude of ray refraction and potentially enhance electrical performance. Future work will include rigorous SoL reliability testing.

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