

A 10 GHz Hybrid Optical/Electrical Clock Distribution Network for Gigascale Integration *

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Abstract

A novel system-level model describing hybrid optical/electrical clock distribution networks in future gigascale architectures is presented. Technological and architectural properties for a high performance microprocessor implemented in 50nm technology are projected for the microelectronic environment. A printed circuit board-level, high-fanout, curved aperture optical waveguide H-tree network globally distributes an intensity-modulated optical signal to monolithic CMOS-based receivers to provide local clock distribution. Approximately 1W of optical input power will be required to propagate globally a local clock frequency of 10GHz to ~1024 individual nodes and thus eliminate the need for local frequency multiplication circuitry.

Introduction

One proposed alternative to avoid the global electrical interconnection limitations that inhibit multi-GHz microprocessor clock frequency distribution [1] is the use of global optical clock distribution networks (OCDNs) [2,3]. Architectural projections for gigascale microprocessors implemented in 50nm technology call for single-chip *multi*processors to overcome conventional single core throughput [4]. There is a need for local frequency multiplication circuitry within each node of a *multi*processor operating at 10GHz due to the inherent bandwidth limitations of global interconnections [5]. To avoid the need for frequency multiplication circuitry within each processing node, a performance requirement for an optimized OCDN is the capability to propagate the local clock frequency globally across chip.

Optical Clock Distribution Network

Figure 1 illustrates the structure under consideration, which exhibits the following key features: a) no on-chip photonic sources; b) monolithic silicon-based detection; c) global optical signal propagation through a board-level guided-wave H-tree distribution ; and d) the use of surface relief focusing grating couplers to provide tolerance relative to horizontal and vertical misalignment of the flip-chip assembly (Fig. 2, Table 1).

Key Components of Distribution

To estimate accurately the performance of a hybrid optical/electrical clock distribution network, three key

properties must be evaluated based on the parameters of Table 2: a) the amount of optical power *available* for chip-level detection at each output of the H-tree distribution (Fig. 3); b) the incident optical power *required* by the monolithic receiver within each node for operation at a specific bit error rate (BER) and bit-rate (Fig. 3)[6]; and c) the minimum *required* fanout of the optical distribution, determined by the maximum number of gates confinable within each processing node given a local clock frequency of 10GHz and maximum chip power density of 50 W/cm² (Table 3) [7]. Estimations of gain-bandwidth properties for a simple three-transistor single-ended CMOS transimpedance amplifier [8] (Figs. 4 and 5) are based on small signal values predicted by the physically-based transregional drain current model [9].

Conclusions

Global propagation of the 10GHz local clock frequency projected for 50nm CMOS technology generations will require ~1W of system-level optical input power. Input power requirements may be eased by higher-efficiency Y-junctions and grating couplers, as well as receiver topologies exhibiting lower input-noise.

References

1. The International Technology Roadmap for Semiconductors, SIA, 1998 revision.
2. J.W Goodman, F.J. Leonberger, S.C. Kung, R.A. Athale, , "Optical interconnections for VLSI systems". Proc. IEEE vol.72, pp.850-66, July 1984.
3. L.C. Kimerling, et al., "Materials for monolithic silicon microphotronics". Materials and Devices for Silicon-Based Optoelectronics Symposium pp.45-56, 1998.
4. W. Dally, "VLSI architecture: past, present, and future," Proc. ARVLSI99', IEEE Computer Soc. Press, Los Alamitos, Calif., 1999, pp. 232-241.
5. D. Matzke, "Will physical scalability sabotage performance gains?". Computer, vol. 30, pp. 37-39, Sept. 1997.
6. J.J. Morikuni, A.Dharchoudhury, Y.Leblicic, and S.M.Kang, "Improvements to the standard theory for photoreceiver noise". J. Lightwave Tech., vol.12, pp.1174-1183, July 1994.
7. Azeez J. Bhavnagarwala, B. L. Austin, K. A. Bowman, and J. D. Meindl, "A Minimum Total Power Methodology for Projecting Limits on CMOS GSI", submitted, JSSC, Jan. 1999.
8. A.V. Krishnamoorthy, D.A.B. Miller, "Scaling optoelectronic-VLSI circuits into the 21st century: a technology roadmap". IEEE J. Select. Topics Quantum Electron. vol.2, p.55-76, April 1996.
9. B.L.Austin, K.A.Bowman, X. Tang, and J.D.Meindl, "A low power transregional MOSFET model for complete power-delay analysis of CMOS gigascale integration (GSI)". Proc. ASIC Conf., pp.125-129, Sept. 1998.

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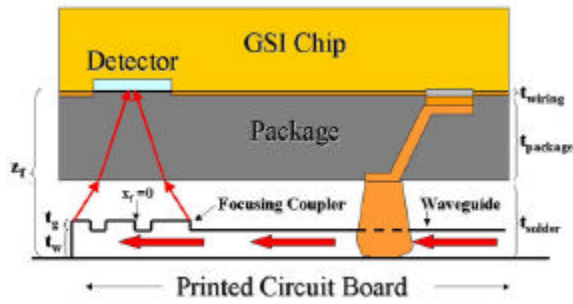


Fig. 1: Proposed structure of OCDN (not to scale)

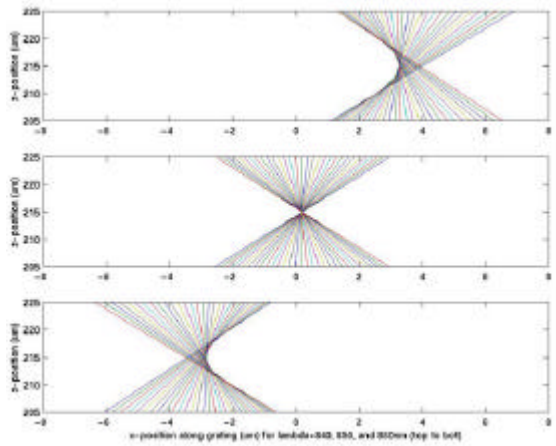


Fig. 2: Ray trace of grating coupler output

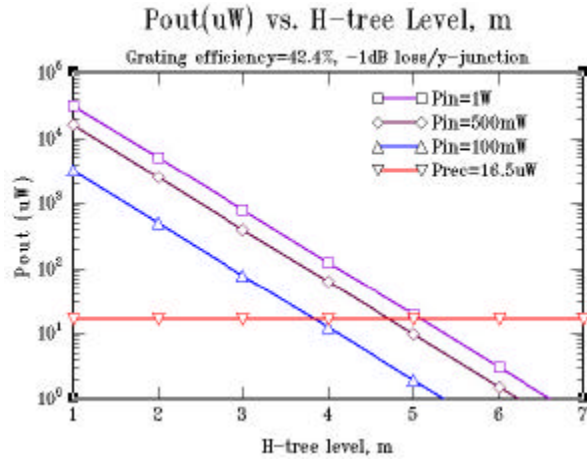


Fig. 3: Optical output power vs. m-level H-tree

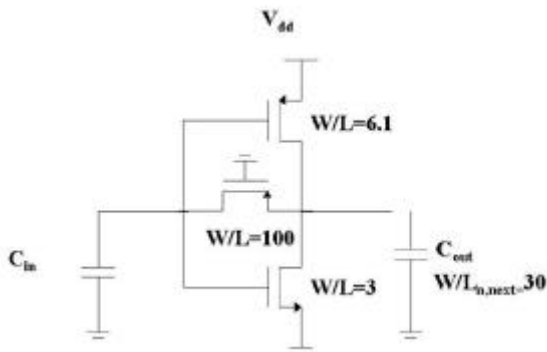


Fig 4: Assumed transimpedance topology of monolithic receivers

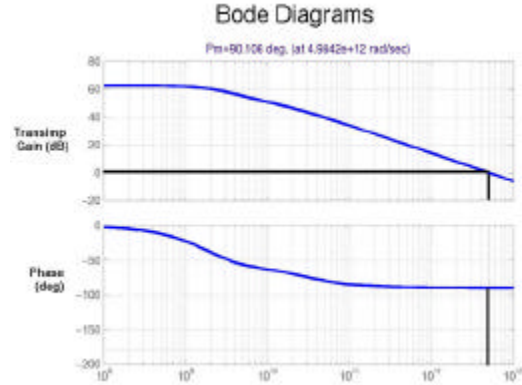


Fig. 5: Gain, stability estimations for transimpedance receiver

Cover index, n_c	1
Substrate index, n_s	1.4
Waveguide index, n_w	1.5
Effective index, N	1.41
Grating thickness, t_g (μm)	0.27
Waveguide thickness, t_w (μm)	0.35
Max grating period, Λ (μm)	0.84
Min grating period, Λ (μm)	0.47
Coupler Length, L (μm)	150
Focal Point (μm)	($x = 0, z = 215$)
Grating Efficiency (%)	42.4

Table 1: Grating Design Summary

Lateral placement variations	$\pm 5\mu\text{m}$
Horizontal placement variations	$\pm 10\mu\text{m}$
Min detector diameter (μm)	$13 \pm 5 = 23\mu\text{m}$
C_{detector} (fF)	100
Detector efficiency, η (%)	25
Responsivity, R (A/W)	0.17
I_{noise} (dark + substrate) (nA)	3
Wavelength, λ (μm)	0.85
Extinction coefficient, r_{ex} (%)	25
Bit rate, B (Gb/s)	10
Bit error rate (BER)	10^{-15}
Laser-to-Waveguide Coupling Loss	-3dB
Loss per Y-junction	-1dB
Air/Dielectric Reflection Loss	-0.2dB
#Nodes/ m^{th} level, H-tree	2^{2m}
Level H-tree	5
# Nodes, H-tree	1024

Table 2: Optical System Summary

F (nm)	50
V_t (V)	0.26
V_{dd} (V)	0.55
$t_{\text{ox, effective}}$ (\AA)	8
Chip size (cm^2)	13
Gate delays/CP*	5
CP gate fan-in	2
CP gate fan-out	3
$N_{\text{gates}} \times 10^6$ (total)	177.5
$N_{\text{gates}} \times 10^3$ (node)	106.3
Activity factor, a	.094
# Nodes, Total	1024
*CP= critical path	

Table 3: 50nm Technology Node Summary