

17.6 Impact of Die-to-Die and Within-Die Parameter Fluctuations on the Maximum Clock Frequency Distribution

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A processor maximum clock frequency (FMAX) distribution is significantly influenced by the magnitude of critical path delay deviations resulting from both die-to-die (inter-die) and within-die (intra-die) fluctuations. FMAX is a measurement performed at wafer sort in which each functional die is tested for its maximum operating clock frequency. Die-to-die fluctuations resulting from lot-to-lot, wafer-to-wafer and some sources of the within-wafer variations affect every element on a chip equally. Conversely, within-die fluctuations consisting of both random and systematic components produce a non-uniformity of electrical characteristics across the chip [1].

The FMAX distribution model is based upon statistical simulations of critical paths for a 0.25µm Pentium®-family processor. Die-to-die (D2D) fluctuations are simulated using statistical process files that incorporate D2D variations. Within-die (WID) fluctuations are analyzed using a WID circuit simulator along with 0.25µm WID variation models. Figure 17.6.1 summarizes the statistical simulations of three critical paths by providing the mean delay ($\mu_{T_{cp}}$) and the ratio of the standard deviation to the mean delay ($\sigma_{T_{cp}}/\mu_{T_{cp}}$) corresponding to D2D and WID fluctuations. The mean critical path delays are different for the three simulated paths, since some circuits require execution in less than one clock cycle. The nominal mean critical path delay ($T_{cp,nom}$) is assumed equal to the longest path delay. The nominal critical path standard deviation ($\sigma_{T_{cp,nom}}$) is calculated by averaging the ratio of the standard deviation to mean path delay for all three simulated paths.

The impact of WID fluctuations on one critical path is modeled as a normal distribution using the nominal mean and standard deviation provided in Figure 17.6.1. The probability of one critical path satisfying a specified maximum delay (t_{max}) is calculated as:

$$P_{WID-T_{cp,nom}}(t \leq t_{max}) = F_{WID-T_{cp,nom}}(t_{max}) = \int_0^{t_{max}} f_{WID-T_{cp,nom}}(t) dt, \quad (1)$$

where t is the variable critical path delay. $F_{WID-T_{cp,nom}}$ and $f_{WID-T_{cp,nom}}$ are the WID cumulative and density functions, respectively, for one critical path. A chip, however, contains many critical paths, all of which must satisfy the worst case delay constraint [2-4]. The paths may be completely dependent (correlation=1), independent (correlation=0) or some correlation between 0 and 1. If two paths are completely dependent, only one distribution is required to model the worst-case delay for both paths. If two paths, however, are not completely dependent, both paths must be statistically combined to obtain the worst-case delay. Assuming a number (N_{cp}) of independent critical paths for the entire chip [4], the probability of satisfying t_{max} is:

$$P_{WID}(t \leq t_{max}) = F_{WID}(t_{max}) = (F_{WID-T_{cp,nom}}(t_{max}))^{N_{cp}}, \quad (2)$$

where F_{WID} is the chip WID cumulative distribution. The chip WID maximum critical path delay density function is then calculated by taking the derivative of (2) with respect to t_{max} as:

$$f_{WID}(t_{max}) = N_{cp} f_{WID-T_{cp,nom}}(t_{max}) (F_{WID-T_{cp,nom}}(t_{max}))^{N_{cp}-1}. \quad (3)$$

Figure 17.6.2 illustrates the dependence of the WID maximum critical path delay density function (3) on N_{cp} . As N_{cp} increases, the mean delay increases and the standard deviation decreases. Since the slowest critical path limits the chip overall performance, the probability of a longer cycle time increases as N_{cp} increases. For example, when only one path is considered, the probability of a delay less than $T_{cp,nom}$ is equal to 0.5. When two independent critical paths are considered, the probability that the delay is less than $T_{cp,nom}$ is $(0.5)^2=0.25$. Notice, however, that increasing N_{cp} from 1 to 10 has a greater impact

on the mean and variance of the WID distribution than increasing N_{cp} from 10^1 to 10^2 , thus elucidating the decreasing dependence of the WID distribution on N_{cp} as N_{cp} increases to relatively large values.

The impact of both D2D and WID fluctuations on the chip maximum critical path delay distribution is analyzed by combining the individual D2D and WID distributions. Shifting the D2D and WID distributions by $-T_{cp,nom}$, the resulting distributions ($f_{\Delta T_{D2D}}$ and $f_{\Delta T_{WID}}$) represent the deviations in delay from $T_{cp,nom}$. Assuming $f_{\Delta T_{D2D}}$ and $f_{\Delta T_{WID}}$ are independent, the maximum critical path delay is calculated as:

$$T_{cp,max} = T_{cp,nom} + \Delta T_{D2D} + \Delta T_{WID}, \quad (4)$$

where ΔT_{D2D} and ΔT_{WID} are the deviations in the nominal critical path delay due to D2D and WID fluctuations, respectively. The maximum critical path delay density function resulting from both D2D and WID fluctuations is then calculated from a convolution,

$$f_{T_{cp,max}} = f_{T_{cp,nom}} * f_{\Delta T_{D2D}} * f_{\Delta T_{WID}}, \quad (5)$$

where $f_{T_{cp,nom}}$ is an impulse at $T_{cp,nom}$.

Figure 17.6.2 also plots the D2D critical path delay distribution. Notice as N_{cp} increases the WID distribution approaches an impulse function with an increasing mean delay. As the D2D and WID distributions are statistically combined through (5), the resulting distribution has a mean equal to that of the WID distribution and a variance resulting predominantly from the D2D distribution. Thus, WID fluctuations determine the mean of the maximum critical path delay distribution, and D2D fluctuations determine the variance.

The combined distribution in (5) is now mapped to a frequency distribution. The maximum clock frequency is calculated as:

$$F_{clk,max} = \frac{b}{T_{cp,max}}, \quad (6)$$

where b is the clock skew factor ($b=0.9$, assumes 10% clock skew). Figure 17.6.3 illustrates the mapping of $f_{T_{cp,max}}$ to the maximum clock frequency density function ($f_{F_{clk,max}}$). The probability that the maximum critical path delay is within some interval $t_0 \leq t \leq t_1$ is equal to the probability that the maximum clock frequency is within the interval $b/t_1 \leq F_{clk} \leq b/t_0$. As $t_1 - t_0$ approaches zero, the maximum clock frequency density function is derived as:

$$f_{F_{clk,max}}(b/t) = f_{T_{cp,max}}(t) \frac{t^2}{b}. \quad (7)$$

Figure 17.6.4a compares the FMAX distribution model, described in (1), (3), (5) and (7), for both D2D and WID fluctuations with $N_{cp}=100$ against the FMAX measured data obtained at wafer sort for a Pentium®-family microprocessor. The predicted FMAX distribution agrees closely with the distribution of measured data in mean, variance and shape. Figure 17.6.4b validates the model with measured data for the cumulative FMAX distribution. Figure 17.6.5 plots the distributions resulting from only D2D and only WID fluctuations to illustrate their individual effects on the FMAX distribution. These results clearly reveal that within-die fluctuations directly impact the FMAX mean and die-to-die fluctuations impact the FMAX variance.

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	Path 1	Path 2	Path 3	Nominal Path
Normalized μ_{TCP}	1.00	0.77	0.51	1.00
D2D: σ_{TCP}/μ_{TCP} (%)	8.63	8.59	9.74	8.99
WID: σ_{TCP}/μ_{TCP} (%)	2.65	3.19	3.32	3.05

Figure 17.6.1: Statistical summary of the die-to-die (D2D) and within-die (WID) fluctuations on three critical paths for an Intel® Pentium® family processor as well as the nominal path.

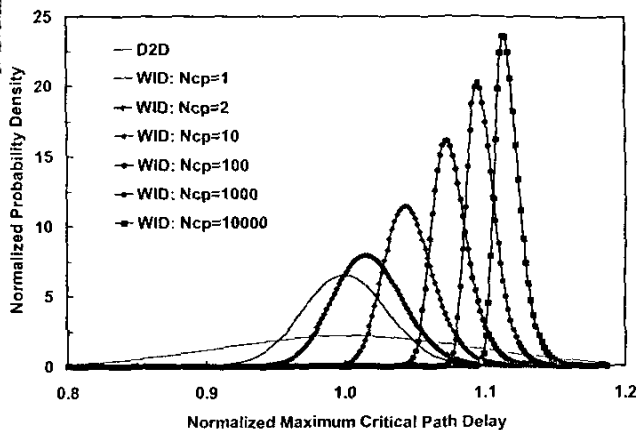


Figure 17.6.2: The within-die (WID) maximum critical path delay distribution for different values of N_{cp} and the die-to-die (D2D) critical path delay distribution.

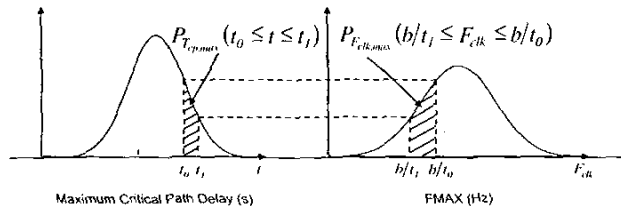


Figure 17.6.3: Mapping the maximum critical path delay distribution to the maximum clock frequency distribution.

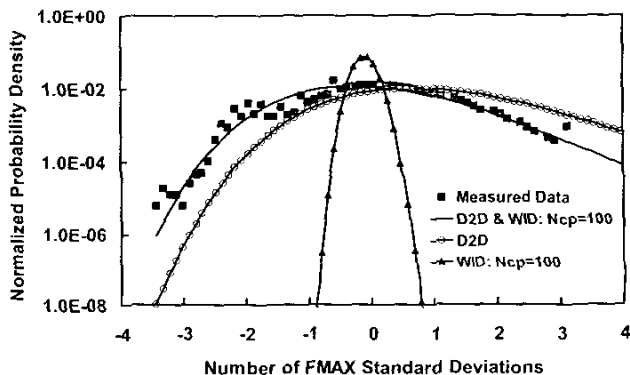


Figure 17.6.5: Individual contributions of die-to-die (D2D) and within-die (WID) fluctuations to the FMAX distribution.

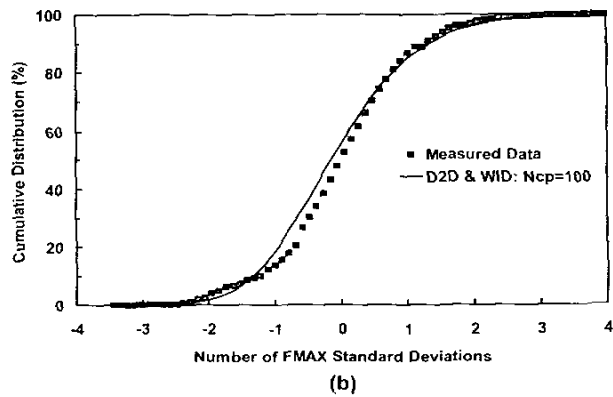
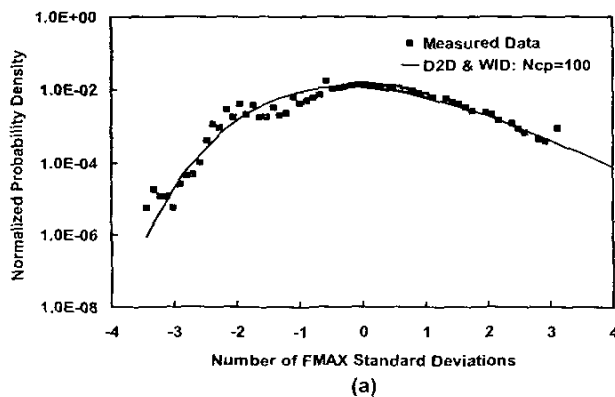


Figure 17.6.4: Comparison of the model projections with measured data for the maximum clock frequency (a) probability density and (b) cumulative distributions.