

# The Limits of System Improvement through Liquid Diagonal Routing of Interconnects

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## ABSTRACT

An interconnect distribution for a system utilizing liquid diagonal routing is rigorously derived. Using the distribution in conjunction with a wiring layer assignment algorithm, the limits of clock frequency and area improvements are quantified as a function of wiring efficiency, the ratio of utilized wiring area to those available. A liquid-routed system with only a 28% wiring efficiency is equivalent to an orthogonally routed system with a 40% wiring efficiency. A wiring efficiency of a liquid-routed system below 28% results in an inferior design in regards to clock frequency and/or required metal resources. If a 40% wiring efficiency is maintained, however, the power-constrained clock frequency can be increased by 38% with a 69% reduction in area, or the power-density-constrained area can be reduced by 75% with a 47% reduction in power. Liquid diagonal routing promises improvements to both area and clock frequency if the wiring efficiency is maintained above roughly 30%.

## I. INTRODUCTION

As device dimensions scale down with each new technology generation, interconnect dimensions must also scale down to achieve higher densities of wiring. In the last decade, this scaling has caused interconnect delay to become a dominant source of total path delay. The increasing dominance of interconnect delay has prompted research into both processing solutions such as copper metallization and low- $k$  dielectrics and design solutions such as repeater insertion and reverse interconnect scaling. Recently, a CAD solution has been proposed in the form of pervasive diagonal routing. Simplex Solutions projects a 20% performance increase and a 10% area reduction from its X Architecture [1],[2]. Whereas interconnects on each metal level in a conventional design are typically constrained to one of the primary compass directions as shown in Figure 1a, the X Architecture makes use of liquid diagonal routing in which there is no preferred direction of routing on a metal level. Liquid-routed interconnects, in the Simplex implementation, can be routed in both primary and secondary compass directions as shown in Figure 1b. In an effort to predict the limits of system improvement through the use of liquid diagonal routing, a new, rigorously derived *a priori* wiring distribution (Section II) is used in conjunction with a wiring layer assignment algorithm (Section III) to project the optimum area and clock frequency for a logic block (Section IV).

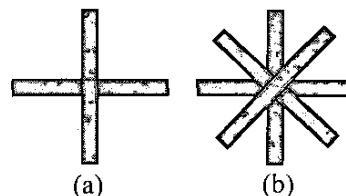


Figure 1. The valid directions of routing in an (a) orthogonal fashion and (b) liquid diagonal fashion.

## II. A PRIORI WIRING DISTRIBUTION FOR LIQUID DIAGONAL ROUTING

As a first step in projecting the performance and area requirements of a generic logic block, an *a priori* interconnect distribution that predicts the number of interconnects per unit length versus the length of interconnect is needed. Figure 2 presents a new interconnect distribution for liquid diagonal routing as derived following a methodology adapted from [3]. Figure 3 is a comparison of the interconnect distributions of conventional orthogonally routed and liquid-routed random logic blocks of 16 million gates with Rent's parameters  $k=4$  and  $p=0.6$ . Length is measured in gate pitches, the average distance between adjacent gates.

$$N(t,d) = 2 - \delta(d) - \theta(t) (n-d)(n-t-d)$$

$$N_{\text{sum}}(t,d) = \begin{cases} (n-t)(n+t) & d=0 \\ n(n-d) & d > 0, d+t \leq \frac{n}{2} \\ n(n-d+t) - 2(d+t) & 0 < d \leq \frac{n}{2}, d+t > \frac{n}{2} \\ 2n(n-2d) + 2(d-t)(d+t) & d > \frac{n}{2} \end{cases}$$

$$N_s(t,d) = t$$

$$N_g(t,d) = \sum_{t'=\frac{t-d}{2}, t'+d=t} N_s(t',d)$$

$$N_c(t,d) = \frac{N(t,d)}{N_{\text{sum}}(t,d)}$$

$$i_s(t,d) = \text{abs} N_{\text{sum}}(t,d) \left[ \begin{array}{l} (N_s(t,d) + N_c(t,d))^k - (N_s(t,d))^k \\ (N_s(t,d) + N_g(t,d))^k \\ -(N_s(t,d) + N_g(t,d) + N_c(t,d))^k \end{array} \right]$$

$$i_t(t) = t + \sqrt{2}d = i_s(t,d)$$

$M$	Number of gate pairs
$N_{\text{sum}}$	Number of starting gates (center of a gate pair)
$N_A, N_B, N_C$	Number of gates in blocks A, B, and C
$h$	Interconnect density function
$n$	Number of gates along chip edge
$t$	Orthogonal length of an interconnect
$d$	Diagonal length of an interconnect
$\alpha$	Parout conversion factor
$k$	Rent's coefficient
$p$	Rent's exponent
$l$	Interconnect length

Figure 2. The complete interconnect distribution for a liquid-routed system.

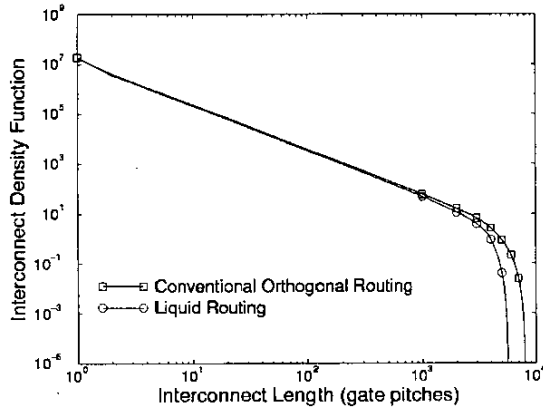


Figure 3. Comparison of interconnect distributions for orthogonally routed and liquid-routed systems of 16 million gates.

### III. WIRING LAYER ASSIGNMENT ALGORITHM

A wiring layer assignment algorithm is required to determine the number of metal levels needed for a design with a given area and clock frequency. In such an algorithm, the interconnect pitch of each pair of metal levels is determined such that (1) the available wiring resources of the levels are consumed and (2) all signal interconnects on those levels meet a delay constraint set by the clock frequency. The pitch of a pair of metal levels is the sum of the signal interconnect width  $w$  and dielectric spacing  $s$  as shown in the cross-sectional view in Figure 4. In the algorithm from [4], the pitch for each metal level is determined by simultaneously solving two constraint equations. The first ensures that the first condition above is met and is expressed as

$$2e_w A_m = \chi p_n \sqrt{\frac{A_m}{N_t}} \int_{L_{n-1}}^{L_n} li(l) dl \quad (1)$$

where  $e_w$  is the wiring efficiency,  $\chi$  is the point-to-point conversion factor,  $p_n$  is the pitch of the  $n^{\text{th}}$  tier defined as the width of an interconnect plus the spacing to an adjacent interconnect,  $N_t$  is the total number of gates, and  $L_n$  is the length of the longest interconnect on the  $n^{\text{th}}$  tier. The equation for the second condition relates the time delay to a fraction  $\beta$  of the clock cycle ( $1/f_c$ ) as

$$\frac{\beta}{f_c} = \frac{4.4 \rho \epsilon_r \epsilon_0 k_{int}}{p_n^2} \frac{A_m}{N_t} L_n^2 \quad (2)$$

where  $\rho$  is the resistivity,  $\epsilon_r$  is the relative permittivity,  $\epsilon_0$  is the permittivity of free space, and the product  $\epsilon_r \epsilon_0 k_{int}$  is the line capacitance per unit length [5].

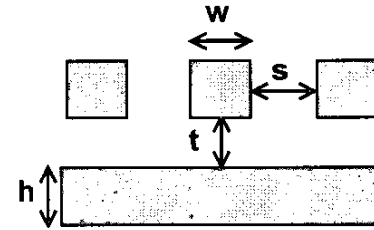


Figure 4. Cross-sectional view of a pair of metal levels with height  $h$ , width  $w$ , spacing  $s$ , and dielectric thickness  $t$ . The pitch is the width plus the spacing.

Under a clock frequency constraint, Eqs. (1) and (2) are simultaneously solved for each pair of metal levels to determine the number of metal levels needed as a function of area. The case study here is for the system of Figure 3 with eight metal levels,  $f_c=1.3$  GHz,  $\rho=1.68 \mu\Omega\cdot\text{cm}$ ,  $\epsilon_r=2.0$ , and  $k_{int}=6.2$  at the 100 nm technology node. Figure 5 plots the resulting functions for the system routed orthogonally with a wiring efficiency of 40% as well as using liquid diagonal routing with various wiring efficiencies. The wiring efficiency is the ratio of utilized wiring area to those available. With the potential added complexity in diagonal routing algorithms, the wiring efficiency may be negatively impacted for such designs. The orthogonal system only meets the restrictions on the number of metal levels at an area greater than  $1.3 \text{ cm}^2$  (Design A). As shown in Figure 5, the curve for liquid diagonal routing with a wiring efficiency of 28% nearly matches that of the orthogonally routed case. If the wiring efficiency decreases beyond that mark (e.g., 20%), the system requires more metal levels than the orthogonal Design A, and no system improvement is achieved. If the wiring efficiency is maintained at 40%, however, the liquid-routed system offers great potential benefits. For instance, the wiring requirements can be decreased by reducing the number of metal levels to six and reducing the area by 10% (Design B).

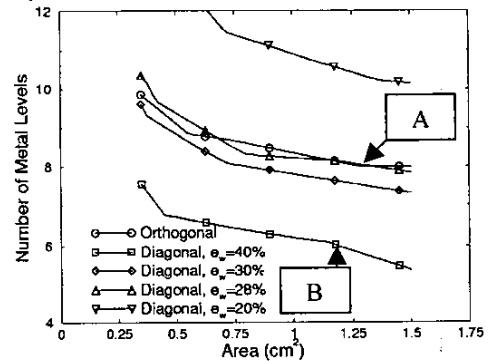


Figure 5. The number of metal levels needed versus area for the orthogonal design ( $e_w=0.4$ ) and several liquid-routed systems.

### IV. OPTIMIZATION RESULTS

To maintain design constraints for a clock frequency optimization, the maximum power of the system is

constrained to that projected for Design A of Figure 5. The total dynamic power ( $P_{total}$ ) is calculated as

$$P_{total} = P_{int} + P_{logic} \quad (3)$$

where  $P_{int}$  and  $P_{logic}$  are the cumulative interconnect and logic gate powers, respectively. The logic power is found as

$$P_{logic} = \frac{a}{2} N_i w_k C_{go} V_{dd}^2 f_c \quad (4)$$

where  $a(=0.10)$  is the activity factor,  $w_k$  is the nFET width in feature sizes,  $C_{go}$  is the gate overlap, junction, and fan-out capacitance for a minimum-sized gate, and  $V_{dd}$  is the supply voltage [4]. The interconnect power is found as

$$P_{int} = \frac{a}{2} \epsilon_r \epsilon_o k_{int} L_{total} \sqrt{\frac{A_m}{N_i}} V_{dd}^2 f_c \quad (5)$$

where  $L_{total}$  is the total length of interconnects in gate pitches. For Design A,  $P_{total}=18.2$  W. Constraining the maximum power dissipation to this value, the maximum clock frequency for the liquid-routed system with a maximum of  $1.3 \text{ cm}^2$  and eight metal levels is plotted in Figure 6 as a function of wiring efficiency. At a wiring efficiency of 28%, the clock frequency is 1.3 GHz; below 28%, the clock frequency is decreased by use of liquid diagonal routing. If the wiring efficiency is maintained at 40%, the clock frequency can be increased by 38% to 1.8 GHz. In addition, as shown in Figure 7, the area can simultaneously be decreased to  $0.4 \text{ cm}^2$  – a 69% reduction. The number of metal levels, however, cannot be reduced significantly.

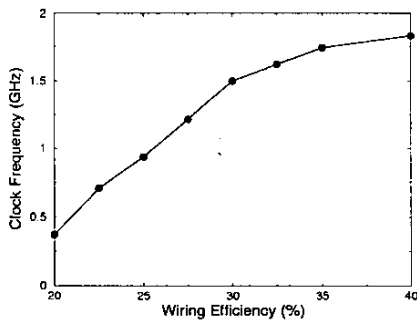


Figure 6. Maximum clock frequency using liquid diagonal routing versus wiring efficiency.

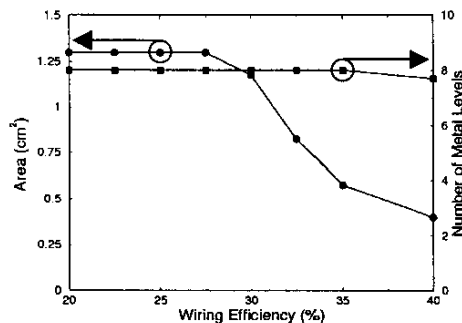


Figure 7. Frequency-optimized area and number of metal levels using liquid diagonal routing versus wiring efficiency.

Constraining the designs further to a power density limitation of  $30 \text{ W/cm}^2$ , the minimum area for a system with a 1.3 GHz clock frequency and eight metal levels is found as a function of wiring efficiency as plotted in Figure 8. Once again, at the break-even wiring efficiency of 28%, the area is equivalent to that of the orthogonal base case at  $1.3 \text{ cm}^2$ ; below 28%, such designs are not achievable. At a wiring efficiency of 40%, however, the minimum area is  $0.32 \text{ cm}^2$  – a 75% reduction. In addition, this is a low-power design only consuming 9.6 W.

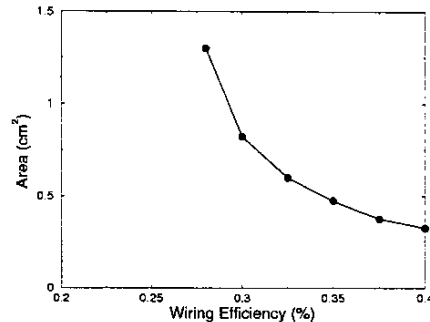


Figure 8. Minimum area using liquid diagonal routing versus wiring efficiency.

## V. CONCLUSIONS

An interconnect distribution for a system utilizing liquid diagonal routing has been rigorously derived. Using the distribution in conjunction with a wiring layer assignment algorithm, the limits of clock frequency and area improvements have been quantified as a function of wiring efficiency. A liquid-routed system with only a 28% wiring efficiency is equivalent to an orthogonally routed system with a 40% wiring efficiency. If the wiring efficiency of the liquid-routed system drops below 28%, the system is inferior to its orthogonally routed counterpart in clock frequency and/or required, metal resources. If a 40% wiring efficiency is maintained, however, the power-constrained clock frequency can be increased by 38% with a 69% reduction in area, or the power-density-constrained area can be reduced by 75% with a 47% reduction in power. Liquid diagonal routing provides significant benefits to both area and clock frequency if the wiring efficiency remains above roughly 30%.

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