A Three-Dimensional Stochastic Wire-Length Distribution for Variable Separation of Strata

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Abstract†

A complete wire-length distribution for future three-dimensional, homogeneous gigascale integrated (GSI) architectures with *variable vertical separation of strata* is derived. Because stratal pitch was not found to impact the wire-length distribution significantly, bonded three-dimensional implementations which are technologically feasible can be used to obtain large increases in global clock frequencies. The longest interconnect can be reduced by 30% through the introduction of a single additional stratum. A 93% reduction in the length of the longest interconnect can be obtained through the optimal use of a three-dimensional architecture for a 100 nm ASIC, potentially leading to a 15.8 times increase in global clock frequency.

I. Introduction

The wiring requirements of a GSI system have recently come to be the dominant limiting factor for performance and productivity [1–3]. To understand the impact that these requirements have on clock frequency, power consumption, and chip size, it is necessary to first quantify the wiring demand [4]. Wire-length distributions have previously been derived for traditional two-dimensional architectures and have met with success [4,5] when compared to data from real designs.

With the advent of SOI technology, the prospect of three-dimensional architectures with vertical interconnects connecting multiple levels of transistors has become a foreseeable advancement in high performance GSI microelectronics [6]. After [6], a stratum is defined as a single layer of transistors with its corresponding metal levels. In general, the distance between two adjacent strata, the stratal pitch, may differ from the gate pitch within a stratum as in the structure of Fig. 1. Efforts have been reported previously to describe the wire-length distribution for such a three-dimensional system for a stratal pitch equal to the gate pitch [7, 8].

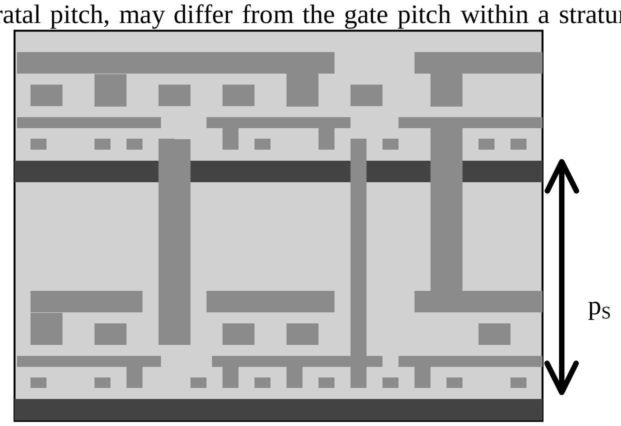

Fig. 1. Cross-section of a three-dimensional architecture of two strata showing the two active layers separated by a variable stratal pitch p_S.

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In Section II, a new wire-length model is derived for three-dimensional architectures with unequal stratal and gate pitches based upon the method outlined by in [4]. In Section III, results of simulations using the new model are presented and explained. Concluding remarks are made in Section IV.

II. Derivation of Model

To predict the wiring requirements for three-dimensional GSI systems, an interconnect density function is derived as the product of two terms. The first term $M_t[\ell]$ gives the number of gate pairs which are separated by a given length ℓ. The second term $I_{exp}[\ell]$ is the number of expected interconnects connecting a gate pair separated by a length ℓ.

The number of gate pairs separated by ℓ gate pitches in a single stratum is given in [4] as

$$M_S[\ell] = \begin{Bmatrix} \ell^3 - 2\ell^2\sqrt{N_S} + \frac{1}{3}\ell(6N_S - 1), & 1 \le \ell < \sqrt{N_S} \\ \begin{bmatrix} -\frac{\ell^3}{3} + 2\ell^2\sqrt{N_S} - \frac{1}{3}\ell(12N_S - 1) \\ + \frac{2}{3}\sqrt{N_S}\left(2\sqrt{N_S} - 1\right)\left(2\sqrt{N_S} + 1\right) \end{bmatrix}, & \sqrt{N_S} \le \ell < 2\sqrt{N_S} \end{Bmatrix} \quad (1)$$

where N_S is the number of gates in the stratum. By inspection, the number of stratal pairs in a three-dimensional system separated by v stratal pitches is

$$M_z[v] = 2(S - v)u[S - v]u[v] - S\delta[v] \quad (2)$$

where S is the number of strata and $u[x]$ and $\delta[x]$ are the discrete unit step and impulse functions, respectively. The number of gate pairs separated by v stratal pitches vertically and a total ℓ gate pitches can be written as

$$M_{tz}[\ell, v] = \frac{M_z[\ell]}{1 + u[\ell / r]} \cdot M_S[\ell - vr] \quad (3)$$

where r is the stratal-to-gate-pitch ratio. From this, the total number of gate pairs in a three-dimensional system can be found through the evaluation of

$$M_t[\ell] = \sum_{v=0}^{S-1} M_{tz}[\ell, v]. \quad (4)$$

The number of expected interconnects can be found by use of the well-established empirical relationship known as Rent's Rule [9]. This relationship predicts the number of signal I/O terminals T in terms of the number of gates N in a random logic network. This relationship is a simple power law expression

$$T = kN^p \quad (5)$$

where k and p are empirical parameters.

Combination of the conservation of terminals and Rent's Rule yields an expression for the number of interconnects between two gates in blocks of gates A and C separated by a third block B,

$$I_{exp}[\ell] = \frac{\alpha k}{N_A N_C[\ell]}\begin{bmatrix}\left(N_A + N_B[\ell]\right)^p + \left(N_B[\ell] + N_C[\ell]\right)^p \\ -\left(N_B[\ell]\right)^p - \left(N_A + N_B[\ell] + N_C[\ell]\right)^p\end{bmatrix} \quad (6)$$

where α is a fanout factor and N_X represents the number of gates in a block X [4]. To find the expected number of interconnects separated by a length ℓ, N_A is considered as a single gate. N_C represents the average number of gates on the periphery of a manhattan semisphere of radius ℓ and can be expressed as

$$N_C[\ell] = \frac{M_t[\ell]}{N_{start}[\ell]} \quad (7)$$

where $N_{start}[\ell]$ is the number of gates in the system that can serve as the center of a semisphere. N_B can then be expressed as a summation over N_C

$$N_B[\ell] = \sum_{\ell'=1}^{\ell-1} N_C[\ell']. \quad (8)$$

III. Results

The new model that projects the wire-length distribution for three-dimensional GSI systems is

$$I_{idf}[\ell] = M_t[\ell] \cdot I_{exp}[\ell] \quad (9)$$

where $M_t[\ell]$ is given by (4) and $I_{exp}[\ell]$ is given by (6). Fig. 2 compares the new model for a one-stratum or two-dimensional system with the two-dimensional model given in [4]. For all simulations, the system consists of 4 million gates, Rent's exponent p is 0.6, and the fanout-Rent's coefficient product αk is 3. The two distributions show good agreement but exhibit a slight deviation for long interconnects because the previous distribution assumes an infinite plane of gates in the calculation of N_C [4] while the new model takes the average of possible values of N_C over the whole system.

As the number of dimensions of the system is increased, the lengths of the longest interconnects are reduced greatly as shown in Fig. 3. This reduction results from both shorter corner-to-corner distances and from each gate's having more neighboring gates. The shortest interconnects are not significantly impacted. Similarly, as the number of strata is increased in a three-dimensional architecture, the longest interconnects are reduced in length by at least 30% as illustrated in Fig. 4. The large shift exhibited in the global region of the curves in Figs. 3 and 4 is balanced out by a small percentage increase in density in the local region such that the total number of interconnects is exactly conserved. As demonstrated in Fig. 5, increasing the stratal-to-gate-pitch ratio r does not impact the distribution as significantly as a change in the number of strata S.

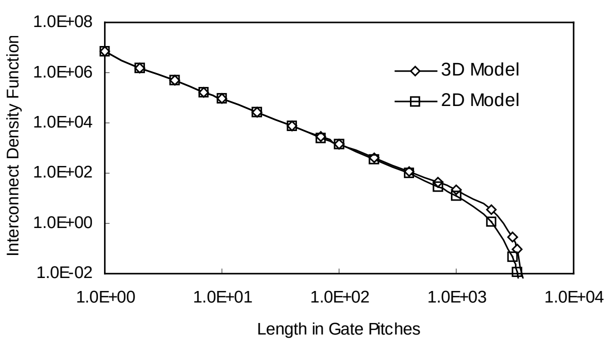

Fig 2. Comparison of new model to previous 2D model [4] for a one-stratum system.

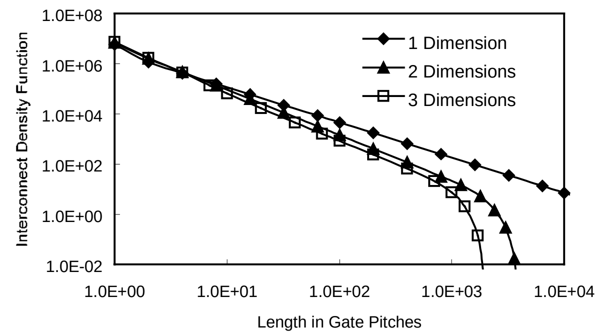

Fig. 3. Interconnect distributions for one-, two-, and three-dimensional architectures.

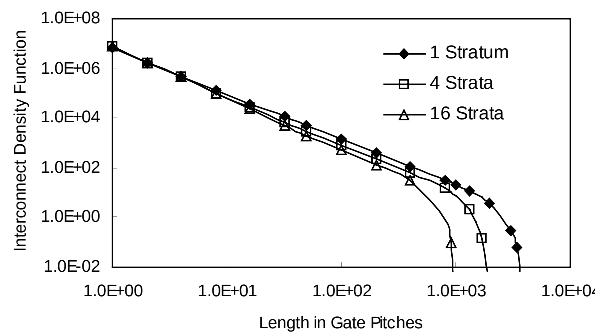

Fig. 4. Interconnect distributions as the number of strata is varied.

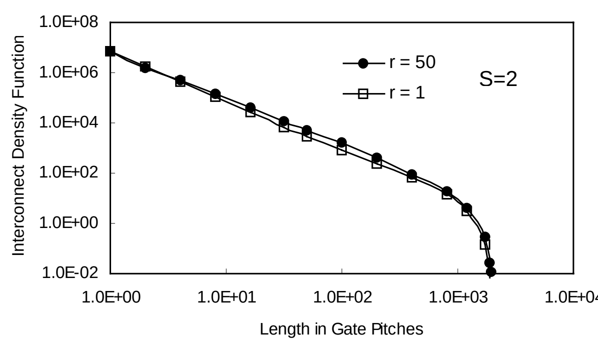

Fig. 5. Interconnect distributions as r is changed. r is the ratio of vertical separation to the gate pitch.

Fig. 6 shows the impact of increasing the number of strata on the length of the longest and average interconnects. The average interconnect length is reduced by at least 20% as the first few strata are added, but the returns quickly diminish as the reduction saturates at 45%. The longest interconnect, however, receives a greater reduction of at least 30% that does not diminish as quickly with respect to an increase in S. The longest interconnect is compared to the corner-to-corner distance of the system. This distance is given as

$$\ell_{cc} = 2\left(\sqrt{\frac{N_T}{S}} - 1\right) + r(S-1) \qquad (10)$$

where N_T is the total number of gates in the system. The longest interconnect follows the same trend as the corner-to-corner distance. If the system is sufficiently large such that $r << N_S$, the corner-to-corner distance, and thus the longest interconnect, can be reduced in length by 30% by adding only one stratum to a traditional two-dimensional architecture. This 30% reduction that decreases interconnect delay and allows for clock frequency increase [10] is calculated only in units of gate pitches. As three-dimensional architectures can allow a much higher interconnect density, the gate pitch may also be reduced in a wire-limited system, compounding this gain to an even greater reduction in units of absolute length and a further increase in clock frequency.

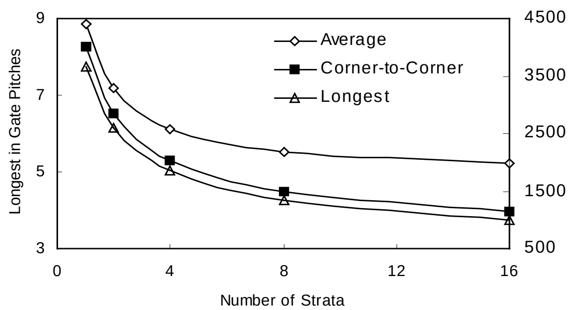

Fig. 6. Lengths of longest and average interconnects vs. number of strata for r = 5.

The corner-to-corner distance can be minimized if the number of strata is increased to

$$S_{opt} = \sqrt[3]{\frac{N_T}{r^2}}\,. \qquad (11)$$

Substituting (11) into (10), the minimum corner-to-corner distance can be expressed as

$$\ell_{cc,min} = \frac{1.5}{\sqrt[6]{N_T r}}\,\ell_{cc,2D} \qquad (12)$$

where $\ell_{cc,2D}$ is the corner-to-corner distance in a two-dimensional system. For a 2005 100 nm ASIC with a maximum 173.3 million gates [11] and r=1, the longest interconnect length is reduced by 93% leading to a possible 15.8 times increase in global clock frequency.

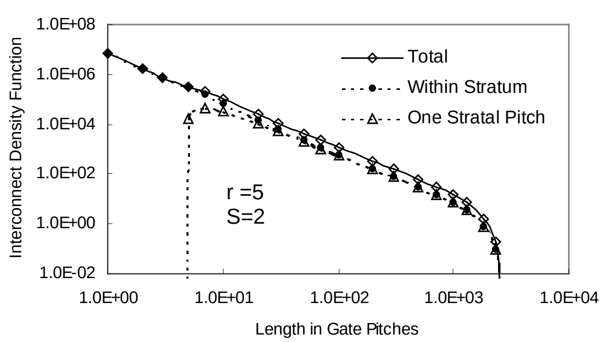

Fig. 7. Interconnect distribution resolved into vertical components.

The interconnect density function can be resolved into component distributions for interconnects that span a given number of stratal pitches. Fig. 7 shows the results of this for a two-strata system with r=5. For all interconnect lengths, fewer interconnects run vertically by one stratal pitch than are contained completely within one stratum. Comparisons of vertical interconnect requirements for different numbers of strata with the same parameters as above are given in Fig. 8. Since a very small percentage of interconnects have vertical components, consumption of transistor area in the construction of vias through the active layers can be kept to a minimum.

Vertical Distance	**Number of Strata in System**		
	1 Stratum	2 Strata	4 Strata
Within Stratum	1.20E+07	1.13E+07	1.11E+07
One Stratal Pitch	___	6.30E+05	6.73E+05
Two Stratal Pitches	___	___	1.59E+05
Three Stratal Pitches	___	___	4.62E+04
Total Number	1.20E+07	1.20E+07	1.20E+07

Fig. 8. Number of interconnects.

IV. Conclusions

A new model that projects wire-length distributions for two- and three-dimensional GSI systems has been derived that includes the impact of the stratal pitch on interconnect probability. The model holds good agreement with a previous two-dimensional model that has been shown to agree with experimental data. Results of the model have shown that the addition of a single stratum can lead to at least a 30% reduction in the longest interconnect length. Furthermore, three-dimensional architectures can lead to such significant increases in clock frequency as 15.8 times for a 100 nm ASIC. For a typical system, less than 10% of the total interconnects have vertical components. Because stratal pitch was not found to impact the wire-length distribution significantly, bonded three-dimensional implementations which are technologically feasible can be used to obtain large increases in global clock frequencies.

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