Sea of Leads Microwave Characterization and Process Integration with FEOL & BEOL

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Abstract — Complete front-end-of-the-line (FEOL), back-end-of-the-line (BEOL), and Sea of Leads (SoL) process integration is reported with the end result being fully packaged CMOS dice at wafer-level. In addition, SoL microwave characterization in the 0.1-45GHz frequency range demonstrates that the insertion-loss decreases with increasing lead thickness and decreasing lead length. Worst case insertion-loss for signal path into- and out- of the package was measured at wafer-level to be 1.15dB at 45GHz. Crosstalk between parallel leads was approximately –30dB at 45GHz. Finally, the fabrication of a high-density substrate for SoL using low cost multi-crystalline Si is reported.

I. Introduction

The fabrication process of a Sea of Leads (SoL) package with embedded air-gaps has been demonstrated [1]. This paper presents recent advances in SoL packaging technology by first describing SoL process integration with an in-house CMOS process. The end result is the concurrent packaging of dice across a wafer with SoL rendering the wafer ready for wafer-level testing and burn-in. In addition, SoL is electrically characterized with thru-line and crosstalk measurements in the 0.1-45GHz frequency range using a network analyzer. While high-density organic substrates have been demonstrated, a high-density substrate using low cost multi-crystalline Si is fabricated as a potential alternative.

II. SoL Process Integration with FEOL and BEOL

SoL has been successfully process integrated with a CMOS FEOL and Al BEOL process. Fig. 1 is a chip micrograph illustrating a fully packaged CMOS die at wafer-level. Since O_2 rich plasma process is used to etch vias in the package polymer layer, Al_2O_3 is formed on the Al pads. Consequently, the use of an Ar plasma to remove Al_2O_3 potentially causes polymer sputtering onto the pads, which is reminiscent of the deposition of interlayer dielectric SiO_2 into interconnect vias during Ar sputter cleaning of vias in multi-level interconnects [2]. Instead, dilute HF solution was used to remove the oxide growth with no side effects if nitride/polymer chip passivation is used. Following this process step, the compliant interconnects are electroplated following seed layer deposition. Another critical issue in via fabrication using a plasma process is the ability to selectively etch the polymer's etch mask once the vias are fabricated.

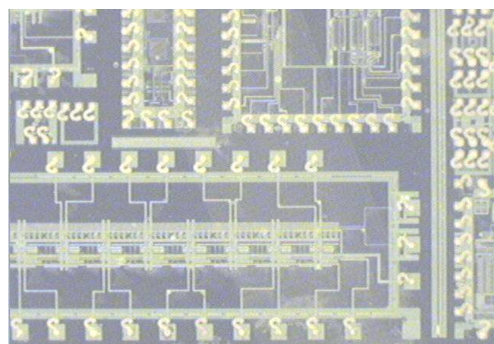
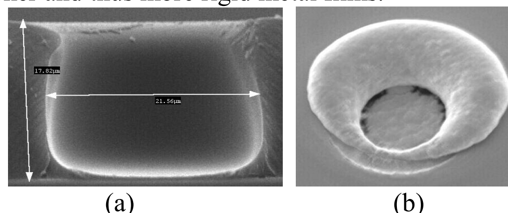


Fig. 1: For clarity, the above micrograph shows only a portion of a fully packaged CMOS die with SoL at wafer-level. The bright S-like structures are the compliant leads that would interconnect the die pads to their respective pads on the substrate once the wafer is diced and the packages are flip-chip mounted. No underfill is required because of the compliant leads.

While photo-definable polymers could potentially eliminate some of the concerns just mentioned, controlling via sidewall angle is more difficult [3]. Fig. 2a is an SEM micrograph illustrating the sharp sidewall profile of a photo-defined via with an approximate height/width aspect ratio of 18µm/20µm and Fig. 2b is the resulting Cu electroplating in a via of that structure. While the polymer's contrast curve can be controlled to yield desirable sidewall angle, plasma processing offers greater control of via sidewall angle. For example, Fig. 3 is an SEM micrograph of via fabricated using RIE where the initial pressure set point was decreased midway through the process yielding a via with a sidewall angle that is high at the via's neck and low at the via's knee. This is significant because it enhances plating uniformity (i.e., increases thickness) at the via's neck thereby potentially minimizing reliability concerns in that area due to the plating of thicker and thus more rigid metal films.



(a) (b)

Fig. 2: (a) SEM micrograph of a photo-defined via illustrating the sharp via sidewall angle. The polynorbornene polymer described in [4] was used for this experiment. Higher energy dosage during photo-definition increased the kink at the via's neck. (b) Using a 300Å/2000Å Ti/Cu seed layer, Cu was plated in a via of similar structure to that shown in Fig. 2a. The SEM micrograph vividly illustrates the poor and unreliable sidewall plating.

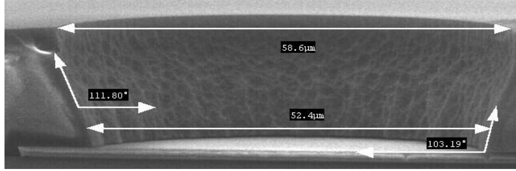


Fig. 3: SEM micrograph illustrating via sidewall profile as a result of RIE. The initial pressure set point of 300mtorr was decreased midway in the process to 200mtorr to yield a via that attains higher sidewall angle at the via's neck and lower sidewall angle at the via's knee. The benefits of such a via structure include enhanced via sidewall plating as well as reduced undercutting at the via's knee, which could cause the polymer to delaminate and prevent seed layer continuity.

III. SoL Microwave Measurements

Using an HP8510C network analyzer and 150µm coplanar ground-signal-ground (GSG) probes, the SoL package shown in Fig. 4 was characterized in the 0.1-45GHz frequency range with a series of thru-line and crosstalk measurements. First, in order to characterize the compliant interconnects alone, three samples were prepared consisting of different Au and Ni plated lead thicknesses on a 15µm thick polymer. The return-loss and insertion-loss of the leads as a function of thickness and metal are plotted in Fig. 5. It is seen that the insertion-loss of the 8µm thick Ni leads is comparable to that of the 1.5µm thick Au leads which can be attributed to the lower conductivity of Ni. The significance of the above measurements becomes clear when it is noted that lead thickness is an important parameter that influences the attainable lead compliance at a given force load. Moreover, the leads can be made mechanically harder, when desirable, by plating them from different metal layers such as Au/Ni/Au while maintaining the leads' resistance to corrosion. Thus, the above measurements indicate potential trade-offs between electrical and mechanical performance. The normalized impedance of the 7.5µm thick Au leads versus frequency as seen by the microwave probes is plotted on a Smith chart in Fig. 6. The final thru-line measurement was made on a fully processed package where the leads were connected in pairs by a 1µm thick copper interconnect on the wafer's surface (beneath the package polymer layer and above the wafer's passivation layer). Fig. 7 is a plot of the return-loss and insertion-loss of a pair of large and small interconnected leads. Crosstalk between adjacent parallel leads was measured to be less than -30dB at 45GHz as shown in Fig. 8 and the derived normalized impedance seen by the microwave probes is also plotted on the Smith chart in Fig. 6. Crosstalk between orthogonal leads was approximately -40dB or 10dB lower than parallel leads.

IV. Discussion

Similar microwave measurements for other packaging technologies exist in the literature and they are summarized in Fig. 9 [5]. Although some of these measurements take into account the effect of the substrate material when the packages are flip-chip mounted and our measurements do not (since all measurements were made at wafer-level), it is seen that the SoL measurements rank high in the figure. However, the ultra-high I/O density of SoL can provide an exceptionally high I/O bandwidth that probably cannot be easily matched by the other packaging technologies in a cost effective and high performance manner. For example, if 8,000 leads are assigned as signal I/Os and operated at only 5GHz, the SoL package shown in Fig. 4 can yield an aggregate *electrical* I/O bandwidth of 40Tb/(cm^2-s). Moreover, since no underfill is required during assembly, SoL packages avoid all microwave performance degradation caused by underfill that is essential for flip-chip and BGA packages [6-7]. Since the size of the package is exactly equal to the size of the die, chips may be tiled as close as possible thereby reducing signal delay and degradation between them. To this end, a high-density substrate, shown in Fig. 10, has been fabricated using low cost multi-crystalline Si in a process similar to that used to fabricate on-chip multi-level interconnect networks. However, unlike on-chip interconnects, complete power and ground planes can be fabricated to improve electrical performance as a result of ideal signal return path.

Future work will include the fabrication of a SoL package with both optical and RF I/Os as well as reliability characterization.

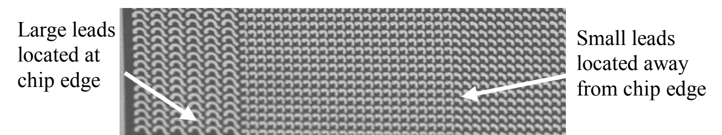


Fig. 4: SEM micrograph showing portion of a SoL package with 12x10^3 x-y-z compliant chip I/O interconnects distributed across a cm^2. In-plane compliance compensates for the coefficient of thermal expansion mismatch between the chip and the substrate. Out-of-plane compliance is needed during wafer-level testing/burn-in due to non-planarity of testing boards.

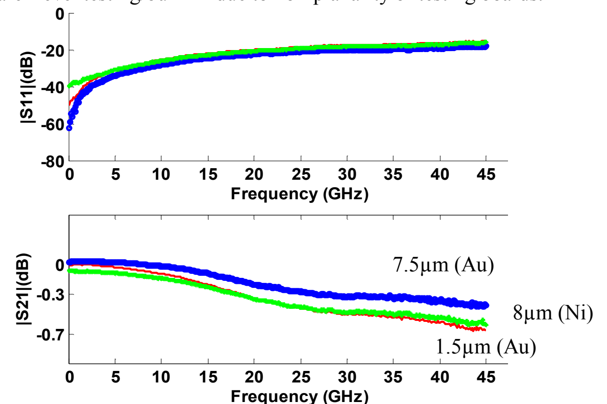


Fig. 5: Return-loss and insertion-loss versus frequency as a function of lead thickness and metal. The three curves are labeled according to the metal used to plate the leads and their thickness. All measurements were made on the large leads located at the chip edge as shown in Fig. 4, which are approximately 110µm in length and 20µm in width. In addition, the leads were fabricated on a Si wafer with a 15µm thick polymer layer. It is clear that thicker leads provide lower insertion-loss and Au leads out perform Ni leads. Au leads 15µm in thickness were also tested and they attained an insertion-loss of less than 0.2dB at 45GHz, which is approximately 0.1dB better than the insertion-loss of the 7.5µm thick Au leads at that frequency. The final lead thickness will ultimately be determined by both electrical and mechanical constraints. In this measurement, a thin Au layer was plated on the Ni leads to prevent Ni oxidization which could prevent reliable electrical interconnection between the microwave probes and the leads.

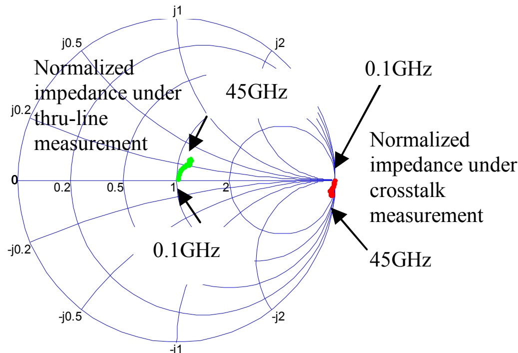


Fig. 6: Normalized impedance (as seen by the microwave probes) of the Au leads when they are under thru-line and crosstalk measurements. In the thru-line measurement, the leads were 7.5µm thick. In the crosstalk measurement, the leads were parallel to each other (60µm apart) and 15µm thick. It is important to remind the reader that the measurements do not reflect the impedance of a single lead, rather, the plotted normalized impedance is that of the ground-signal-ground lead interconnection.

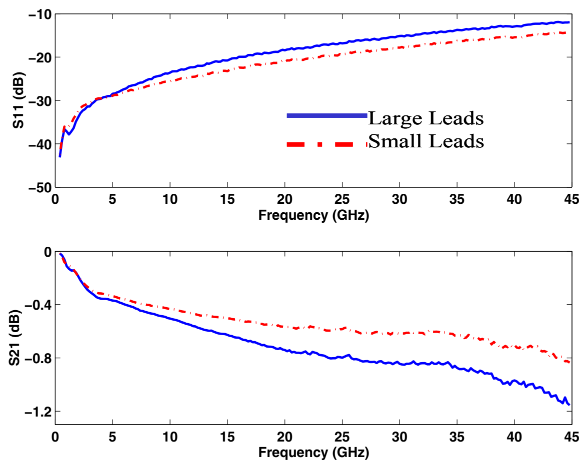


Fig. 7: Return-loss and insertion-loss versus frequency when two leads are interconnected by an approximately 100µm long and 1µm thick Cu interconnect at the wafer's surface. As indicated in the figure, this measurement was performed on a pair of large and small interconnected leads. While the shorter leads out-perform the longer leads electrically, the longer leads are mechanically more compliant than the shorter leads. Since both set of measurements were performed on the same die, all leads were processed identically and thus have the same thickness. In addition, the dimensions of the via through the package polymer layer are identical for the large and small leads. In this measurement, the compliant leads were 10µm thick and the package polymer layer was 15µm thick. The above plots include the effects of the 1µm thick Cu interconnect.

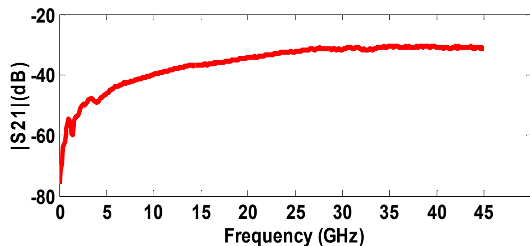


Fig. 8: Crosstalk measurement between the long Au leads shown in Fig. 4 when they are parallel to each other (60µm apart). In this measurement, the leads were 15µm thick and fabricated on a 15µm thick polymer layer. The normalized impedance of this measurement is plotted in Fig. 6.

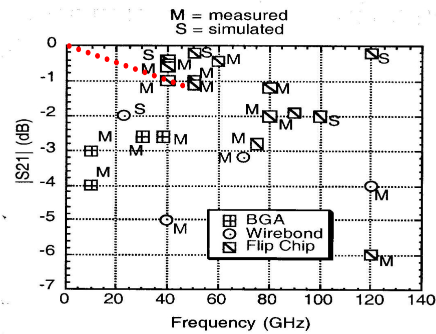


Fig. 9: A summary of insertion-loss versus frequency for BGA, flip chip, and wirebond packages (Original figure is reproduced from [5]). The dotted line is the approximate representation of SoL performance shown in Fig. 7 that measured insertion-loss of signal propagation into- and out- of the package using the large leads. It should be noted that some of the measurements plotted for the other packages take into account the effects of the substrate and our measurements do not (all measurements were made at wafer-level).

Fig. 10: A multi-crystalline Si board is used to fabricate a high-density substrate for SoL high-density packages. While organic substrates can also be used, this substrate is a potential alternative and its fabrication process is similar to that of on-chip multi-layer interconnect networks. The above micrograph shows two dice each with 10^3 area-array distribution of bumps on a cm^2 area bonded to the substrate. The dark region around the dice is flux residue.

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