Compliant Wafer Level Package (CWLP) With Embedded Air-gaps for Sea of Leads (SoL) Interconnections

Hollie A. Reed, Muhannad S. Bakir*, Chirag S. Patel*, Kevin P. Martin*, James D. Meindl*, and Paul A. Kohl

School of Chemical Engineering; *School of Electrical and Computer Engineering
Microelectronics Research Center; Georgia Institute of Technology
791 Atlantic Drive, N.W.; Atlanta, Georgia 30332-0269
(404) 894-9432; e-mail: paul.kohl@che.gatech.edu

Abstract

Sea of Leads (SoL) is an ultra-high I/O (input/output) density (>10^4 leads per cm^2) compliant wafer level package (CWLP) that potentially enables terabit on/off chip electrical bandwidth as well as enhances on-chip high current (e.g. > 290 A) distribution of a mixed-signal system-on-a-chip (SoC). The addition of embedded air-gaps may mitigate problems with thermal expansion between the chip and printed wiring board, increase effective compliance of the package for wafer level testing applications, and reduce the dielectric constant of the interconnect dielectric material. An SoL package with 12,000/cm^2 leads has been designed and fabricated, along with a prototype SoL package with 1,000/cm^2 leads on top of a dielectric layer containing embedded air-gaps.

I. Introduction

The prospect of gigascale integration (GSI) and system-on-a-chip (SoC) places substantial electrical performance constraints on the package, which must deliver high dc current (> 290 A) with minimal ground bounce as well as deliver high frequency signals (> 2 GHz) with minimal signal degradation [1]. On-chip interconnects, especially global interconnects which can span a chip's corner-to-corner distance, substantially reduce the global clock frequency. Sea of leads (SoL) wafer level packaging technology provides an ultra-high I/O density of x-y-z compliant leads (>10^4 per cm^2) to enable high power and high electrical bandwidth requirements of future SoC [2]. SoL provides the capability of enhancing the performance of a SoC by routing critical on-chip global interconnects off-chip to reduce signal delay and increase global clock frequency [3]. In addition, SoL minimizes on-chip IR voltage drops as well as simultaneous switching noise (SSN) by allocating an ultra-high number of I/Os interconnections for voltage and ground distribution.

The mechanical performance of a package is as equally important as its electrical functionality for wafer level testing, protection, and reliability. Wafer level testing requires simultaneous contact to all die across a non-planar wafer. Air-gaps may be included with SoL to increase the effective compliance of the package for probe contact and other movements, to mitigate problems in thermal expansion between the chip and printed wiring board, and also to reduce the dielectric constant of the interconnect dielectric material. The combination of an x-y flexible lead with a z-direction compliant, low modulus composite containing an air-gap forms a structure capable of moving in three dimensions. This type of structure also eliminates the need for chip underfill during package assembly to the system board and can reduce the overall size and weight of the package.

Compliant wafer level package processing [4] and SoL fabrication utilizes wafer level processing, providing a low cost packaging technology. With only 3 masking steps, all dice across the wafer are fully packaged with both compliant leads and interposer [2]. The addition of embedded air gaps adds a single additional masking step to the fabrication process to enable wafer level testing and burn-in of all packages simultaneously.

II. Fabrication of SoL and Embedded Air-Gaps CWLP

SoL and embedded air-gaps are fabricated as a continuation of back-end-of-the-line processing. After back-end die pad fabrication, all dice across the wafer are packaged with an ultra high I/O density of x-y-z compliant leads (>10^4 per cm^2) [2]. The complete fabrication process is schematically depicted in Fig. 1. The compliant wafer level SoL package with embedded air-gaps permits *wafer level* functionality testing as well as *wafer level* burn-in to identify known good packaged die (KGPD).

A. *Mask 1: Air-gap fabrication*

Once the IC fabrication is complete and die-pads are exposed, the first step in SoL packaging, which is fabrication of the embedded air-gaps, immediately follows. The fabrication of these micro air-gap structures has been demonstrated through the use of a polynorbornene (PNB) sacrificial polymer (Unity™ 400), which thermally decomposes at 400-425°C [4]. The PNB polymer is spin-coated on the wafer and softbaked. The thickness of the sacrificial polymer film (i.e. ultimately the height of the air-gap) is controlled by both the weight fraction of the polymer in solution as well as the spin speed. Next an aluminum layer is deposited to serve as a hard mask for the polymer. Photolithography is used to define the air-gap pattern in the aluminum, followed by reactive ion etching (RIE) etching of the polymer and subsequent removal of the aluminum. The encapsulating polymer is then blanket coated onto the wafer. The polymer must be a low modulus material to allow the x-y-z compliant leads to deflect as needed during wafer level

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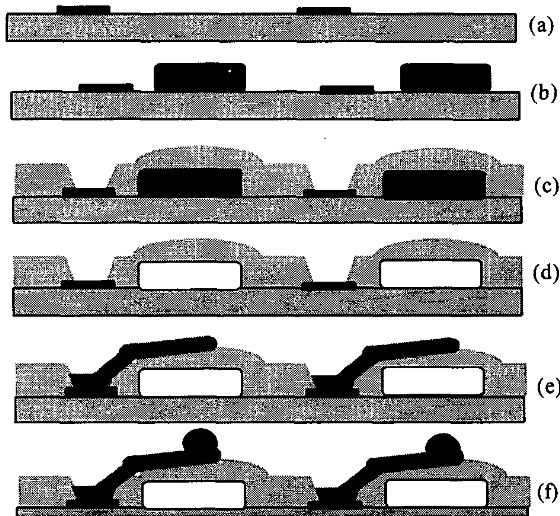

Figure 1: SoL and embedded air-gaps fabrication process (a) wafer with die-pads on the surface (b) application and patterning of sacrificial PNB polymer film (c) deposition of polymer encapsulating layer and via etching (d) decomposition of sacrificial polymer to air-gaps (e) electroplating of leads (f) electroplating and re-flow ol solder bumps

testing and burn-in, during thermal cycling, and provide the leads the capability to stretch and contract in the x-y axis.

B. Mask 2: Via patterning in overcoat polyimide

The second masking step (Fig. 1c) defines via holes in the polymer in order to provide contact to the underlying die-pads. These vias are etched in the encapsulating polymer using RIE. Following via etching, the thermal decomposition step of the sacrificial polymer (Fig. 1d) is performed by holding at the decomposition temperature for 1-2 hours in a horizontal tube furnace. The decomposition products diffuse through the overcoat material leaving a virtually residue-free hollow structure. A cross-sectional view of these air-gaps before lead fabrication is shown in Fig. 2. The decomposition occurs before electroplating the compliant leads in order to prevent stress or distortion of the leads that may occur during the decomposition process.

C. Mask 3: Lead fabrication

Once the polymer is etched exposing the die pads, SoL is then monolithically electroplated across the wafer to a 10 μm thickness (Fig. 1e). Photoresist is used as an electroplating mold. Electroplating 12K leads per cm^2 on a twelve-inch wafer translates into fabricating more than *8.75 million* leads in a series of parallel process steps.

D. Mask 4: Tin/lead solder ball fabrication

The final fabrication step is the formation of the solder bumps. Eutectic solder alloy (67% tin)\(33% lead) is electroplated on the tail end of the lead. Lead-free solder alloys are also process compatible with SoL.

The I/O density of the package was maximized based on compliance constraints and lead orientation. The final package is shown without embedded air-gaps in figure 3 with 12,000 I/O leads per cm^2 at a constant 80 μm pitch, different lead lengths of 53 and 106 μm, and lead width of 20 μm [2]. To demonstrate the compliant package with embedded air-gaps, a prototype was fabricated with a density of 1,000 leads/cm^2, an air-gap thickness of 10 μm and 170 μm in diameter, an overcoat polyimide thickness of 15 μm, and copper leads 10 μm thick and 250 μm in length. The resulting structure is shown in Fig. 4.

III. Enhancing SoC Electrical and Mechanical Performance Through Air-Gaps and SoL

The 1999 ITRS projects that the 50 nm generation node high performance chips will be 8.17 cm^2 in area and consume 174 w from a 0.6 V power supply (290 A) [1]. Based on a 12,000 leads per cm^2 [2], 50 nm generation node chips could have as many as 98,040 leads for electrical I/O interconnection. SoL technology can be used to enhance the electrical performance of a mixed signal SoC for this generation node.

A. Sol Enhances Electrical Performance

1. Increases Global Clock Frequency

SoL offers approximately 1800 package I/Os to route on-chip critical global interconnects off-chip for a higher global clock frequency [2]. On-chip wires are RC and RLC dominated while off-chip wires are LC dominated due to the large width of the interconnects. As a result, signal propagation reaches time of flight (ToF) delay, that is only limited by material properties.

2. Terabit I/O Bandwidth

The package's electrical bandwidth may be limited by the availability of the number of package leads as well as the package parasitics. The short complaint leads provided by SoL technology have low parasitic inductance and exhibit a self resonant frequency in the tera-hertz range [2]. If 10k leads (~10% of the total available leads) are allocated for

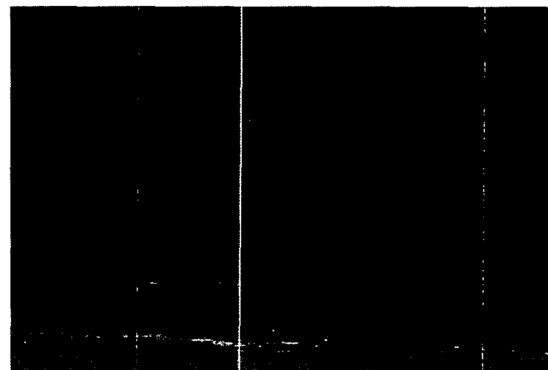

Figure 2: Cross-sectional SEM photograph of 170 μm wide air-gaps fabricated in Ultradel™7501 polyimide.

Figure 3: SEM image of SoL package containing 12K leads per cm^2 [2]. The leads are smaller at the inner region and larger at the perimeter to maximize I/O density, and oriented along the contour of expansion for a higher degree of compliance.

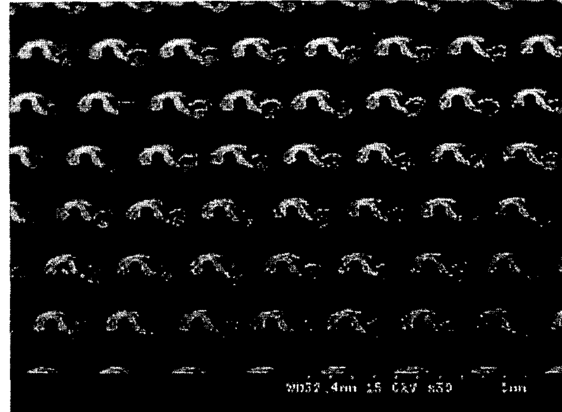

Figure 4: SEM image of SoL package containing 1000 leads per cm^2 and embedded air-gaps in the polymer dielectric layer under each lead.

signal transmission and each channel is operated at 4 Gbs, then the aggregate package bandwidth is 40Tbs.

3. *Enhances On-Chip Power Distribution*

One of the most stringent requirements of the 50 nm generation chips is the ability to dissipate 174 W from a 0.6 V power supply [1]. On-chip IR drops and ground bounce can be reduced for power distribution by using a large number of package leads for voltage and ground distribution [6]. If 85k leads are allocated for both voltage and ground supply (an order of magnitude greater than what is being projected by the ITRS), this would limit the maximum current in each lead to 6.8 mA. Another advantage of a high number of power leads is the ability to shield signal leads with ground leads significantly reducing cross talk and preserving signal integrity.

B. *Functional Testing*

The integration of different cores such as DSP, RAM, microprocessor, RF, and analog on a single chip requires careful testing considerations early in the chip design cycle [7]. If SoL can provide 1,240 leads for only AC/DC testing of a mixed-signal SoC, direct access to the various cores may be possible, providing insight and diagnosis of failure locations and mechanisms. The high number of leads will provide very high bandwidth to perform faster testing. In addition, the inclusion of embedded air-gaps provides mechanical compliance for waver level contact.

C. *Mechanical Performance of CWLP*

Mechanical testing has shown that incorporation of an air-gap into CWLP improves the effective compliancy of the package. The compliant lead repeatedly returns to position when a downward force is applied via a probe tip on the copper pad above the air-gap. In addition to experimental testing, mechanical modeling has also demonstrated improvements in 3-D compliancy through the combination of a flexible lead and embedded air-cavity.

IV. Conclusion

A prototype compliant wafer level package (CWLP) [4] with embedded are gaps has been designed and fabricated. The air gaps are comp atible with ultra high I/O density Sea of Leads (SoL) packaging technology. In this paper, the air-gaps were fabricated with a CWLP having 1,000/cm^2 leads. The complete fabrication process requires only four masking (monolithic) steps after the completion of the IC fabrication on a wafer to yield fully packaged dice ready for wafer level functionality testing and burn-in.

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