

Sea of Leads Ultra High-Density Compliant Wafer-Level Packaging Technology

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Abstract — Sea of Leads (SoL) is a novel ultra high-density compliant wafer-level packaging technology. SoL extends wafer-level batch processing of multilayer on-chip interconnect networks to include x-y-z compliant chip input/output (I/O) interconnects with a density exceeding 10^4 leads per cm^2 . A package with 12×10^3 compliant leads distributed across a cm^2 has been demonstrated. The compliance enables wafer-level testing as well as eliminates the need for underfill between chips and substrates with a CTE (coefficient of thermal expansion) mismatch thereby enhancing reliability, electrical performance, manufacturing throughput, and cost. Two methods of fabricating non-adherent or 'slippery' leads are demonstrated. The fabrication of slippery leads is desirable because adhesion between the lead and the package polymer layer is eliminated thereby freeing the leads to stretch and contract during thermal cycling. Compared to adherent leads, preliminary results show that slippery leads enhance the overall in-plane compliance. Moreover, the feasible z-axis compliance attained from polymer films with and without embedded air-gaps is compared. Following a series of micro-indentations, it is shown that a $35\mu\text{m}$ tall air-gap with $5\mu\text{m}$ of overcoat polymer yielded $18\mu\text{m}$ of z-axis compliance while a $35\mu\text{m}$ thick low-modulus polymer without an embedded air-gap yielded only $2.8\mu\text{m}$ of compliance at the same force (8mN). With 15mN of force, the polymer with embedded air-gap yielded $35\mu\text{m}$ of z-axis compliance. The electrical performance of the highly x-y-z compliant leads is excellent due to their short length. The dc resistance of a compliant lead as a function of its physical dimensions is analyzed. The typical value of resistance is found to be less than $25\text{m}\Omega$. Finally, the SoL package with $12 \times 10^3/\text{cm}^2$ compliant leads was characterized at wafer-level using a network analyzer in the 0.1-45GHz frequency range. Worst-case insertion loss into and out of the package was measured to be 1.15dB at 45GHz.

I. Introduction

The demand for high performance and low cost packages will become ever more critical as the semiconductor industry moves towards the development of a giga-scale system-on-a-chip (SoC). It is estimated by the International Technology Roadmap for Semiconductors (ITRS) that high performance chips in the 35nm technology node will drain as much as 400A and require chip-to-board bandwidth per signal I/O of more than 2GHz [1]. These requirements clearly call for the development of high-density and high performance packaging

technologies. No packaging technology has so far been able to satisfy these requirements while also being chip-size, low cost, and highly reliable. This is not difficult to understand considering that conventional chip manufacturing is divided into front-end, back-end, and tail-end processing. Front-end processing refers to the fabrication of transistors while back-end processing refers to wafer metallization. Tail-end processing refers here to the packaging of the individual dice. Conventionally, the final wafer-level process step is the fabrication of the die pads which serve as the interface between the die and the package. Each individual die, while still part of the wafer, then undergoes wafer-sort to identify known good die (KGD) followed by wafer singulation. The KGDs are then shipped to a packaging foundry where they are individually placed in temporary packages for burn-in. The dice that pass this test are then individually packaged and re-tested for functionality. This final step concludes tail-end processing and the packaged dice are finally ready for system assembly. From this description, it is evident how redundant and expensive tail-end processing is.

Sea of Leads (SoL) is a novel ultra high-density compliant wafer-level packaging technology (I/O density exceeding $10^4/\text{cm}^2$) and is proposed as a key enabling technology for a future high performance gigascale SoC. The overhead testing and temporary assembly steps between BEOL and TEOL in conventional packaging are eliminated with the use of SoL. Through a series of massively parallel monolithic process steps immediately following back-end processing, all dice across the wafer are packaged with x-y-z compliant leads laying on a low-modulus polymer with embedded air-gaps as schematically depicted in Fig. 1. In essence, SoL simply extends wafer-level batch fabrication of on-chip multilevel interconnect networks to include the chip I/O leads. Thus, this approach extends the economic benefits of wafer-level front-end and back-end processing to include packaging and testing. Novel design methods and fabrication of high-density compliant probe substrates for SoL are also currently under investigation in [2].

This paper first describes the fabrication process of highly compliant slippery leads on a polymer layer with embedded air-gaps in Section II. Section III presents a method of maximizing the I/O density of a SoL package based on compliance constraints. The attainable z-axis compliance from polymer films with and without embedded air-gaps is also discussed. Section IV characterizes the electrical performance of SoL from dc-to-45GHz through modeling and measured results. Section V is the conclusion.

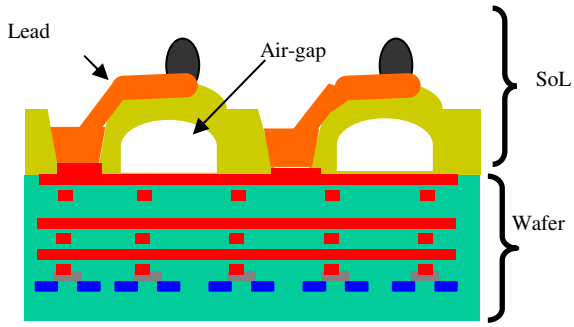


Fig. 1: A schematic representation of a SoL package. Through a series of monolithic process steps, dice across a wafer are packaged with a compliant interposer and leads enabling wafer-level testing and burn-in. In essence, SoL extends wafer-level batch processing of multi-layer interconnect networks to include chip I/O leads.

II. Methods of Fabricating Highly Compliant Slippery Leads

As described above, through a series of wafer-level process steps, highly compliant package I/O leads are fabricated. Two possible methods of fabricating a SoL package with slippery leads and embedded air-gaps are schematically illustrated in Fig. 2. The first process step in SoL fabrication is the application and patterning of the sacrificial polymer with the patterned geometry being ultimately the shape of the air-gap. The sacrificial polymer used in the package is described in [3-4]. Next, an overcoat polymer is deposited on the wafer to encapsulate the patterned sacrificial polymer. The wafer is then placed in a furnace where the sacrificial polymer is thermally decomposed to form an air-gap embedded within the overcoat polymer. The wafer at this stage in the process is illustrated in the SEM micrograph shown in Fig. 3. Next, vias are fabricated in the overcoat polymer to expose the die pads. As seen in Fig. 2, two different methods of fabricating the leads may follow at this stage in the process. Since the leads are typically greater than 10 μ m thick and must be resilient to oxidation, the leads are electroplated gold. The adhesion of the lead to the overcoat polymer may be controlled in several ways and the first method (Method 1 in Fig. 2) of doing so is through careful seed layer selection. For strong adhesion, a titanium/gold (Ti/Au) seed layer is sputter deposited where the Ti layer functions as an adhesion promoter between the Au layer and the overcoat polymer. For poor adhesion, Au alone can be sputter deposited on the wafer. If the die pads are copper (Cu), as they are in all the wafers used in this paper, the adhesion between the Cu pad and the Au seed layer is decreased without the Ti layer. As a result, in order to anchor the leads at the die pad end and leave the remainder of the lead free to move, electroless nickel (Ni) can be plated on only the Cu die pads as an adhesion promoter and diffusion barrier before the sputtering of the Au seed layer. Next, leads are plated and since the Au seed layer has poor adhesion to the overcoat polymer, so do the plated leads thereby creating the slippery leads.

The second method (Method 2 in Fig. 2) of fabricating the slippery leads is to plate the Au leads on a seed layer that is selectively etched away when the leads are ready to be released from the surface. This fabrication method was demonstrated by plating Au leads on a Ti\Cu seed layer.

Following the fabrication of the leads, solder bumps are fabricated on the lead's end. Following bump fabrication, the Cu seed layer is first selectively etched away with a dilute nitric acid solution and the Ti seed layer is etched next using Buffered Oxide etchant (BOE). Notice that neither etchant etches Au. It is best if the leads are released from the surface once all processing is completed (for alignment purposes) and this is much easier to implement using the selective seed layer etch method because the leads only become slippery once the seed layer is selectively etched. However, when the leads are plated on an Au seed layer, it is not possible to control their release.

The slippery leads fabricated using Method 1 (see Fig. 2) are shown in Fig. 4. The lead on the left is observed to move easily in the x-y plane due to lack of adhesion. Similar behavior was observed for the slippery leads fabricated using Method 2. Figs. 5-6 are SEM micrographs of a SoL package with embedded air-gaps. The I/O density of the packages in Figs. 4-6 is 10³/cm². However, these processes can be extended to packages with higher I/O density. Fig. 7 is an SEM micrograph of a SoL package with 12x10³/cm² leads and Fig. 8 is an SEM showing the fabrication of high-density solder bumps for this high-density SoL package. The ultra-high I/O density of SoL is visualized easier when it is compared to a low I/O density DIP package as shown in Fig. 9.

III. SoL Package Design and Mechanical Measurements

The I/O density of a SoL package is constrained by the amount of in-plane compliance required to compensate for the CTE mismatch between the chip and the substrate. The higher the CTE mismatch, the more compliance a lead must attain, resulting in larger leads and lower I/O density. Even with no CTE mismatch, the leads cannot approach zero in size (i.e., just bumps) because they would not provide any z-axis compliance. The CTE mismatch between the chip and substrate may be expressed by

$$\mu = \Delta T(\alpha_{pwb} - \alpha_{chip})x, \quad (1)$$

where μ is the maximum displacement (compliance) a lead must attain, α is the CTE of the component noted in subscript (PWB or chip), ΔT is the maximum change in temperature, and x is the radial distance from the center of the die. The three material and process dependant parameters of (1) are α_{chip} , α_{PWB} , and ΔT . Because Si is the dominant semiconductor material for gigascale integration (GSI) [5], the chip is assumed to be Si with a CTE of \sim 3ppm/ $^{\circ}$ C. In addition, because organic boards pose the highest CTE mismatch for Si chips, the substrate is assumed to be organic with a CTE of \sim 15ppm/ $^{\circ}$ C. The maximum temperature the chip and substrate are exposed to is taken to be 125 $^{\circ}$ C, the highest temperature of a shock reliability test.

Based on the above analysis, the I/O density of the SoL package shown in Fig. 7 was maximized. The application of Eqn. (1) proceeds as follows: First, a 3x3cm² chip area is partitioned into three different regions as shown in Fig. 10 and the maximum compliance in each region was calculated using Eqn. (1). The value of the calculated compliance in each region is shown in Fig. 10. The choice of the chip area is

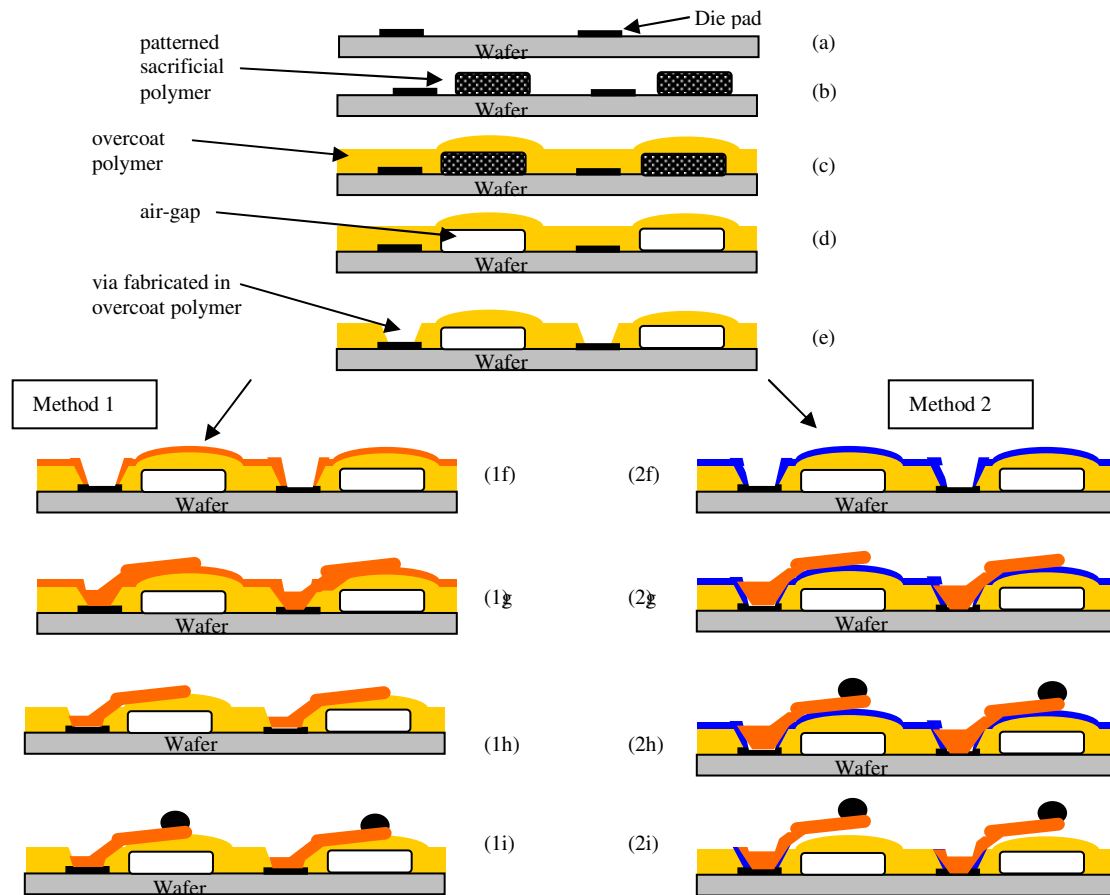


Fig. 2: Sea of leads fabrication process: (a) back-end-of-the-line processing is complete: die pads are exposed through passivation, (b) deposition and patterning of sacrificial material, (c) application of overcoat polymer, (d) sacrificial material is decomposed to form air-gaps [3-4], and (e) via fabrication in overcoat polymer to expose die pads. The wafer at this stage in the process is ready for lead fabrication. Method 1: (1f) Au seed layer is

deposited, (1g) Au leads are electroplated, (1h) Au seed layer is etched away, and (1i) solder bumps are fabricated on the leads. Method 2: (2f) Ti/Cu seed layer is deposited, (2g) Au leads are electroplated, (2h) solder bumps are fabricated, and (2i) seed layer is selectively etched away to release the leads from the polymer's surface. The typical thickness of the Ti/Cu seed layer is 300Å/2000Å.

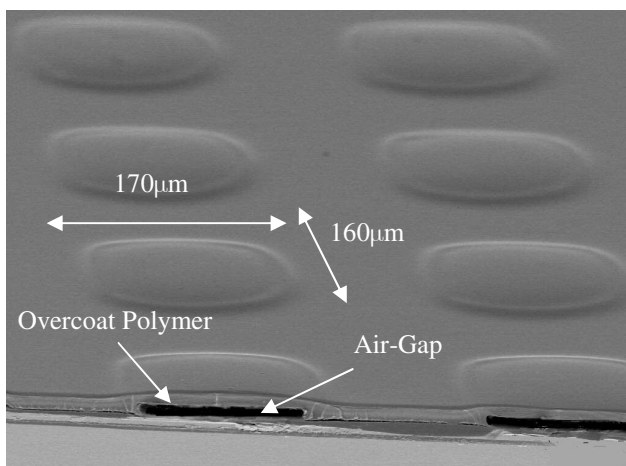


Fig. 3: SEM micrograph of a cross section of the highly compressible air-gaps after the sacrificial polymer has been thermal decomposed, i.e., process step (d) in Fig 2. Air-gap thickness and width can be varied across a wide range of values.

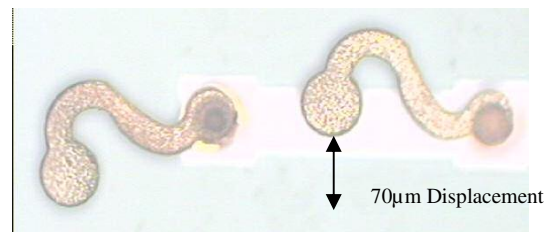


Fig. 4: Micrograph illustrating slippery leads. The lead on the left is shown to have moved by approximately 70µm after the application of a lateral force. This pair of slippery leads were fabricated using Method 1 in Fig. 2, i.e., an Au seed layer was used.

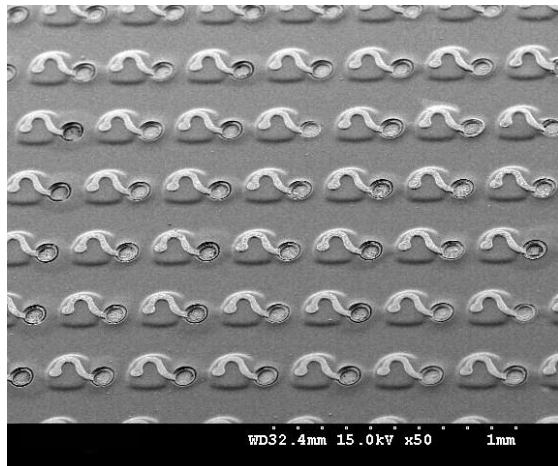


Fig. 5: SEM micrograph showing compliant leads fabricated on a polymer with embedded air-gaps.

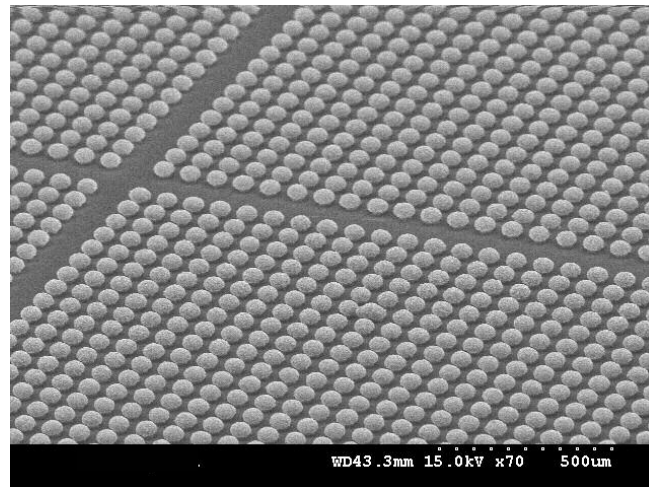


Fig. 8: SEM micrograph showing the fabrication of high-density solder bumps on a wafer ($12 \times 10^3/\text{cm}^2$). The bumps are electroplated eutectic tin/lead.

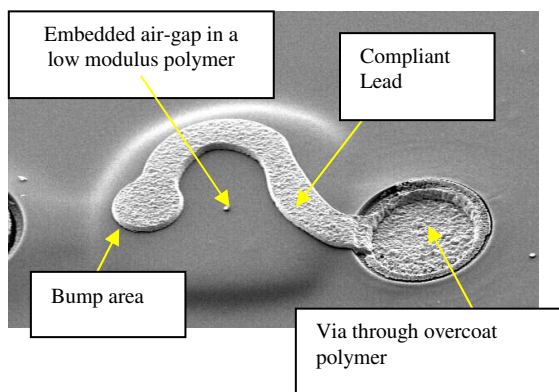


Fig. 6: Higher magnification SEM micrograph of a compliant lead fabricated above a highly compressible air-gap as schematically depicted in Fig. 1.

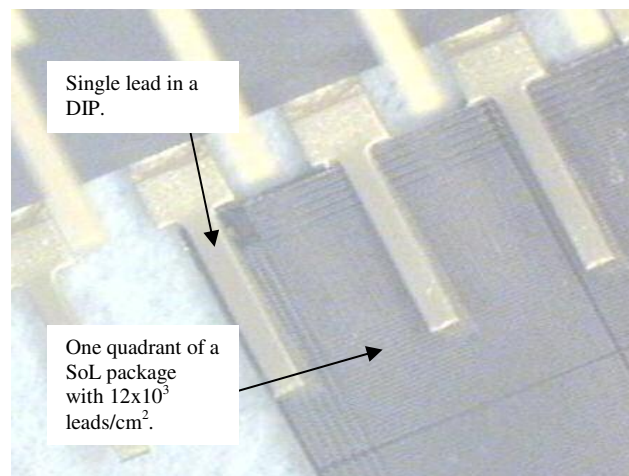


Fig. 9: Micrograph comparing the SoL package in Fig. 7 to a low I/O density DIP. Notice how three DIP leads occupy the same space as a single quadrant (3×10^3 x-y-z compliant leads) in the SoL package.

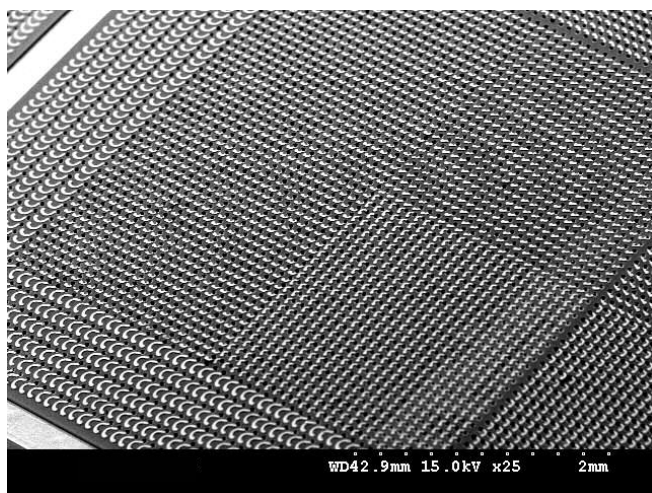


Fig. 7: SEM micrograph of one quadrant ($\sim 3 \times 10^3$ leads) of the fabricated SoL package with 12×10^3 leads per cm^2 . The package contains $53\mu\text{m}$ long leads distributed on an $80 \times 80\mu\text{m}$ square lattice and $106\mu\text{m}$ long leads distributed on an $80 \times 160\mu\text{m}$ rectangular lattice in regions 2 and 3 (Fig. 10), respectively. This distribution maximized the I/O density of the package.

based on the 35nm technology node high-performance ITRS projections [1]. The three regions were selected such that different lead designs and sizes can be implemented thereby maximizing the I/O density of the package. Following an iterative design process, two different lead lengths of approximately $60\mu\text{m}$ and $110\mu\text{m}$ were designed, the former being distributed on an $80 \times 80\mu\text{m}$ square I/O lattice in regions 1 and 2 and the latter being distributed on an $80 \times 160\mu\text{m}$ rectangular I/O lattice in region 3 as shown in Figs. 7 & 11. Next, the three regions are scaled downward to fit into a $1 \times 1\text{cm}^2$ area in order to meet our in-house reticle mask masking capability. The end result is an area array distribution of 10^4 leads in regions 1 and 2, and an area array distribution of 2×10^3 leads in region 3. One method to emulate the reliability of the $3 \times 3\text{cm}^2$ package using the fabricated $1 \times 1\text{cm}^2$ package is by using a substrate with a CTE higher than $15\text{ppm}/^\circ\text{C}$.

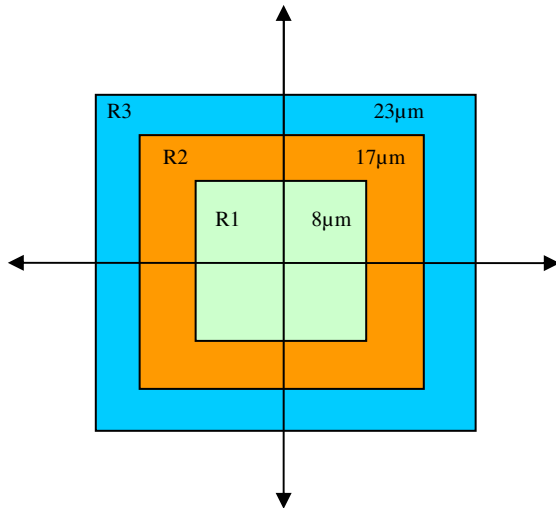


Fig. 10: Package partitioning into three regions (R1, R2, R3). This will later allow the design of smaller (less compliant) leads in R1 and R2, and larger (more compliant) leads in R3. As a result, the I/O density of the package is maximized. The required compliance in each region is also indicated in the figure.

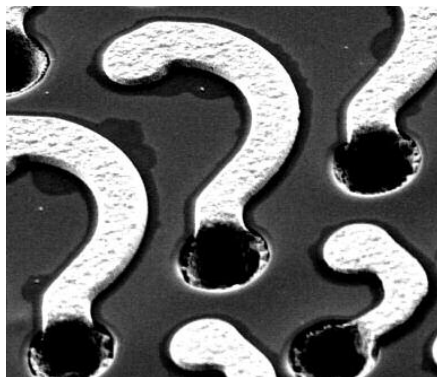


Fig. 11: SEM micrograph showing the two different lead sizes. The shorter leads are distributed in regions 1 and 2 of Fig. 10, while the longer leads are distributed in region 3.

The leads in the package under consideration were also oriented perpendicular to the contours of chip expansion for a higher degree of compliance flexing radially outward during thermal cycling. Fig. 12 is an SEM micrograph illustrating the perpendicular lead orientation with respect to the chip's contours of expansion at the chip's neutral region (center). Although the package has different lead sizes and various orientations, the final package has 12×10^3 I/O leads distributed on an $80 \times 80 \mu\text{m}$ square I/O lattice and an $80 \times 160 \mu\text{m}$ rectangular I/O lattice for simple substrate layout. The complete package is less than $70 \mu\text{m}$ in thickness and weighs less than $100 \text{mg}/\text{cm}^2$ providing an ultra-thin and lightweight package for hand-held as well as high-performance applications.

The design procedure for z-axis compliance in SoL differs from the design procedure for x-y-axis compliance. This fact can be easily understood by noting that the motivation for each is different: x-y-axis compliance compensates for the CTE mismatch between the chip and the substrate while z-axis compliance provides the ability for two non-planar structures to make reliable electrical contact, as required during wafer-level testing and burn-in. Recent research indicates that wafer-

level testing and burn-in requires approximately $50 \mu\text{m}$ of z-axis compliance [6]. The leads can achieve high z-axis compliance as long as the material/structure under the leads is very compliant. There are two methods of attaining this compliance in SoL. The first method is to fabricate the leads on a low-modulus polymer [7] and the second method is to fabricate the leads on low-modulus polymer with embedded air-gaps. The later method will be shown to be the better of the two experimentally.

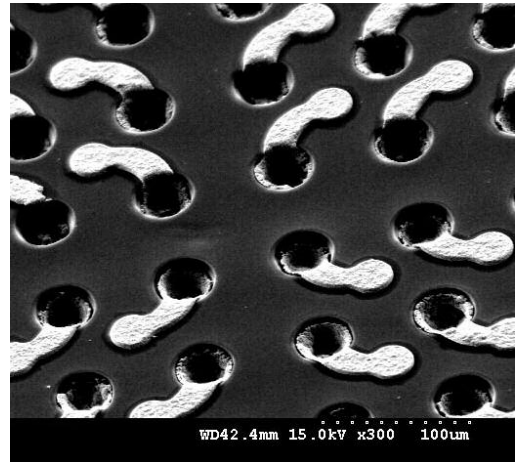


Fig. 12: SEM micrograph illustrating the leads' perpendicular orientation at the chip's neutral region (chip's center) for higher compliance.

An experiment was designed to allow comparison between the two methods of attaining z-axis compliance. For the first method, two wafers were spin coated with two different thicknesses of a polynorborene polymer called Avatrel that has a manufacturer specified tensile modulus of $\sim 0.5 \text{GPa}$. After polymer cure, the first wafer had a $18 \mu\text{m}$ thick layer while the second wafer had a $35 \mu\text{m}$ thick layer. Using Hysitron's TriboIndenter, the force-displacement properties of the two polymer films were tested. For this measurement, a $10 \mu\text{m}$ wide 60° conical tip was used. In addition, a trapezoidal force load function was used with a 10-second ramp to 8mN followed by 30-second hold and finally a 10-second downward ramp to 0N . The force-displacement curve of the $35 \mu\text{m}$ thick polymer film is shown in Fig. 13. The maximum recorded displacement for this sample at 8mN was approximately $2.8 \mu\text{m}$. A similar measurement was made for the wafer with $18 \mu\text{m}$ thick polymer layer, and the recorded maximum displacement at 8mN was approximately $1.6 \mu\text{m}$. In both samples, there were no permanent indents on the polymer's surface indicating purely elastic deformation during the measurements. Based on these measurements, if we assume a 10% compression ratio for this polymer ($1.6 \mu\text{m}$ displacement for $18 \mu\text{m}$ thick polymer film), then the polymer must be $500 \mu\text{m}$ thick to provide $50 \mu\text{m}$ of compliance at 8mN . A polymer layer that thick would not only complicate fabrication but also degrade SoL design compatibility with board-level optical waveguide interconnection [8].

The second method of attaining z-axis compliance is by fabricating embedded air-gaps within the polymer film. To compare the two methods, a similar experiment was conducted where $30 \mu\text{m}$ thick air-gaps with $5 \mu\text{m}$ thick polyimide overcoat (with an approximate modulus of 5GPa) were fabricated on a

wafer. The patterned air-gap geometry on the wafer was a $190 \times 190 \mu\text{m}^2$ square shown in Fig. 14(a). The force-displacement characteristic of this structure is shown in Fig. 15 illustrating a $30 \mu\text{m}$ displacement at 55mN . At forces beyond 55mN in magnitude, the tip contacts the substrate (Si) giving rise to the spike shown on the curve. The same air-gap structure after the indent is shown in Fig. 14(b) and clearly illustrates that the overcoat polymer did not puncture following the indent. The black spot is simply the deformation of the overcoat polymer once the indenter's tip reached the substrate's surface. A similar indent was also made on a rectangular air-gap geometry with dimensions of $9 \text{mm} \times 190 \mu\text{m}$. The force-displacement curve of this structure at its center is shown in Fig. 16 and shows a maximum displacement (compliance) of $35 \mu\text{m}$ at 15mN of force. The force-displacement ratio of this structure is much lower than that of the square shape air-gap shown in Fig. 15, i.e., both air-gap shapes attained approximately $30 \mu\text{m}$ of compliance at substantially different force magnitudes. This result indicates that air-gap geometry plays an important role in the design of z-axis compliance in SoL. In addition, air-gap thickness, overcoat polymer thickness, and the modulus of the overcoat polymer also influence the attainable z-axis compliance at a given force.

When the two different methods of attaining z-axis compliance are compared, it is evident that the method of fabricating embedded air-gaps within the polymer film provides a superior way of attaining high z-axis compliance. At 8mN , the polymer film with embedded air-gaps yielded approximately $18 \mu\text{m}$ (see Fig. 16) of compliance compared to the $2.8 \mu\text{m}$ compliance yielded by $35 \mu\text{m}$ thick polymer film without embedded air-gaps. The above z-axis measurements were made on embedded air-gaps without any leads fabricated above them. It is expected that the force-displacement ratio of the embedded air-gaps with and without the leads will be different.

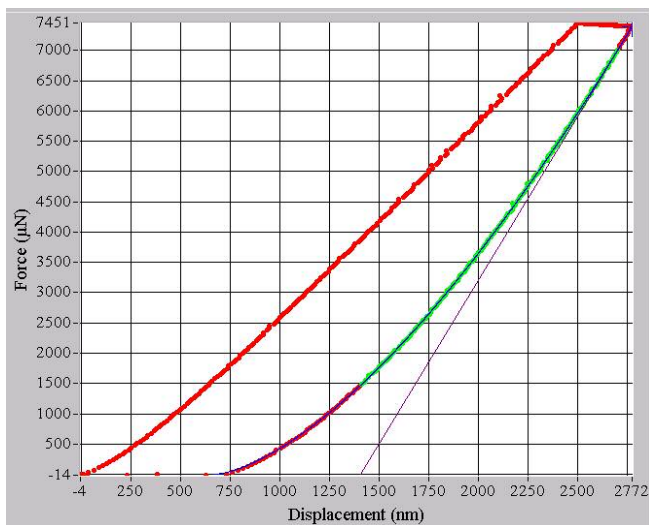


Fig. 13: Force versus displacement characteristics of the $35 \mu\text{m}$ thick Avatrel polymer film. For this measurement, a $10 \mu\text{m}$ wide indenter tip was used. In addition, a trapezoidal force load function was used.

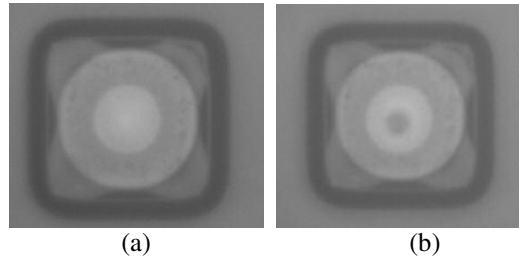


Fig. 14: (a) A $30 \mu\text{m}$ tall air-gap embedded within a $5 \mu\text{m}$ thick overcoat polymer. This image is before the indent. (b) The same air-gap shown in Fig. 12(a) after the indentation shown in Fig. 15.

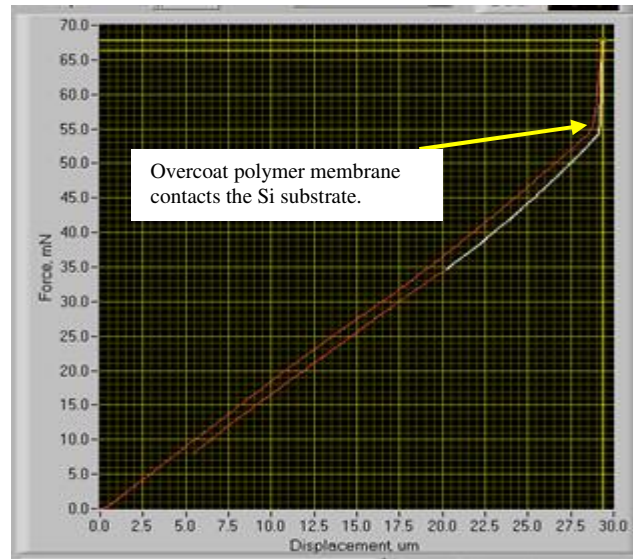


Fig. 15: Force versus displacement characteristics of the air-gap structure shown in Fig. 14. The attained z-axis compliance is $30 \mu\text{m}$ at 55mN . At forces higher than 55mN , the overcoat membrane contacts the wafer surface giving rise to the spike. The thin overcoat polymer did not puncture following the measurement. For this measurement, a $20 \mu\text{m}$ wide indenter tip was used. In addition, a triangular force load function was used.

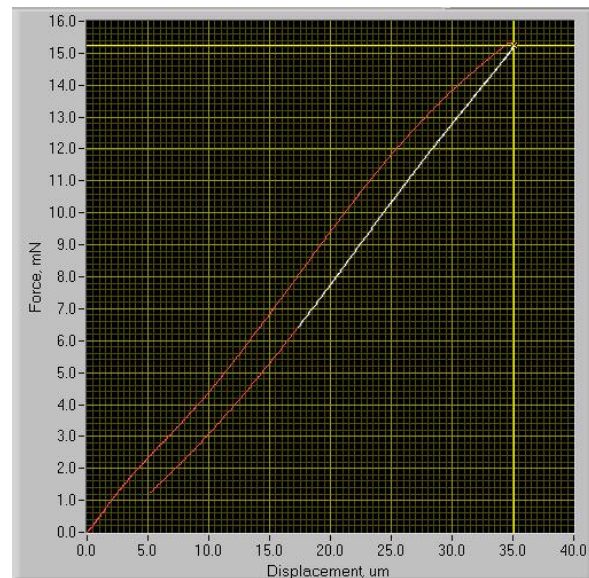


Fig. 16: Force versus displacement characteristics at the center of an embedded air-gap with rectangular dimensions of $9 \text{mm} \times 190 \mu\text{m}$. This structure attained lower force-displacement ratio than the structure shown in Fig. 14. For this measurement, a $20 \mu\text{m}$ wide indenter tip was used. In addition, a triangular force load function was used.

IV. SoL Electrical Characterization

Not only do SoL packages exhibit excellent mechanical performance, but also excellent electrical performance from dc to the frequency of 45GHz. This section will demonstrate SoL's high electrical performance through both modeling and measured results.

The dc resistance of a lead is a function of the lead's cross sectional area and length as shown in Fig. 17. The value of the resistance is seen to vary from 1mΩ to 60mΩ with a nominal value of approximately 20mΩ. At the risk of stating the obvious, low resistance is desirable to minimize power dissipation and heat generation in the package. In addition, because the leads are short, their self-inductance value was calculated to be less than 0.1nH. Low parasitics at dc are important for power distribution.

The highly compressible air-cavities can also reduce the package's electrical parasitics. The effective dielectric constant coupling the lead to the top most global wiring level can be reduced with the fabrication of embedded air-gaps. Considering the cross section view of the lead-polymer-air-gap structure shown in Fig. 1 and using Gauss's law and electromagnetic boundary conditions across the two dielectric media (the overcoat polymer and the air-gap), the effective capacitance coupling the lead to the top-most global wiring level can be approximated with

$$c_{eff} = \frac{\epsilon_{poly}\epsilon_0 A_{bottom}}{l_{poly} + \epsilon_{poly}l_{airgap}} \quad (2)$$

where A_{bottom} is the lead's surface area, l_{poly} and l_{airgap} are the thickness of the polymer and air-gap, respectively. ϵ_{poly} and ϵ_0 are the polymer's dielectric constant and permittivity of free space, respectively. Note that the relative dielectric constant of air does not appear in the expression because it has a value of unity. This equation clearly demonstrates that capacitance decreases with increasing air-gap thickness.

The microwave characteristics of SoL were measured at wafer-level using a two-port network analyzer with 150μm coplanar ground-signal-ground probes. Fig. 18 is a plot of the return-loss and insertion-loss versus frequency for signal propagation into and out of the package as illustrated in Fig. 19. The leads were 10μm thick and the package polymer layer was 15μm thick. No air-gaps were fabricated in this sample and a Ti adhesion promoter layer between the lead and the polymer was used. The leads were interconnected through a 1μm thick Cu interconnect at the wafer's passivation layer. The measured insertion-loss includes the losses due to the Cu interconnect.

A key interconnection level that will be severely challenged by GSI is the chip-to-module interconnection that integrates the packaged chip into the system. The 35nm technology node ITRS projections for high-performance, cost-performance, and hand-held market sectors are summarized in Fig. 20. The ITRS highlights these projections in red on the roadmap indicating that there are no known packaging technologies that meet these requirements. Fig. 21, on the other hand, presents the possible number of I/Os using SoL for the same chip dimensions presented in Fig. 20 and using an I/O density equal to $12 \times 10^3 / \text{cm}^2$. In both tables, the number of

power and ground I/Os is assumed to be equal to two-thirds of the total number of chip I/Os with the remaining I/Os dedicated to signal. It is clear that SoL provides at least an order of magnitude more I/Os than is projected by the ITRS for as far as the 35nm technology node. This is important because the simultaneous-switching noise, IR voltage drops, and total area consumed by global power distribution decreases with the increasing number of power and ground I/Os [9]. In addition, with an I/O density exceeding 10×10^3 leads per cm^2 , SoL can also increase I/O bandwidth, satisfy 3D structure I/O demands, and improve isolation in mixed signal systems. As a result, SoL provides numerous opportunities of performance enhancement for a 2011 and beyond gigascale SoC.

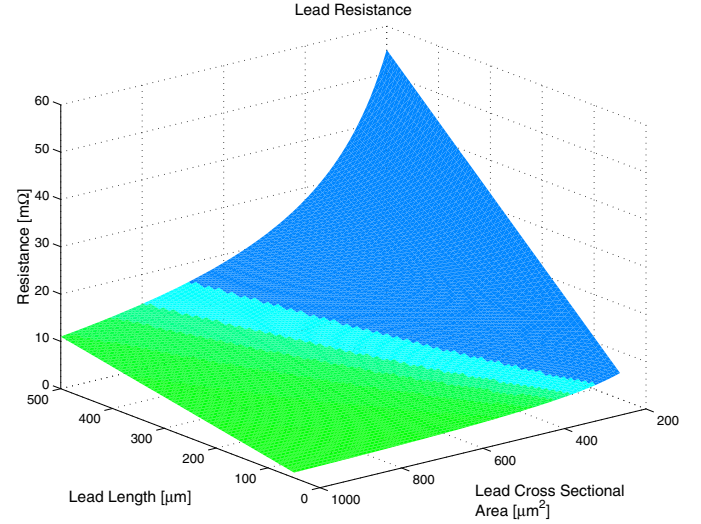


Fig. 17: DC resistance of a compliant lead as a function of the lead's cross sectional area and length. It is assumed that the lead is gold.

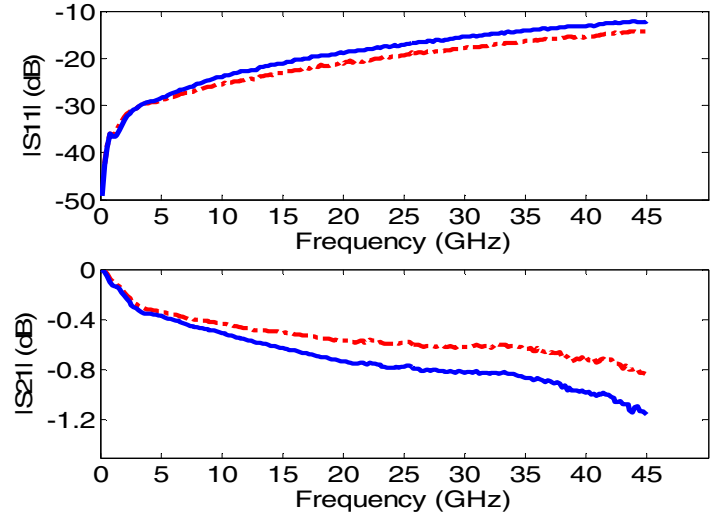


Fig. 18: Return-loss and insertion-loss versus frequency for a pair of interconnected leads (see Fig. 19). The dotted line represents the performance of the small lead pair while the solid line represents the performance of the long lead pair (see Fig. 7).

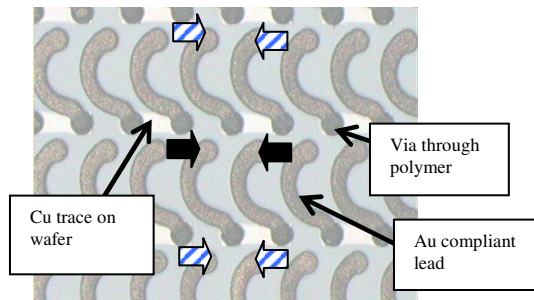


Fig. 19: Two-port microwave measurement setup for the plots shown in Fig. 18. The stripe arrows represent the ground probes and the black arrows represent the signal probes. Similar setup was used for the smaller leads shown in Figs. 7 & 11.

	High-Performance	Cost-Performance	Hand-Held
Die Area (mm ²)	937	351	90
Aggregate Current Drain (A)	366	230	9
Number of Package I/Os	8,758	3,541	1,167
Number of Power and Ground I/Os	5,868	2,372	782
Number of Signal I/Os	2,916	1,179	389
Current per power I/O (mA/lead)	124.7	193.9	15.4

Fig. 20: Summary of the 35nm technology node ITRS projections for various market sectors [1]. According to the roadmap, there is no known packaging technology that meets all these requirements.

	High-Performance	Cost-Performance	Hand-Held
Number of Package I/Os	112,440	42,200	10,800
Number of Power and Ground I/Os	75,335	28,220	7,236
Number of Signal I/Os	37,442	14,026	3,596
Current per power I/O (mA/lead)	9.7	16.3	2.5

Fig. 21: This table summarizes the possible number of package I/Os using SoL ultra high-density packaging technology based on the die areas noted in Fig. 20. Notice that SoL provides an order of magnitude more package I/Os than is projected by the ITRS. This has the consequence of significantly lowering the current per I/O and therefore enhancing power distribution and bump reliability.

V. Conclusion

Three intimately interrelated aspects of Sea of Leads (SoL) packaging technology have been described. First, two methods of fabricating slippery leads have been described. Slippery leads are highly compliant in-plane because they do not adhere to the underlying polymer surface thereby mechanically decoupling the leads for restriction-free motion. Second, the paper described a method where the I/O density of the SoL package was maximized based on mechanical constraints. The end result is the design of small, less compliant leads at the package inner region and large, more

compliant leads at the package edges. In addition, the leads in the package under consideration were oriented perpendicular to the chip's contours of expansion for a higher degree of compliance. Moreover, it was shown that polymer films with embedded air-gaps provide much higher z-axis compliance than polymer films without embedded air-gaps. For the same force load, polymer films with embedded air-gaps provided ten-times higher compliance. In fact, the polymer film without air-gaps yielded only 10% compression while the polymer film with embedded air-gaps yielded 100% air-gap compliance at low forces. Third, and finally, this paper demonstrated that the compliant leads do not degrade the electrical performance of the package through modeling and microwave measurements. Based on the above analysis, SoL technology can find application in high performance systems to enhance their performance, cost, and manufacturing throughput.

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