

An Analysis of the Gap Between PWB Technology and Chip I/O Interconnect Technology, and a New Wafer-Level Batch Packaging Concept

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Abstract

A dramatic reduction in the size and cost of electronic devices has taken place in the past decades. The functionality of electronic devices continues to increase leading to higher I/O counts. This trend of reduced size and higher I/O count requires the examination of the compatibility between the integrated circuits (IC) and the Printed Wiring Board (PWB) interconnection technologies. Wafer level batch packaging addresses the packaging and interconnections needs of IC by building flexible embedded leads in a compliant overcoat that will extend the on-chip I/O pad to the point where it can be directly attached to the system Printed Wiring Board (PWB) without using underfill. As such, the entire assembly is an extension of IC fabrication and on-chip interconnections. In this paper, the IC and PWB interconnection needs are analyzed and compared. First, an analysis of the I/O needs of ICs from the NTRS roadmap are compared to the microvia PWB technologies from NEMI, ITRI and JPCA roadmaps. Various IC-to-PWB interconnection technologies are examined to study their use and limitations in meeting the I/O needs of future IC under wafer level batch packaging concept. Second, the products from specific PWB manufacturers are reviewed in terms of roadmap needs. Third, the impact of IC and PWB interconnection designs on the electrical performance issues such as I/O current density, cross talk, off-chip speed are qualitatively described. This analysis indicates that the opportunities for miniaturization lie on the chip-side rather than on the PWB side.

Key words: IC and PWB interconnections, Technology Roadmaps, Microvia PWB Technologies, High-Density Packages, Wafer Level Package, Electrical Performance Issues.

Introduction

Steady advancement of the semiconductor industry and, in turn, the electronic industry depends on the success of three intertwined sectors: the integrated circuits (IC), electronic packaging, and printed wiring board (PWB) industries. ICs on a silicon die (chip) provide the functionality and performance of electronic products. The electronic package, electrically and mechanically, connects the IC to PWB. Along with discrete devices, the PWB connects the packaged ICs to make a complete electrical system. Because of this interdependence among the technology sectors, the progress of the electronic industry is limited by the least advanced of the three technologies. The IC is the industry driving force leading the way by reducing the minimum feature size of transistors and integrating millions of transistors on a single chip- achieving high performance and increased functionality demanded by modern electronic products. This has also raised

the number of input/output (I/Os) connections required by an IC, placing greater demands on the electronic package and PWB technologies. To meet the smaller, thinner and lighter product demands of portable electronics, electronic packages have scaled from an area ratio of 100:1 (package area to IC area) to 1:1, as provided by chip scale package (CSP) and wafer level packaging technologies. These developments have challenged the electronic package technology to meet two advancements, higher density of wiring and higher I/O count, leading to very high I/O density packages. To cope with this high I/O density, electronic packages are shifting towards area-array I/O distribution utilizing interconnection technologies such as solder bumps, stud bumps, stencil printing and conductive adhesives. These advanced packages with small footprint occupy less space (surface mounting area) on PWB and enable the reduction of total PWB area. Smaller PWB, in turn, reduces the size, height and weight of the

products as desired by the portable market. As such, more I/Os have to be routed within smaller mounting area on PWB by achieving small geometry features (i.e. via land, via, line/space) and multiple wiring levels. It is important at this juncture to carry a three pronged study to analyze the compatibility among the IC, packaging and PWB technologies.

As the industry moves forward with the challenges of integrating billions of transistors on a single chip, miniaturizing the footprint of the package to equal the area of the chip, and providing very high density wiring on the PWB, a careful examination of the progresses of IC, package and PWB interconnection technologies with respect to each other is essential. Any mismatches among the technologies and/or their limitations need to be identified so that they can be effectively resolved by development of proper design guidelines. In the following sections, we analyze the I/O needs of ICs as projected by the International Technology Roadmap for Semiconductors (ITRS). Electronic package and PWB technology projections are studied as described in the National Electronics Manufacturing Initiative (NEMI), Japan Printed Circuits Association (JPCA), and Interconnection Technology Research Institute (ITRI). The needs of the IC technology and required wiring density on the PWB are studied by means of an analytic model. Particular attention is paid to derive the optimal number of PWB wiring layers and minimal device feature sizes (i.e. via pad, lines/spaces, via land, etc.) required to meet the I/O needs of future high performance ICs. State of the art microvia PWB technologies are reviewed to gauge their progress in meeting the needs of high performance ICs. The limitations in providing high I/O count and mismatches among the IC, package and PWB technologies are succinctly identified. Various electrical performance issues encountered when designing for very high density packages and PWBs are briefly discussed. A new wafer level batch packaging concept is described to address the I/O density demands of future electronic products.

Technology Roadmaps

Historically, many of the chip packaging requirements (e.g. technical performance, physical specifications, and manufacturing costs) have been spelled out in technology road maps prepared by the semiconductor industry, including the National Technology Roadmap for Semiconductors (NTRS) and more recently the ITRS 1998 update [1]. In this paper, we refer to both NTRS and ITRS since ITRS is in the developmental stage. Table 1 shows the total number of I/Os, chip area and I/O density specifications as derived from the ITRS for high-

performance chips in the years 2002, 2005, 2008, and 2011. High performance market is chosen since it requires the maximum I/O connections. The total number of chip I/Os and chip area are monotonically increasing- implying greater functionality and integration of transistors per IC. However, the number of I/Os (pads) increase faster than the area of the chip- yielding higher I/O density, as shown in table 1. This requires the package and the PWB to provide higher wiring density per unit area from one IC technology generation to the next.

Table 1: I/O Needs of High Performance ICs

Generation (year)	2002	2005	2008	2011
Area (mm ²)	430	520	620	750
Chip (IC) I/Os (pads)	2553	3492	4776	6532
I/O Density (pads/mm ²)	5.94	6.72	7.70	8.71

The scaling of IC dimensions and need for higher I/O density described in the ITRS is the basis for predictions of future directions needed in electronic packaging as described in the NEMI and ITRI roadmaps. The JPCA roadmaps describe research trends for the next generation of packaging and the PWB technology, based on the questionnaire survey including over a hundred questions. This survey was performed with the assistance of the Ministry of International Trade and Industry Mechanical Information Industry Office Electronic Equipment Section. The questions cover silicon technology, packaging, assembly, board, design & analysis tools, and optical interconnections. These roadmaps provide the directions for the changing paradigms in microelectronics. The increased density of transistors on ICs produces a critical need for higher density packages and PWBs as discussed earlier. As the package I/O pitch (center to center I/O pad distance) is much coarser than IC I/O pitch, the package roadmap concentrate on redistributing the IC I/Os in an area-array fashion, such as ball grid array (BGA), to provide high I/O density. To achieve higher wiring density, the PWB roadmaps reduce the minimum feature size of its devices (i.e. via pad, via land, signal lines and spaces) and increase the number of wiring levels- migrating toward micro-via boards. This trend is analyzed in Figure 1 where the roadmap projections for high density substrates from 1997 NTRS, 1998 NEMI and 1998 ITRI are compared in terms of minimum line/space widths. The roadmaps project varying line/space width depicting differing requirements of major technology markets, such as automotive, hand-held, memory, cost/performance and high performance. For our analysis, we plot the severest projections of each roadmap in Figure 1. This corresponds to flip chip

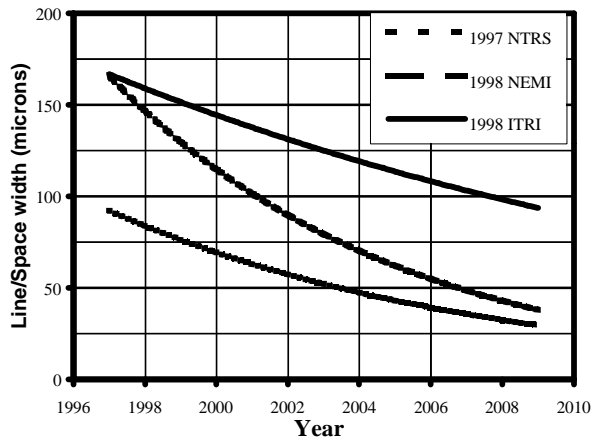


Figure 1: PWB (substrate) Technology Roadmaps

on substrate for 1997 NTRS and hand-held for 1998 NEMI. The 1998 ITRI only has one projection for line/space widths, called the state-of-the-art technology. The reader is, therefore, urged to analyze Figure 1 with caution. Driven by the growing demand of increased functionality, the NTRS projects the most aggressive trend in reducing the minimum feature size on the substrates. Close agreement between the NEMI and ITRI is seen circa 1997, however, significant divergence is observed in future years where NEMI projections coincide with the NTRS. Further investigation in the methodology used for projecting these values is necessary to determine the cause of this disagreement. However, the authors' viewpoint is provided to seek a valid clarification for the difference in the roadmap projections. If only a peripheral distribution with two to three rows of I/Os can be allowed as opposed to full area-array distribution, then the I/Os on the periphery have to be placed on a much tighter pitch as compared to the pitch required by an area-array distribution. When this package is mounted on the PWB, very fine line/space widths are needed to escape all of the inner I/Os to the periphery. On the contrary, a fully populated area-array distribution eases the minimum I/O pad pitch requirement-permitting coarser pitch as compared to the peripheral distribution. An assumption of a fully populated area-array distribution versus peripherally populated area-array distribution may have contributed to the differences among the roadmaps in Figure 1. The roadmaps try to project the advancement of the industry and their success in doing so can only be verified by actual products manufactured by the industry. The PWB industry's response to meeting the I/O needs of ICs will be examined later on in the paper.

We have thus far studied the needs of the ICs and corresponding technology projections of

electronic package and PWB industry by means of various technology roadmaps. To address the compatibility between the IC and PWB industry, thorough understanding of the impact of the number of wiring levels and the device feature size on PWB I/O wiring density is needed. How can the I/O needs of an IC be met by the PWB? Is the PWB industry capable of providing substrates with required feature size and the number of wiring levels? The electronic package is the bridge between the IC and the PWB. How compatible is the package to the IC and PWB? These questions are resolved in the following sections.

IC – PWB Compatibility Analysis

An analytic model [2] has been developed to calculate the number of I/Os routed by multi-layer PWB as a function of device feature size and the total number of wiring levels. The methodology used in the derivation of the model is succinctly described in Figure 2.

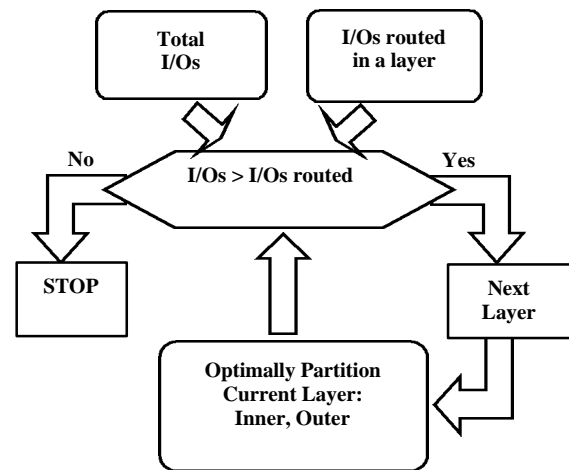


Figure 2: Calculation of Number of routed by PWB

Total number of I/Os need to be routed are first compared with total number of I/Os routed in one layer of the PWB. If total I/Os are more than the I/Os routed in one layer, then a second layer is utilized for routing of the extra I/Os. In doing so, the layers are optimally partitioned into inner and outer layers. The inner and outer layers are geometric interpretations where outer layer I/Os are routed within that layer and inner layer I/Os are routed in the next layer. This is repeated until total number of I/Os are routed. And in such case, the analysis stops and reports total number of layers needed to route the I/Os. The PWB feature sizes, I/O pad pitch, total mounting area along with the number of wiring levels are input to the model and given all of these inputs, the model

calculates the total I/Os routed by PWB. Optimum number of wiring levels and/or minimum feature size can also be easily found if the total I/Os are specified as an input. It is out of scope of this paper to go in detailed analysis of the model. It has been rigorously developed in [2]. The reader is urged to consult [2] for detailed analysis of the model. The multi-faceted features of the model are used in this paper to analyze the IC – PWB compatibility.

The impact of feature size and the number of wiring levels on total I/Os routed by PWB is shown in Figure 3. Number of wiring levels are allowed to vary from 1 to 10 and line/space width, t , is varied from 0.15mm (6 mils) to 0.10mm (4 mils) to 0.05 mm (2 mils). The diameter of via and via land on PWB are assumed to be $2t$ and $4t$, respectively. For a particular line/space width, the number of I/Os routed within PWB increases with the number of wiring level. A saturation point, however, is reached when all of IC I/Os are routed and the availability of more wiring levels is not needed. For example, using 2 mils line/space width, the number of I/Os routed in PWB increases with the number of wiring levels from one to four and a saturation point is reached beyond four wiring levels. Required value of feature size and number of wiring levels to meet the IC I/O needs can easily be derived from the model. To further illustrate this point, we compare the I/O needs of the IC and required PWB technology in Figure 4.

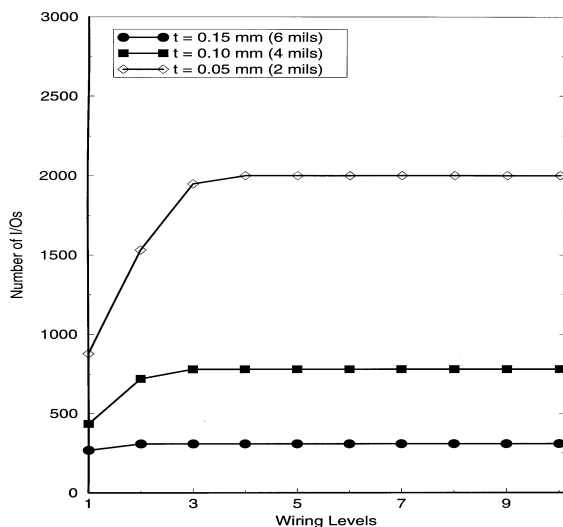


Figure 3: Number of PWB I/Os as a function of line/space width

For ICs packaged in wafer level packages, the area and the footprint of the package is equal to the area of the IC it contains. We also constrained the PWB to route all of the I/Os within the footprint of the package. The surface area required by the package on the PWB is therefore also restricted to the area of

the IC. These are the ultimate limits on the area of the packages and the PWB, nonetheless, required by future electronic products. To seek the size and packing density advantage of wafer level packages, the surface mounting area of the package on the PWB has to be the same as the package footprint. Divergence from this will be counterproductive to the implementation of the wafer level packages, hampering the goals of smaller, thinner, lighter products. The Total number of I/Os routed by multi-layered PWB is plotted versus the surface mounting area on the PWB in Figure 4. The number of wiring levels on the PWB are varied from four to seven while the PWB line/space width, t , is held constant at 50 μ m (2 mils). Also plotted in Figure 4 is the 1998 ITRS projections for the number of I/Os required by the high performance market. The high performance market is used in this analysis because it requires the maximum number of I/Os in all of the technology sectors. For a specific area, higher number of wiring levels yield higher I/Os as expected. For the PWB to meet the I/O projections of ITRS, technologies that yield curves above the ITRS curve must be used. For example, 2386 I/Os are projected for the area of 620 mm^2 . From Figure 4, we observe that this point is above four-layered PWB and therefore, will not meet the IC I/O projections. Five-layered PWB barely meets the requirement and higher levels will exceed the projections.

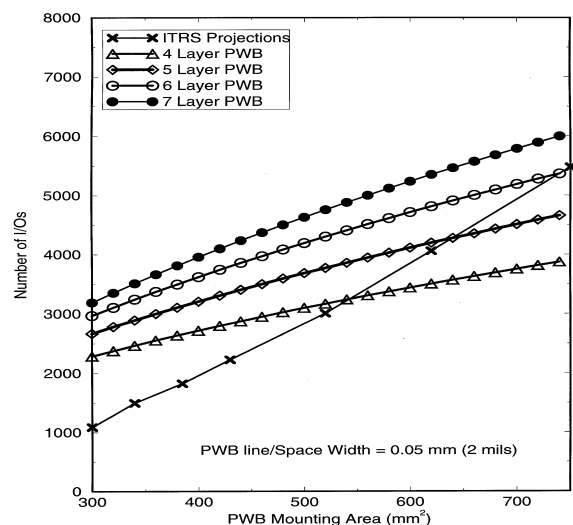


Figure 4: IC vs. PWB Compatibility

This gives a clear understanding of what PWB technology, in terms of levels and feature size, is needed to meet the I/O needs of the ICs. It can be inferred from Figure 4 that seven levels of wiring on the board with 50 μ m line/space width will meet the maximum I/O needs of an IC as projected in the

ITRS. The number of wiring levels referred in the paper account for levels used only for I/O signal routing and do not include levels used for power and ground distribution.

The PWB feature sizes and the number of wiring levels required to meet the IC needs have been defined in this section. How advanced are the PWB manufacturers in matching these requirements? We explore this question in the next section by discussing advanced PWB technologies as reported in the literature. The goal of the next section is to probe an aggregate progress of the PWB industry, by choosing examples of different technologies, in meeting the IC I/O needs and not to single out any one particular technology.

Microvia Printed Wiring Board Technologies

The wiring and via density of printed wiring boards (PWB) is a critical design feature for PWB used in flip-chip and direct chip attachment because the density of the I/O must match that of the integrated circuit (IC). Thus, numerous approaches have been followed in the development of high density PWBs. In this section, we will briefly review the fabrication methodology and cite the critical dimensions [3,4].

Ibiden has developed a double sided, four layer build-up, board (8 total layers of build-up) using fully additive copper plating and photosensitive epoxy. The four layers of build-up using microvia technology are on top of a drilled, through-hole board. The technology is capable of producing 35 μm copper lines with 35 μm spaces. The vias can be as small as 80 μm on 125 μm pads. The substrate for the fine-line build-up is a BT resin, copper-clad board with drilled through-holes. A photosensitive epoxy is used as the build-up dielectric material. The fully-additive copper process provides higher resolution metal patterns than subtractive copper processing because of the lack of copper undercutting experienced with subtractive processing. Excellent adhesion is achieved between the epoxy and the copper by using a blend of two epoxies- one with an imidazole hardener and one with an amine hardener. The amine serves as a soluble filler in the epoxy creating a rough surface when chemically oxidized during the surface roughening step. Excellent adhesion of the copper is achieved by mechanical anchoring in the small cavities of the roughened epoxy. Peel strengths of 1.2 kg/cm have been reported. The electroless seeding of the epoxy is followed by photoresist mask coating to form the shape of the metal lines. The photoresist mask is a permanent dielectric and left in place. The epoxy resin does not contain glass cloth. The glass cloth

assists in providing crack-resistancy of the dielectric layers in conventional boards. In place of the glass cloth, Ibiden uses an interpenetrated network structure of a linear, thermoplastic polymer interdispersed in an epoxy. The material composition was optimized for tensile strength (800 kg/cm²) and elongation-to-break (8%). The glass transition temperature was 200°C.

The IBM-Japan surface laminar circuit (SLC) also uses liquid dispensed photo-imaged epoxy in the build-up layers on FR4 or BT substrates. Four build-up layers on each side of the board can be produced. The negative-tone epoxy dielectric is deposited via curtain or slot coaters.

Hitachi Chemical has developed two types of metal clad boards called HITAVIA type 1 and HITAVIA type 3 for mother boards and BGA packages, respectively. In both cases, a metal-clad B-staged epoxy film is used to build the multi-layered structure. A key attribute of the epoxy laminate film is its rheological properties. The epoxy laminate must flow in order to cover the steps created by the conductor lines and fill buried via holes (BVHs) during the lamination process. However, no excess flow occurs eliminating the need for surface polishing and improving the spatial resolution of the lines and spaces. The technology is capable of producing 100 μm copper lines with 100 μm spaces for type 1 and 50 μm lines with 50 μm spaces for type 3. The vias are formed with pre-drilled holes in the laminate. The size of the vias can be 250 to 300 μm diameter on 500 to 600 μm pads for type 1, and 100 μm diameter vias on 250 μm diameter pads for type 3. A CO₂ laser is used to etch the microvias. The area to be etched is defined by patterning the copper metalization. Excellent adhesion (peel strength of 1.0 to 1.4 lb/in) and flame resistance (V-0) are reported. After the C stage cure, the epoxy materials show equivalent glass transition temperature, adhesion strength to copper and electrical properties to those of corresponding, conventional epoxy prepregs.

The Victor Company of Japan (JVC) produces a micro-via hole technology on conventional FR4 or BT substrates. The micro-via holes are etched by laser ablation. Two aspects of the process stand out. First, via etching is achieved by use of a conformal laser beam to produce tapered vias. Second, a two-layered dielectric application is used at each dielectric level to achieve a high degree of planarization. Two layers on each side of the substrate with 100 μm lines and 100 μm spaces have been produced.

NEC Toyama has developed high density micro-via (mV) PWB for use in high density, advanced microelectronic packaging applications. The mV technology is built on a conventional four-layer PWB with through-holes. Two layers of fine-line interconnection are fabricated on the board using CO_2 laser ablation for the micro-vias and additive copper plating for the conductors. A permanent photoresist is used defining the conductor patterns. High electroless copper plating rates were obtained ($5\text{ }m/hr$) by automated control and micro-filtering. The technology is capable of producing $50\text{ }m$ copper lines with $50\text{ }m$ spaces. The vias can be as small as $50\text{ }m$ on $150\text{ }m$ pads. NEC Toyama foresees that UV lasers will replace the CO_2 lasers when future miniaturization is needed.

Matsushita has developed unique stacked type substrate technology called "ALIVH" (any layer inner via hole structure). This technology has several advantages over conventional PWB manufacturing process. First, completely dry processes are used to form interconnections using laser ablation (currently CO_2 laser) and Cu paste for burried hole. Second, no plating processes are necessary to form conductive lines. Third, the structure is light weight due to the use of epoxy impregnated aramid non-woven fiber. Fourth, there are no limitations on the layout of interconnections. Lastly, the design time is shorter than conventional products. Matsushita has been successfully manufacturing ALIVH substrates with the following attribute: 30-50% substrate size reduction, 50% cost reduction, and 67% design time reduction compared to conventional PWB manufacturing method. Matsushita reported that its share in the Japanese cellular phone market has risen to 60% with the introduction of ALIVH substrates. The market share of ALIVH in high density substrate market is 38%, in terms of production capability. Matsushita's target for conductor line and space resolution is $50\text{ }m/50\text{ }m$ in 1999, and $25\text{ }m/25\text{ }m$ in 2000.

Toshiba has introduced a unique buried bump interconnection technology (B^2it). This technology is an adaptation of multi-layered ceramic processing. Silver paste is used to form conductive bumps on copper foil. The bumps have a conical shape and pressed into B-staged prepreg. The bumps penetrate the insulator and form a conductive path through the prepreg. The B^2it can be used by itself to form the multilayered substrate. Alternatively, B^2it can be fabricated on a conventional PWB core or microvia layers can be fabricated on B^2it using laser ablation or photosensitive insulators. B^2it has several advantages over conventional PWB technologies.

First, the silver paste printing method used to form interconnecting Ag bumps is simpler than drilling, using photovias or laser ablation vias. Second, no plating is necessary to form conductive lines in B^2it (only lamination using prepreg material). Third, there are no limitations on the placement of position of the interconnecting bumps. Fourth, there are few requirements on the interlayer dielectrics allowing new materials to be used. Lastly, the design time is shorter because there are no limitations on interconnection layout. Toshiba has been manufacturing 2 to 8 layer substrates with a 40% reduction in substrate size compared to those conventional boards. The via and land diameters are currently $200\text{ }m$ and $400\text{ }m$, respectively. Toshiba is planning to reduce these dimensions to $100\text{ }m/200\text{ }m$ and $50\text{ }m/75\text{ }m$ in the future. The conductive lines and spaces, currently $75\text{ }m$ width each, are being formed by subtractive processing using photoresist. Toshiba is pursuing $30\text{ }m$ lines and $30\text{ }m$ spaces by combining MCM-D processing on B^2it substrates.

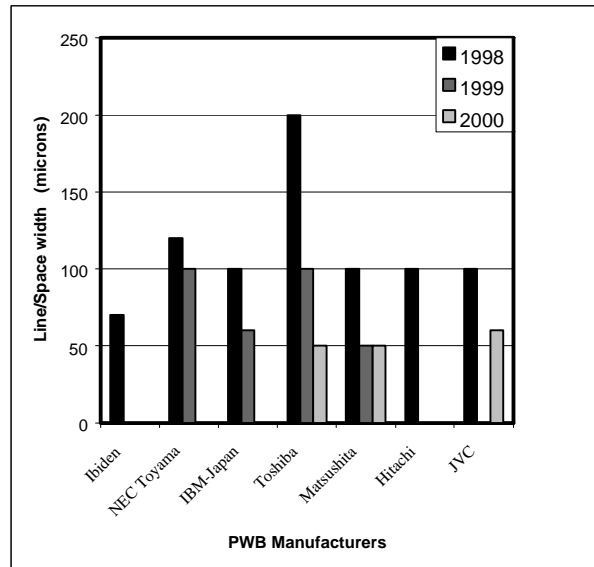


Figure 5: Minimum Signal Trace Width on PWB

The progress of PWB industry in terms of minimum feature sizes is summarized in Figure 5. The PWB feature sizes range from $50\text{ }m$ to $100\text{ }m$ and continuing a steady progression towards smaller values. Correlating this with Figure 1, we observe that PWB industry considerably ahead of the projections made by NTRS, NEMI and ITRI roadmaps. The $50\text{ }m$ line/space widths are projected to take place in 2004, 2006 by the 1997 NTRS and 1998 NEMI, respectively, whereas 1998 ITRI does not project a value below $100\text{ }m$. Two

sets of data are available with respect to the number of PWB layers. To avoid confusion, we have plotted both in Figure 6a and 6b. Maximum build-up layers without counting the core layers are shown in Figure 6a where they range from 2 to 10. In case of Matsushita, core layers are included with the build-up layers as this was the only information available. Figure 6b shows total number of layers on the PWB. These include both the wiring and power distribution layers. Wide range, 6 to 20, of total PWB layers are available from the industry.

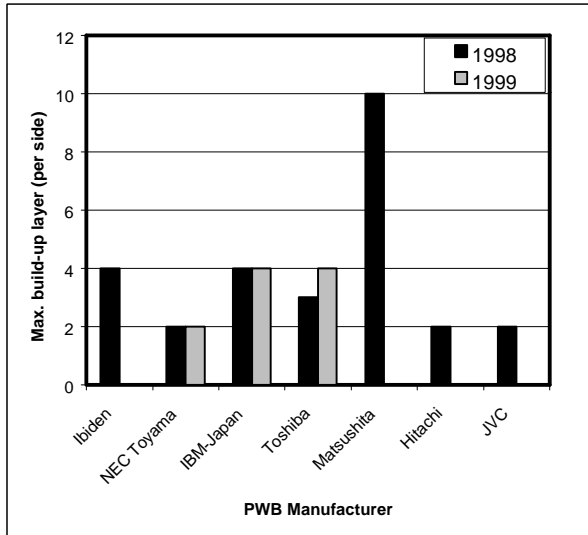


Figure 6a: Maximum build-up layers on PWB

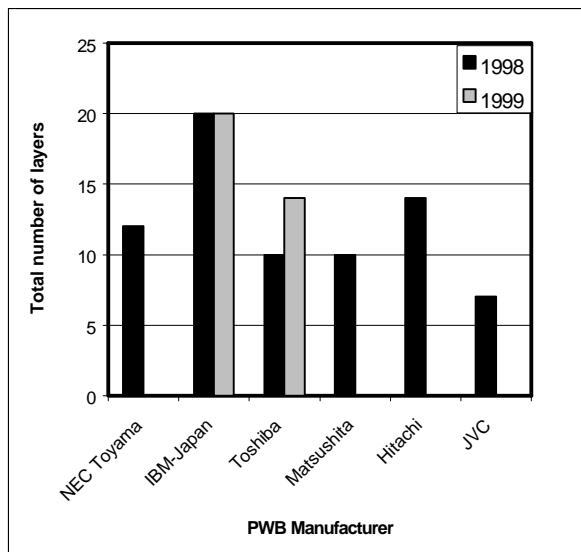


Figure 6b: Total Number of Layers on PWB

These values are in accordance and/or exceed the requirements of the IC as described in the 1998 ITRS update assuring full compatibility between the IC and PWB. To meet year 2011 I/O projections for high performance ICs, we need 50 μ m line/space and

seven wiring levels on the board. The status of the PWB industry assures these values at present time.

IC – Electronic Package Compatibility

The question that remains to be examined is the ability of electronic package in meeting the needs of IC and connecting it to the PWB. The IC has its high I/O count and PWB is capable of routing all of the I/Os. The package has to be able to complete the bridge between the IC and PWB. In case of direct chip attach (DCA) or flip chip, the IC – PWB compatibility has addressed all of the I/O needs. But for wafer level packages, the task of providing high I/Os is non trivial because of I/O pitch (center to center distance between two I/O pads) limitations of package interconnections and thermal mismatch issues between the IC and PWB. Wafer level packages use large solder bumps (150 μ m diameter and in excess of 300 μ m height) as their interconnection technology to withstand thermal and mechanical stress arising from thermal mismatch between the IC and the PWB. This limits the minimum pitch of these packages. Table 2 shows maximum package pitch allowed to address the I/Os of the high performance products.

Table 2: Package Pitch Requirement

Generation (year)	2002	2005	2008	2011
Area (mm^2)	430	520	620	720
Package Pins	1915	2619	3581	4898
Required pitch package (mm)	0.47	0.45	0.42	0.38

The area and the projected package pins for high performance ICs are given. The area of wafer level packages equals that of the IC it contains. The required package pitch is obtained by dividing the area by the pins and taking a square root. This gives pitch projections varying from 0.47 mm to 0.38 mm that are below the reported, 0.5-0.75 mm, pitch of wafer level packages. To effectively resolve the I/O pitch limitations of existing wafer level packages, a new Compliant Wafer Level Package (CWLP) [5] is under development at Georgia Institute of Technology. CWLP process addresses the packaging and interconnections needs of IC by building flexible embedded leads in a compliant overcoat that will extend the on chip I/O pad to the point where it can be directly attached to the system Printed Wiring Board (PWB) without using underfill. As such the entire assembly is an extension of IC fabrication and on chip interconnections. The mechanical compliance of embedded lead structures will address the thermal mismatch between the IC and the PWB, not requiring the use of large bumps for the purpose. This allows to scale down the package pitch to 0.25 mm at present and it is expected to reduce even more.

Such aggressive pitch will provide very high I/O density wafer level packages resolving the IC – electronic package compatibility. Being a chip size package, CWLP provides high I/O needs of ICs and is assembled on the PWB without the use of an underfill. In turn, retaining the size benefits of bare ICs while allowing more protection and ease in assembly.

Electrical Performance Issues

We have addressed the needs of IC and its compatibility with package and PWB. When implementing high density packages and PWB, the electrical performance issues must be carefully evaluated. In this section, we qualitatively identify some of these issues. Two such issues, total current density and the number of power/ground pins, are tabulated in Table 3.

Table 3: Electrical Performance Issues

Generation (year)	2002	2005	2008	2011
Total Power (W)	129	160	170	174
Core Voltage (V)	1.5	1.2	0.9	0.9
Total Current (A)	86	133.3	188.89	193.33
Power Pin Count	479	655	895	1225
Current Density /(Power Pin) A/cm ²	4.07	5.21	6.21	5.26

Power Pin Count: This assumes that 50% of the package pin count is devoted to power and ground distribution and that this number is equally divided between the power and ground pins.

Total Current, and Current Density/(Power Pin): The total current is derived from the power consumption divided by the core voltage. In calculating the current density/(power pin) the power pin is assumed to have a circular cross section with a radius equal to one-fourth the chip pad pitch. The current density/(power pin) is therefore the total current divided by the power pin count and area/(power pin).

Other chip packaging factors should be considered in addition to those cited above. According to the ITRS, in 2002 the chip-to-bus speeds will range from 100 MHz (hand-held) to 884 MHz (high-performance) and by 2011 it is expected that in the later case the chip-to-bus speeds will exceed 1.5 GHz. For speeds in beyond 400 MHz careful consideration should be made regarding impedance control of the flexible leads in the packaged chip and the methods used to attach the packaged chip to the system module (e.g. solder bumps or conducting adhesives). The frequency characteristics arising from the material properties and geometry of the combined flexible-lead and attachment bond figure in the impedance matching. The drive to replace lead-based solders is exemplified

in a recent announcement by the IPC to phase out lead-based technologies by January 1, 2004 [6]. This will result in either different assembly temperatures from the substitution of new solder configurations (with different melting temperatures), or the use of conducting adhesives with yet unknown high frequency characteristics.

Conclusion

The IC and PWB interconnection needs have been analyzed and compared under the purview of various technological roadmaps and an analytic model. The compatibility among IC, package and PWB technology has been thoroughly examined. It is concluded that the PWB is capable of meeting the I/O projections of the ICs for several generations in the future as forecasted in the ITRS. The PWB industry is aggressively pursuing to provide increasing wire density on substrates. It has been found that the industry is exceeding the roadmap projections of NTRS, NEMI and ITRI. To meet high I/O IC needs, a new Compliant Wafer Level Package (CWLP) under development at Georgia Institute of Technology has been briefly discussed. Complete analysis of IC – Package – PWB compatibility has been provided to address the future needs of the electronic industry.

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