Electrical Performance of Compliant Wafer Level Package

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Abstract

As the demand for portable and high speed communication products grows, wafer level packages with high chip-to-chip bandwidth and low package parasitics are required. A Compliant Wafer Level Package (CWLP) technology has been developed to meet the growing demand of higher electrical performance at low cost. The electrical performance of the compliant wafer level package in terms of its package parasitics and chip-to-chip bandwidth is investigated in this paper.

Introduction

The role of the package technology in terms of electrical performance is increasingly becoming important with rapid progress in the semiconductor technology. In the past the primary role of the package (electrically) was limited to providing an electrical connection between the chip and other functional components on the system board. However, as the switching rates of the transistors approach few pico-seconds and as the supply voltage scales down to less than 1 V, the electrical design of the package is becoming more complex and challenging. Because of high parasitics, majority of the existing package technologies are limiting the performance of the chips by introducing large delays in the path of incoming or outgoing signals. The package has to be designed to achieve higher bandwidths to enable high speed communication and computation. Modern communication applications such as ethernet and wireless communications require the package to operate in the gigahertz (GHz) frequency range. Constant scaling down of supply voltages in order to reduce the power consumption of the high-performance chips or to increase the operational time of batteries for portable electronics require the package to be able to supply electrical power to the chip without incurring significant voltage losses or fluctuations.

CWLP Technology

The Compliant Wafer Level package (CWLP) addresses the packaging and interconnections needs of the ICs by building flexible embedded leads in a compliant overcoat that extends the on chip I/O pad to the point where it can be directly attached to the system board without using an underfill. As such the entire assembly is an extension of the IC fabrication and on chip interconnections, resulting into fully packaged and tested individual ICs intact in wafer form. The wafer is diced when the functional and packaged part is needed for system assembly, eliminating yield-lowering steps of shifting and handling individual chips and packages. The CWLP uses three photolithographic masking steps as described in Fig. 1.

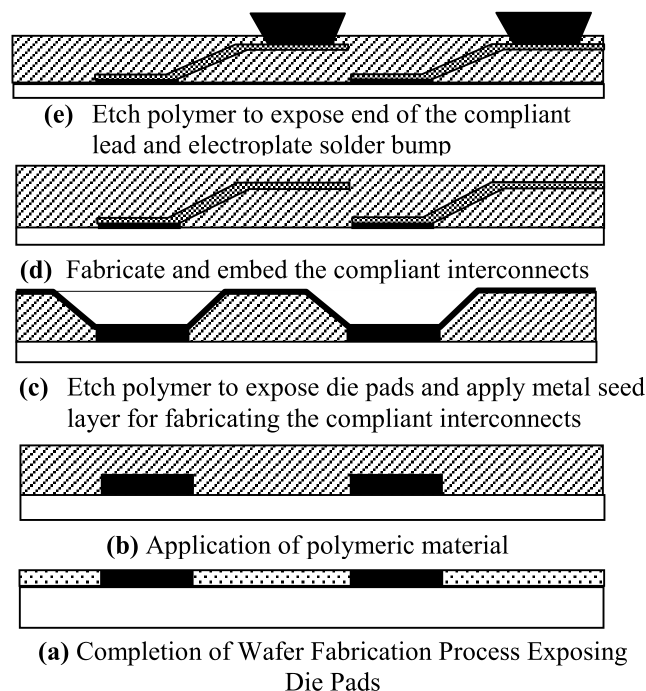
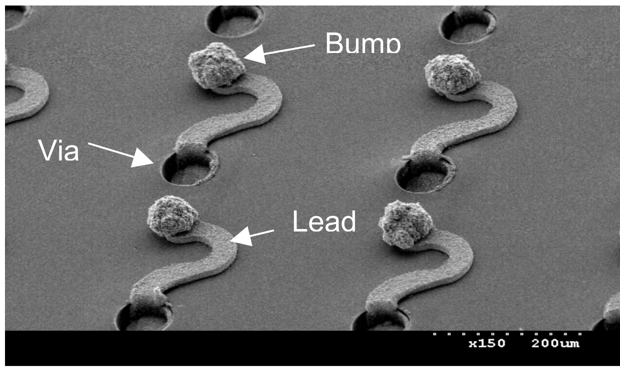
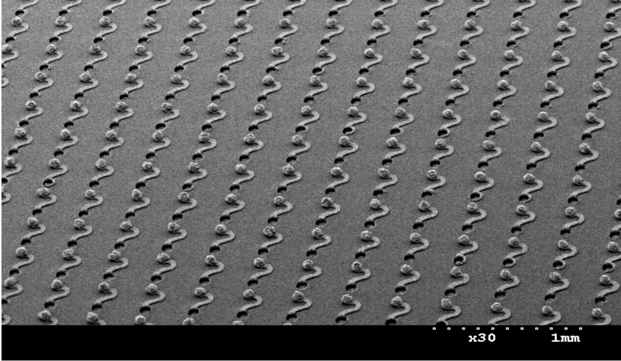


Figure 1: Compliant Wafer Level Package - Monolithic Fabrication Process Flow

A polymeric material is typically applied to the wafer to provide the function of encapsulant and low stress interposer. This material is etched using photolithography to expose the die pads on the wafer. The compliant metal interconnects, extending from the die pad to the solder bump, are fabricated by depositing a metal seed layer and electroplating with either *Cu* or *Au* to final interconnect thickness. The exposed vias are filled with polymer to embed the interconnects. The end of the metal lead is exposed and the solder bumps are electroplated for attachment to the system board. The SEM images of high density (1000 I/Os per 1 cm^2) CWLP fabricated using the lithographic process described in Figure 1 are shown in Figure 2. In this prototype, a 3-inch silicon wafer was fabricated with simple test structures that included two aluminum die pads, 75 µm by 75 µm, connected with 10 µm wide interconnect. The pads were placed at a pitch of 315 µm over 1 cm^2 die area. The prototype wafer contained total of 32 die and each die consisted of 1000 compliant I/O connections seen in Figure 2. The electrical performance of the compliant wafer level package in terms of the package parasitics and chip-to-chip communication speed are discussed in the following sections.



(a)



(b)

Figure 2: SEM image of 1000 I/Os per 1 cm ^{2} CWLP: (a) close-up image of 2 by 2 array; (b) larger array

CWLP Lead Parasitics

The electrical parasitics of the package, i.e. resistance, capacitance, and inductance, are experimentally measured and the resistance and inductance are also obtained by simulating the physical design of the compliant lead in a 3D parameter extractor software called *Raphael*, a CAD tool offered by Technology Modeling Associates (TMA).

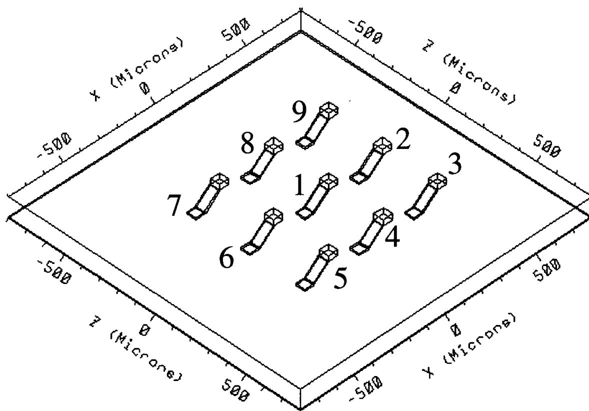


Figure 3: 3 by 3 array of compliant leads for inductance simulation

During the simulation, a 3 by 3 array of compliant leads and the corresponding setup of nodes shown in Figure 3 was used. To calculate the self and mutual inductance of the lead, a 1V input is applied to node 1. Furthermore, the I/O pitch between the leads are changed to study the effect of high density interconnects on the lead inductanace.

The self and mutual inductances of the lead as obtained from the simulation are plotted in Figure 4. The values of inductances are plotted in the units of *nano-Henry* (*nH*). The simulation was carried at a frequency of 5 GHz. To study the impact of the pitch between the compliant leads, the node-to-node pitch was varied from 100 μm to 500 μm. The self inductance of the lead was approximately 0.096 *nH* and was observed to increase minimally as the pitch was reduced.

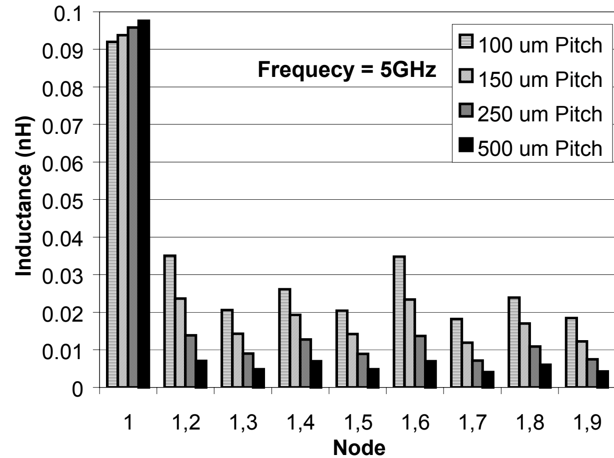


Figure 4: Self and mutual Inductance of high density CWLP leads

The notation (1, X) on the x-axis of the plot in Figure 4 corresponds to the mutual inductance between node 1 and node X, where X is all of the other nodes in the array. It is seen that the mutual inductance between node 1 and its neighboring nodes (i.e., 2,4,6,8) was more than that of diagonal nodes (3,5,7,9). Furthermore, the mutual inductance increased by factor of five as the pitch between the nodes decreased from 500 μm to 100 μm. The pitch is typically reduced to obtain high pin count, however, it is important to note that with the reduction in I/O pitch the mutual inductance between the I/Os will increase. This may weaken the electrical performance of the package. The ratio of self inductance to the mutual inductance varied from 2.6 (in case of neighboring nodes) to 5 (in case of diagonal nodes). The value of resistance obtained through simulation was 11.1 mΩ. The package parasitics were experimentally measured using an RCL four point probe meter. The experimental measurements given in Table 1 agreed well with the simulated values discussed earlier.

Table 1: High density CWLP lead parasitics

Resistance	20 mΩ
Capacitance	0.00531 pF
Inductance	0.10 nH

CWLP Chip-to-chip communication speed

An electrical model was developed to investigate the chip-to-chip communication speed or off-chip speed of the CWLP. A diagram describing the setup used in the model is shown in Figure 5. Two CWLPs can be mounted on the system board

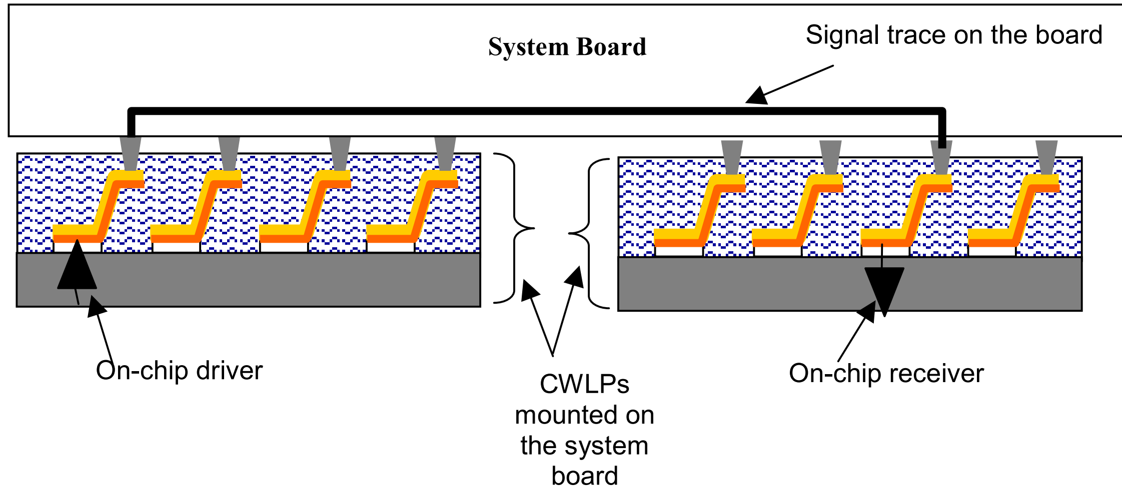


Figure 5: Diagram for modeling the chip-to-chip communication speed of the CWLP

and connected by a signal trace on a system board. The signal trace connects the I/Os of the CWLPs and enables them to communicate during functional operation. An on-chip driver transmits the signal to another chip through the transmitting package lead, trace on the board, and the receiving package lead. A circuit diagram for the off-chip model is shown in Figure 6. The off-chip speed is mainly a function of on-chip drivers, package parasitic, and board level interconnect length.

The total chip-to-chip delay is comprised of: delay through the driver chain, package parasitic, and the board interconnect length. This can be expressed in a mathematical form as:

$$T_{total} = T_{driver} + 2T_{pckg} + T_{board} \tag{1}$$

The on-chip driver is a cascaded chain of inverters with the on-resistance of the last inverter matching the line impedance, Z_o, of the package. The delay through the driver chain is given as follows [1]:

$$T_{driver} = 3e(N-1)R_{tr}C_{tr} \tag{2}$$

$$N = 1 + \frac{\left(ln\left(R_{tr}/Z_0\right)\right)}{ln(5)} \tag{3}$$

where N is the number of drivers in the cascaded chain and which is further expressed in Equation (3). The factor e Equation (2) is a mathematical e^1 and represents an optimal ratio between the size of consecutive inverters and it minimizes the delay through the driver. The factor of *3* in Equation (2) results from the sum of W/L ratios of *n*MOS and *p*MOS transistors (1 + 2 = 3). R_{tr} and C_{tr} is the output resistance and capacitance of minimum sized inverter. The derivation of the number of inverters used in the cascaded driver and size of the inverters is described in [2].

The delay through the package is modeled simply as time of flight since the resistance of the compliant lead and the signal trace is much lower than the inductance of those interconnects. As a result the delay through the package and the board is dominated by LC response or time of flight. The delay through the package and the board is expressed as

$$T_{pckg} = T_{board} = \frac{l_{int}}{v} \tag{4}$$

where l_{int} is the length of the interconnect and v is the velocity of signal through the package and the board. Equation (1) can be rewritten by incorporating all of the delay component

$$T_{total} = 3e\frac{ln\left(R_{tr}/Z_0\right)}{ln(5)}R_{tr}C_{tr} + \frac{1}{c_o}\left[2l_{pckg}\sqrt{\varepsilon_{pckg}} + l_{board}\sqrt{\varepsilon_{board}}\right] \tag{5}$$

where c_o is the speed of light in air and ε_{pckg} and ε_{board} is the relative permittivity of the dielectric material used for the CWLP and the board. To illustrate the high speed characteristic of the CWLP, the package speed is plotted as a function of the CWLP lead length in Figure 7. The low parasitics of the CWLP result into package speed in the range of THz (10^{12} Hz). The relative permittivity of the compliant material used in the CWLP is assumed to be 2.6. Higher speed is achieved as the compliant lead length is reduced. The chip-to-chip or off-chip speed expressed by Equation (5) is plotted in Figure 8 as a function of the length of the signal trace on the system board.

The parameters used in determining the off-chip speed such as R_{tr} and C_{tr} scale according to the scaling of the minimum size transistors used in the cascaded driver. In this example, the values of R_{tr} and C_{tr} are calculated for 50 nm technology generation. The relative permittivity of the system board is assumed to be 5, which corresponds to FR-4 material. It is seen in Figure 8 that the off-chip speed decreases as the signal trace length on the board is increased. The increase in signal trace length corresponds to an increase in the distance between two chips or two CWLPs on the board.

The size of the CWLP allows the system designer to place the packages closer to each other compared to conventional

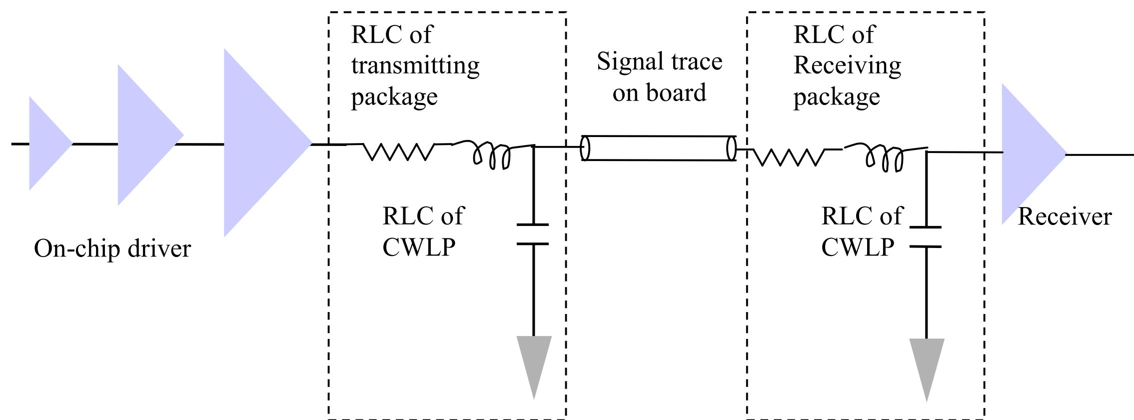


Figure 6: Circuit diagram for modeling the chip-to-chip communication speed of the CWLP

package technologies whose size is larger than the size of the chip. The CWLP can be 'tiled' on the board and hence, maximum off-chip speed can be achieved. Depending on the length of the signal trace on the board, the off-chip speed in the range of several GHz can be achieved by using CWLP.

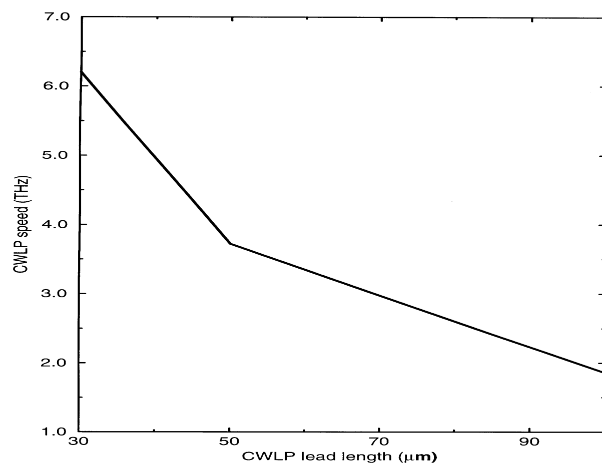


Figure 7: High density CWLP performance

Conclusions

The electrical performance of the high I/O density compliant wafer level package in terms of the package parasitics and chip-to-chip communication speed have been discussed. The self inductance of the lead was approximately 0.096 *nH* and was observed to increase minimally as the pitch between the leads was reduced. The mutual inductance between the compliant leads increased by factor of five as the pitch between the nodes decreased from 500 μm to 100 μm. The ratio of self inductance to the mutual inductance varied from 2.6 (in case of neighboring nodes) to 5 (in case of diagonal nodes). The value of resistance obtained through simulation was 11.1 mΩ. An electrical model was developed to investigate the chip-to-chip communication speed or off-chip speed of the CWLP. The total chip-to-chip delay was modeled as a function of the delay through the driver chain, package parasitic, and the board interconnect length. The low parasitics of the CWLP resulted into package speed in the range of THz (10^{12} Hz). Depending on the length of the signal trace on the board, the off-chip speed in the range of several GHz can be achieved by using CWLP.

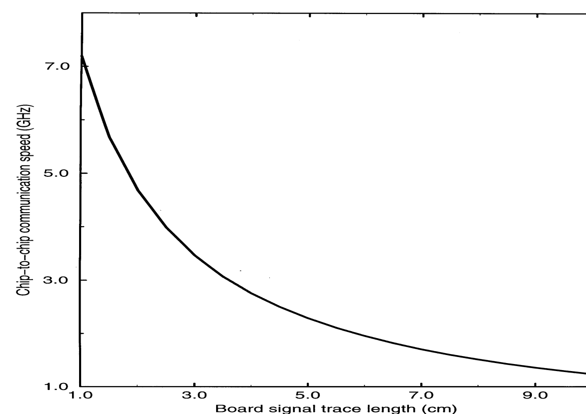


Figure 8: Chip-to-chip speed of the CWLP

References

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2. Y. P. Uyemura, *CMOS Logic Circuit Design,* Kluwer Academic Publishers, Massachusetts, 1999.