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A Compact Physical via Blockage Model

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***Abstract*—Via blockage due to signal interconnects and its impact on wirability of multi-billion-transistor chips are systematically analyzed. Via classifications are introduced. By taking advantage of a stochastic interconnect length distribution and a multi-level interconnect network architecture, a physical via blockage model exploiting channel availability is proposed. This model reveals that the most severe via blockage occurs on first metal level, wasting more than 10% and up to about 50% of wiring area. A new perspective on chip size limit imposed by via blockage is also provided by using the proposed model.**

***Index Terms*—Analysis, channel-routing, design, SLIP99: system level interconnect, system-level, via blockage.**

I. Introduction

With increasing number of interconnects and the fact that time delays of electrical signals travelling along them are approaching or even surpassing device delays [1], future multi-billion-transistor chips must account for interconnects from the beginning of the design cycle.

Initial work in designing an apriori multi-level interconnect network is based upon the Davis–Meindl interconnect length distribution [2], [3], which leads to statistically accurate apriori knowledge of what total area is *required* by all signal interconnects for desired performance. However, such design depends on *available* wiring area and therefore on the wiring efficiency factor that accounts for area consumed by power and clock networks and unused wiring area [4]. The main reasons for unused area are routing efficiency and via blockage [4]–[7]. Routing efficiency is currently *empirically* estimated from 40 to 66% [4]–[7]. Via blockage has been predicted to limit the maximum number of metal levels [5]. Therefore, it is imperative to fully understand the implications of via blockage for future chips that are predicted to have more than ten metal levels [1]. An accurate via blockage model can not only improve multi-level interconnect network design, but also potentially provide a quantitative means to characterize efficiency of CAD routing tools by decoupling via blockage and routing efficiency.

In Section II of this paper, vias are classified and their implications are systematically explored. A novel via blockage model is then proposed in Section III. Its application to future chip designs is studied in Section IV. Section V provides a new perspective on the limiting role of via blockage in chip miniaturization. Finally, main conclusions are drawn in Section VI.

II. Via Classification and Via Blockage Concept

A via is formed in the inter-level dielectric to connect metal lines on different levels. It is an inextricable component of multi-level interconnect networks. There are two different types of vias observed on chip: *terminal vias* and *turn vias*. The former serve the terminals of interconnects, while the latter are the result of routing necessity, connecting "doglegs" of interconnects. In terms of blockage, they act differently. Turn vias are essentially an internal part of an interconnect, and do not cause additional blockage to that caused by "doglegs" of interconnects. However, terminal vias do block routing of those interconnects that they interrupt. From the point of view of three-dimensional (3-D) interconnection, terminal vias are the 3-D span of interconnects, while turn vias do not propagate to other levels. As a result, only terminal vias need to be considered in the impact of vias on wiring efficiency.

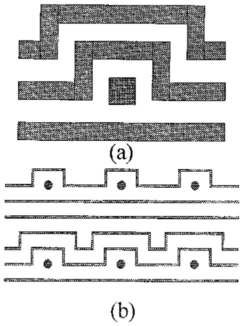

Fig. 1. Illustration of ripple effect.

As terminal vias link interconnects with the silicon surface, they cause blockage at all levels in between. Their *explicit* impact can be estimated through their physical footprint area [8], but their *implicit* impact may go far beyond that. The reason is that vias may force interconnects to detour [Fig. 1(a)], and detouring interconnects force others to detour even further, like a ripple. The average interconnect length (L_{avg}) can be a useful criterion in this situation. If the density of vias is so small ("*sparse vias*") that the average inter-via distance is much larger than L_{avg}, the majority of interconnects can be routed without encountering vias at all. In such case via blockage is limited to their footprint area, which will hardly affect routing. However, when the density of vias is large ("*dense vias*") such that their average distance is less than L_{avg}, the ripple effect is accentuated which causes the area penalty of each via to increase dramatically. In future chips, one can expect to have to deal with dense vias rather than sparse ones.

Different routing techniques use "channels" in both tangible and intangible form (in software) as the resources to place interconnects [9]–[11]. Channels consist of wiring tracks along which interconnects are placed so that they do not overlap each other. Because of the way dense vias cause blockage, their impact can be approximated through wiring track availability by lining up vias [Fig. 1(b)]. When a potential wiring track is congested by dense vias, it is no longer available as a resource for routing tools to use.

III. Main Assumptions and Results

Before proceeding to analytical expressions for via blockage, several key assumptions need to be made:

1) All terminal vias are distributed across the chip uniformly as in a grid with uniform distances between them.
2) X–Y orthogonal metal levels are used pair-wise.
3) Every interconnect is placed on a pair of X–Y metal levels exclusively based on its length.

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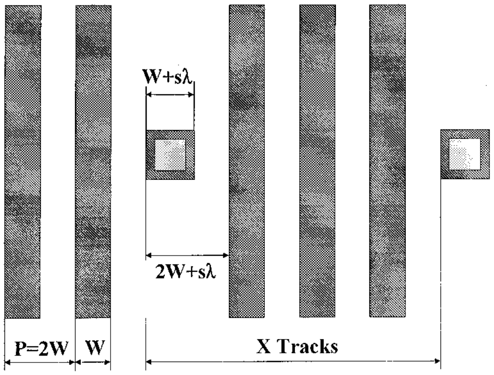

Fig. 2. Via blockage factor derivation.

4) Both terminals of an interconnect can be located on either upper or lower levels (i.e. X- or Y- level) of a wiring pair with equal probability.
5) Power lines are uniformly and equally distributed over all layers. The area used by clock lines is small enough to be ignored [5], [12].

From Assumption 3, every interconnect on the nth wiring pair has two terminal vias in each underlying level, but does not have impact on the upper level of nth pair, while giving two vias to its lower level with probability 0.5 (Assumption 4). Therefore, the number of terminal vias N_V for a metal level can be found as the following:

1) For the upper level of the nth wiring pair

$$N_v = 2[I(L_{\max}) - I(L_n)]. \tag{1}$$

2) For the lower level of the nth wiring pair

$$N_v = 2I(L_{\max}) - I(L_n) - I(L_{n-1}) \tag{2}$$

where

$L_{\max}$	longest on-chip interconnect length;
L_n	longest interconnect length placed on the nth wiring pair [3];
$I(l)$	cumulative interconnect density function [2] that gives the number of interconnects with length less than or equal to l.

For a given metal level the via blockage factor B_V is defined as

$$B_v = A_v/A_c \tag{3}$$

where A_V is the unused wiring area due to vias, and A_C is the chip area. (3) can be modified to

$$B_v = B'_v(A_{\text{eff}}/A_c) \tag{4}$$

where

$$B'_v = A_v/A_{\text{eff}} \tag{5}$$

and A_{eff} is the area left after removing the areas used by power (A_{PS}) and clock (A_{CLK}) lines. In terms of available wiring tracks (Fig. 2) B'_V can be expressed as follows:

$$B'_v = (2W + s\lambda)/(2WX + s\lambda) \tag{6}$$

where

W	interconnect width on a given level and assumed to be half of the interconnect pitch;
s	via covering factor;
λ	layout rule unit which is usually equal to half of the minimum feature size;
X	number of available tracks between neighboring vias plus one (Fig. 2).

It characterizes the average inter-via distance in interconnect pitches. X can be determined from (Assumptions 1 and 5)

$$\sqrt{N_v}[(X-1)2W + (2W + s\lambda)] = A_{\text{eff}}/\sqrt{A_c}. \tag{7}$$

TABLE I
MULTI-LEVEL INTERCONNECT ARCHITECTURE DESIGNS [13]

Multi-tier Design: A_C=1.79cm^2; Frequency: f_C=2GHz

Metal Level	8/7	6/5	4/3	2/1
Pitch, μm	1.78	0.94	0.45	0.2
L_n, gate pitch	7043	1862	887.7	209.6

Three-tier Design: A_C=0.70cm^2; Frequency: f_C=578MHz

Metal Level	8/7	6/5	4/3	2/1
Pitch, μm	0.60	0.31	0.2	0.2
L_n, gate pitch	7043	1832	481	49.9

Then, the final expression for via blockage factor is

$$B_v = \sqrt{N_v(2W + s\lambda)^2/A_c} \tag{8}$$

which illustrates that a larger number of vias (N_V), smaller chip size (A_C), and a larger interconnect pitch ($2W$) lead to an increase in via blockage.

It is interesting to note that the terms under the square root in (8) are equal to the ratio of via to chip area, which is the blockage factor for sparse vias. Given that B_V is always less than unity, (8) shows that using only footprint area to assess via blockage for *dense vias* yields a substantial underestimate due to the ripple effect of vias that is described in Section II. Even though (8) is expected to give a more realistic estimate of via blockage, it may still tend to underestimate the problem because the proposed via blockage model assumes ideal lining up of vias, which may not be observed in real designs.

IV. CASE STUDY

Both three-tier and multi-tier interconnect network design examples from [13] are taken for case study. The longest interconnects at all levels, determined in these designs, are shown in Table I for convenience.

As the first step to study via blockage in these designs, the average interconnect length (L_{avg}) on each wiring pair is calculated as

$$L_{\text{avg}} = \int_{L_{n-1}}^{L_n} i(l)l\,dl/[I(L_n) - I(L_{n-1})] \tag{9}$$

where $i(l)$ is the interconnect density function [2], and compared to the average inter-via distance (X) on each level (Table II), which is found by using (7) and assuming $s = 3$ [8] and $A_{PS}/A_C = 0.2$ [5]. Table II shows that an average interconnect can span from several to more than 100 vias, confirming that dense vias are encountered in future chips.

Therefore, by using (8) via blockage factors are found and shown in Fig. 3. A significant message from Fig. 3 is that via blockage is severe only on the lowest metal levels, especially on the first one. It can be explained by two factors: one is that in multi-level interconnect networks the overwhelming portion of (short) interconnects is placed on local levels that must also accommodate the overwhelming portion of vias. Another is that interconnect pitch increases from local to global levels much more slowly than the number of interconnects placed at each level decreases, leading to increasingly smaller via density at higher levels.

Via blockage factors are also compared against that calculated using the methodology [6] that is based on [5] (Fig. 3). While the via blockage model in [5] is only concerned about the number of metal levels, the new model additionally takes account of chip

TABLE II
AVERAGE INTERCONNECT LENGTH VERSUS AVERAGE INTER-VIA DISTANCE (BOTH EXPRESSED IN INTERCONNECT PITCHES)

Level	8	7	6	5	4	3	2	1
A_C =1.79cm^2								
X	n.a	50	67	41	67	36	63	8
L_{avg}	5425		5013		3379		145	
A_C =0.70 cm^2								
X	n.a.	91	124	53	61	26	20	5
L_{avg}	9951		6554		1592		59	

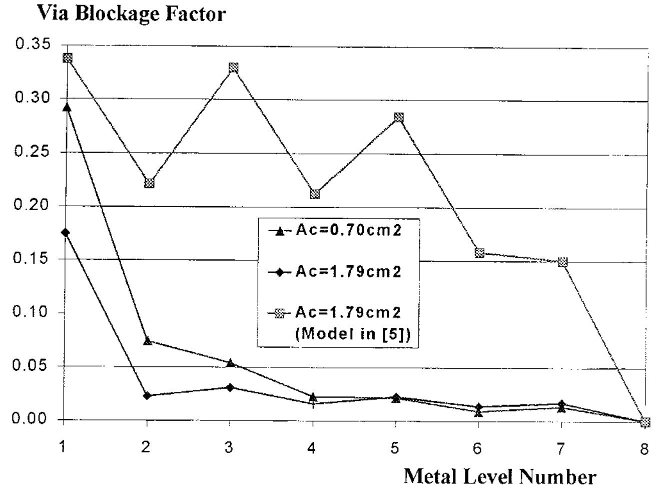

Fig. 3. Via blockage factor distribution.

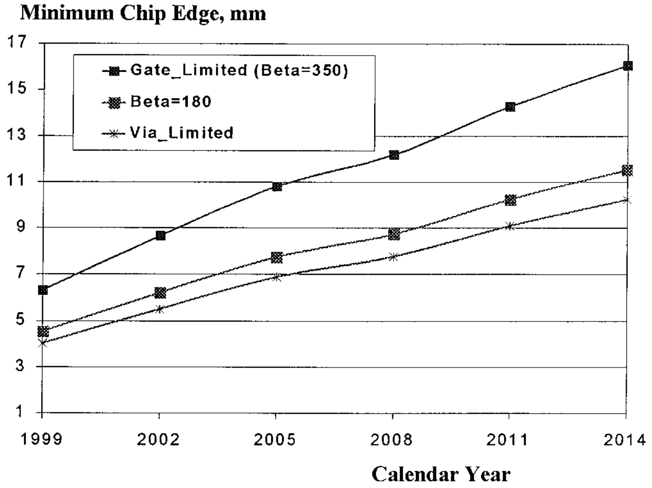

Fig. 4. Minimum chip size in millimeters versus calendar year.

area in estimating via blockage. Although adding one more metal level elevates some number of interconnects to higher levels, their number and the number of associated vias is very small compared to interconnects remaining at lower levels. This is true because the Davis–Meindl interconnect length distribution indicates that the number of interconnects decreases very quickly with length. However, the chip size shrinkage, which benefits from more metal levels, causes a remarkable rise in via density, thus in via blockage. Therefore, *chip size*, rather than *number of metal levels*, should be considered as the direct cause for potentially severe via blockage problems. The newly proposed model is capable of making such estimates and predictions.

V. VIA BLOCKAGE IN FUTURE CHIPS

Via blockage has been assumed a pivotal factor that could inhibit multi-level metallization and/or chip miniaturization [5]. Based on the novel via blockage model, it is investigated when chip size becomes via-limited and how big it is.

The limit on chip size imposed by vias definitely will occur on the first level that has the most severe via blockage. Figs. 1(b) and Fig. 2 intuitively suggest that $X = 2$ corresponds to the ultimate via distribution for feasible wiring. Any further decrease in X, equivalent to any increase in via density, will make routing virtually impossible. Therefore, the first metal level of a via-limited chip must be characterized by

$$B'_{v,\max} = (2W + s\lambda)/(4W + s\lambda). \tag{10}$$

If $s = 3$, $B'_{v,\max}$ becomes 63.6% with $\lambda = W/2$ on the first level.

If the chip edge is denoted by $D = \sqrt{A_c}$, then the via-limited chip size can be found using (4) and (8)

$$D_{\min} = (A_c/A_{\text{eff}})(2W + s\lambda)\sqrt{N_v}/B'_{v,\max}. \tag{11}$$

By approximating $I(L_1) \approx I(L_{\max})$, the number of vias on the first level can be estimated by

$$N_v \approx I(L_{\max}) \tag{12}$$

where

$I(L_{\max})$	$= \alpha k N(1 - N^{p-1})$ [14];
N	number of gates;
k	Rent's coefficient;
p	Rent's exponent;
α	factor determined by fan-out.

By assuming $A_{PS}/A_C = 0.2$ [5], six transistors per gate, $a = 0.75$, $k = 4$, and $p = 0.6$ [3], via-limited chip size is predicted for future generations from [1]. It is compared against gate-limited chip size (Fig. 4), which is determined as $\sqrt{N(\beta F^2)}$, where β is the numerical factor describing average gate area in minimum feature size squares (F^2). β can be estimated by using the gate area model in [6] for custom or standard cell design. For transistor aspect ratios of 1.5 and 10, β is about 180 and 350, respectively. Fig. 4 shows that the chip size limited by gate area with smallest transistor aspect ratio of 1.5 is still about 10% larger than via-limited chip size.

VI. CONCLUSION

Via blockage and its impact are systematically studied. A novel compact model of via blockage based on physical parameters of a chip is proposed. Applicability of this model is established. This new model reveals that the via blockage factor on the first metal level is as high as 10% to about 50%, while via blockage at higher levels is much smaller. A new perspective on the limiting role of via blockage in chip miniaturization is provided.

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