

Physics-Based Device Models for Nanoscale Double-Gate MOSFETs

Qiang Chen*, Lihui Wang, and James D. Meindl

Microelectronics Research Center, Georgia Institute of Technology
791 Atlantic Dr. N.W., Atlanta, GA 30332-0269, U.S.A.

*Advanced Micro Devices, One AMD Place, MS 79, Sunnyvale CA 94088, USA, qiang.chen@amd.com

ABSTRACT

Compact, physics-based models of subthreshold swing and threshold voltage are presented for undoped double-gate (DG) MOSFETs in symmetric, asymmetric, and ground-plane modes of operation. Applying the new device models, a novel scale-length based methodology is demonstrated to comprehensively and exhaustively investigate threshold voltage variations in DG MOSFETs. In light of ultra-thin silicon film used as the channel and possible introduction of high-permittivity gate dielectrics, physical, analytical models of quantum mechanical effects, gate direct tunneling current, and fringe-induced barrier lowering effect are developed to assess their impact on DG MOSFET scalability. Scaling limits projections indicate that individual DG MOSFETs with good turn-off behavior are feasible at 10nm scale; however, practical exploitation of these devices toward gigascale integrated systems requires significant improvement in process control.

I. INTRODUCTION

The double-gate (DG) MOSFET, illustrated in Figure 1, has been considered as the most promising device structure to extend CMOS scaling into the nanometer regime [1]. The ultra-thin silicon channel is undoped (i.e., lightly doped with the background doping concentration less than 10^{16} cm^{-3}) to avoid random dopant fluctuation and mobility degradation associated with heavy doping. Depending upon gate work functions and gate-bias conditions, a DG MOSFET can operate in symmetric (SDG), asymmetric (ADG), or ground-plane (GP) modes. Two key characteristics of a MOSFET, namely, subthreshold swing (S) and threshold voltage (V_{TH}), and their dependences on device parameters are usually exploited to gauge the device's immunity to short-channel effects (SCE), i.e., its scalability. In this paper, compact, physics-based models of subthreshold swing and threshold voltage are described for symmetric, asymmetric, and ground-plane DG MOSFETs, including quantum mechanical effects and fringe-induced barrier lowering (FIBL) effect. These new device models are applied to comprehensively analyze parameter variations, reveal device design insights, and project scaling limits and opportunities of DG MOSFETs.

II. SUBTHRESHOLD SWING MODELS

Under the full-depletion condition, a two-dimensional (2-D) Poisson equation with the dopant term only is solved using the evanescent-mode analysis in the channel region to obtain the channel potential distribution [2]. It is then

assumed that the drain current is proportional to the *sheet* density of inversion carriers at the virtual cathode (i.e., the minimum potential point between the source and drain). Such an approach eliminates the uncertainty of choosing the most representative leakage path (channel surface versus channel center [3, 4]) for subthreshold swing calculations, and leads to the following general model [5],

$$S = \left[\int_{y=-t_{Si}/2}^{t_{Si}/2} n_m(y) \frac{\partial \varphi_{\min}(y)}{\partial V_{GS}} dy / \int_{y=-t_{Si}/2}^{t_{Si}/2} n_m(y) dy \right]^{-1} \frac{kT}{q} \ln 10, \quad (1)$$

where V_{GS} is the gate voltage, $n_m(y) = n_i \exp[\varphi_{\min}(y)q/kT]$, n_i is the intrinsic electron concentration, $\varphi_{\min}(y)$ is the potential profile at the virtual cathode.

Although undoped devices are of most interest in this study, a detailed analysis exploiting (1) of subthreshold swing's dependence on the channel doping concentration [2] reveals that subthreshold swing in short-channel DG MOSFETs can be closely described by a concept of effective conducting path, i.e., its location with respect to the gate, d_{eff} . The closer the effective conducting path is to the switching gates, the better (i.e. smaller) is the subthreshold swing. And (1) can be simplified as [5]

$$S = \left[1 - 2\Gamma_1 \frac{(V_1 + V_{DS}/2) \cos \frac{d_{eff}}{\lambda_1} e^{-\frac{L}{2\lambda_1}}}{\sqrt{V_1(V_1 + V_{DS})}} \right]^{-1} \frac{kT}{q} \ln 10, \quad (2)$$

for both SDG and ADG devices, and

$$S = \left[\frac{1}{2} - \frac{r}{r+2} \frac{d_{eff,linear}}{t_{Si}} - \Gamma_1 \frac{V_1 + V_{DS}/2}{\sqrt{V_1(V_1 + V_{DS})}} \cos \frac{d_{eff}}{\lambda_1} e^{-\frac{L}{2\lambda_1}} \right]^{-1} \frac{kT}{q} \ln 10, \quad (3)$$

for GP devices, where $r = \epsilon_{Si} t_{ox} / \epsilon_{ox} t_{Si}$. The parameter λ_1 is a scale length and can be approximated as [2],

$$\lambda_1 = \frac{t_{Si} + \epsilon_{Si} t_{ox} / \epsilon_{ox}}{1 + \pi/2} \quad \text{or} \quad \lambda_1 = \frac{t_{Si} + \sqrt{2} \epsilon_{Si} t_{ox} / \epsilon_{ox}}{\sqrt{2} + \pi/2}, \quad (4)$$

for $r \leq \pi/2$ and $r > \pi/2$, respectively. It provides an efficient guideline in selecting appropriate t_{ox} and t_{Si} values for device designs.

In undoped symmetric DG devices, the effective conducting path is found in-between the channel surface and the channel center (i.e., $d_{eff} \approx t_{Si}/4$) because of the volume inversion effect, which results from symmetry and the minuscule amount of ionized dopant atoms [2]. Consequently, (2) can be further simplified for SDG devices without comprising much accuracy [2],

$$S = \left[1 - 2\Gamma_1 \frac{(V_1 + V_{DS}/2) \cos \frac{t_{Si}}{4\lambda_1} e^{-\frac{L}{2\lambda_1}}}{\sqrt{V_1(V_1 + V_{DS})}} \right]^{-1} \frac{kT}{q} \ln 10. \quad (5)$$

The new S model is compared to previous models and Medici numerical simulations with improved agreement (Figure 2). Ideal subthreshold swing is achieved at large

channel-lengths, which is explained by ideal gate-to-gate coupling through the dielectric-like undoped channel [6].

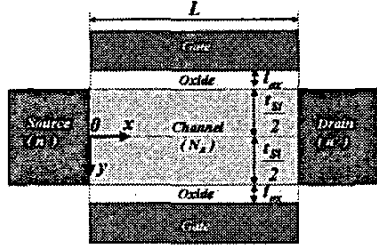


Figure 1: Cross-section schematic of a DG MOSFET.

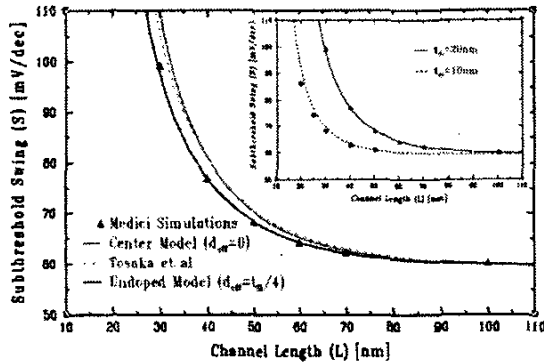


Figure 2: S roll-up in undoped SDG MOSFETs [2].

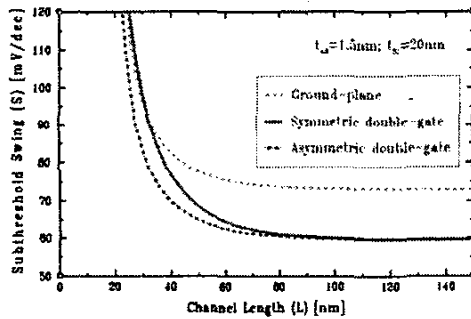


Figure 3: Comparison of subthreshold swing in SDG, ADG, and GP MOSFETs [5].

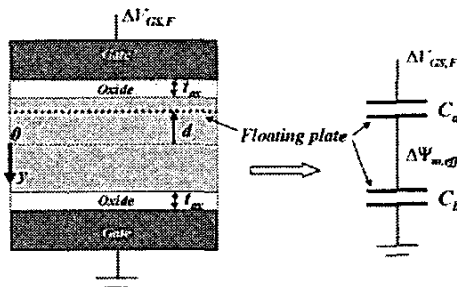


Figure 4: Capacitor divider concept for GP MOSFETs [5].

For asymmetric DG MOSFETs, d_{eff} is a more complex and sensitive function of gate work-functions and device geometry than in SDG devices [5]. In general, because of asymmetric channel potential profile, the effective conducting path in ADG MOSFETs is found to be closer to the gate than in symmetric devices of the same geometry, resulting in a stronger gate control over the channel, and consequently, a slightly smaller S (Figure 3). The improved subthreshold swing of ADG devices may translate into a higher drive current than in SDG ones for a normalized off-current.

The subthreshold swing behavior in GP MOSFETs can be comprehended by the effective conducting path in combination with the capacitor divider model [5] (Figure 4), where the effective conducting path acts as a floating plate in series-connected capacitors. For long-channel and moderately short-channel designs, GP MOSFETs demonstrate a significantly larger subthreshold swing than both SDG and ADG devices (Figure 3).

III. THRESHOLD VOLTAGE MODELS

It has been observed that the concentration of inversion carriers can exceed that of ionized dopant atoms under the threshold condition in undoped devices [7, 8, 9, 10]. Exclusion of inversion carriers from consideration leads to noticeably overestimated channel potential (Figure 5), and consequently undervalues threshold voltage. Moreover, the conventional way of using the surface band bending equal to $2q\phi_B$, where $\phi_B = \ln(N_A/n_i)kT/q$, to define the threshold condition becomes irrelevant. An alternative is to define the threshold voltage as the gate voltage at which the sheet density of inversion carriers reaches a value of Q_{TH} adequate to identify the turn-on condition [11]. Such a definition is equivalent to the constant-current V_{TH} measurement widely used in both experiments and simulations.

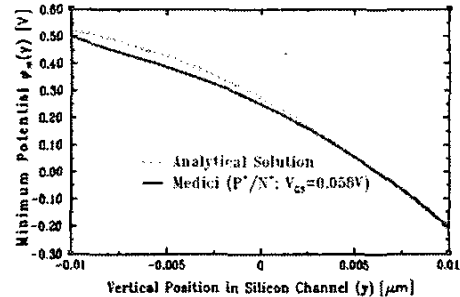


Figure 5: Channel potential at the virtual cathode under the threshold condition: Medici simulations vs. analytical solution of 2-D Poisson equation with the dopant term only. ($t_{ox}=1.5\text{nm}$, $t_s=20\text{nm}$, $L=30\text{nm}$) [5].

III.1 Symmetric DG MOSFETs

A 2-D Poisson equation with only the mobile charge term included is analytically solved in the near-threshold region for SDG MOSFETs [11]. The potential profile at

the virtual cathode is then determined, which, through the sheet density of inversion carriers, leads to a general short-channel threshold voltage model [11],

$$V_{TH} = \Phi_{MS,i} + \eta \frac{kT}{q} \frac{\cosh(\theta)}{\cosh(\theta/2)} \ln\left(\frac{Q_{TH}}{n_i t_{Si}}\right) - \left[\frac{\cosh(\theta)}{\cosh(\theta/2)} \eta - 1 \right] \phi_{0m}, \quad (6)$$

where $\Phi_{MS,i}$ is the gate work-function referenced to the intrinsic silicon. At large channel lengths, (6) readily reduces into a long-channel V_{TH} model for $\theta \rightarrow 0$ and $\eta \rightarrow 1$,

$$V_{TH, long} = \Phi_{MS,i} + \frac{kT}{q} \ln\left(\frac{Q_{TH}}{n_i t_{Si}}\right). \quad (7)$$

Models (7) and (6) are compared with published FIELDAY numerical simulations [12] with close agreement (Figure 6 and Figure 7). The slight dependence of long-channel V_{TH} on t_{Si} is caused by the volume inversion effect [11].

Applying the new model (6), it was discovered [11] that the normalized V_{TH} sensitivities, $\delta V_{TH}/(\delta X/X)$, where X stands for L , t_{Si} , or t_{ox} , and $\delta X/X$ is its process tolerance expressed in percentage, can be represented, with reasonably good accuracy, by three unified, unique functional dependences on L/λ_1 for virtually all (L , t_{Si} , t_{ox}) designs (Figure 8). It enables a convenient and exhaustive study of the impact of process variations across technology nodes. For practical device designs (with L/λ_1 around ~ 4.5 to ~ 7) L causes 30% to 50% more V_{TH} variation than does t_{Si} for the same process tolerance, while t_{ox} causes the least, relatively insignificant amount of V_{TH} variation.

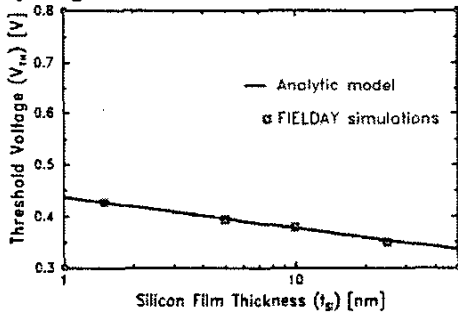


Figure 6: Long-channel V_{TH} vs. t_{Si} in SDG MOSFETs. Mid-gap gates are assumed [11].

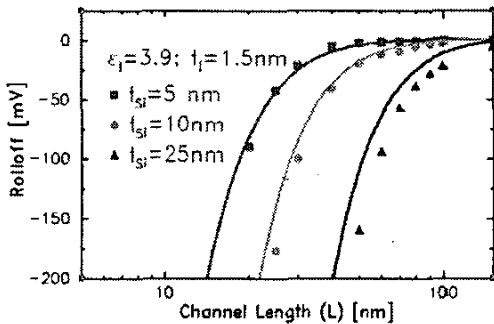


Figure 7: V_{TH} rolloff in undoped SDG MOSFETs: model vs. FIELDAY simulations [11].

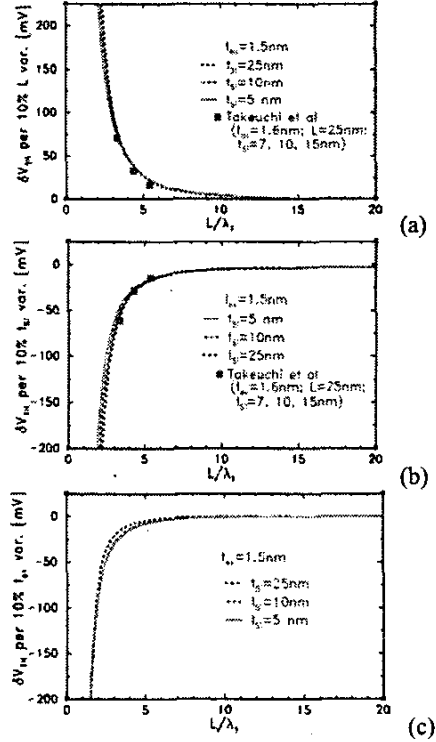


Figure 8: V_{TH} change versus the ratio of L/λ_1 caused by 10% increase of (a) L , (b) t_{Si} , and (c) t_{ox} , respectively [11].

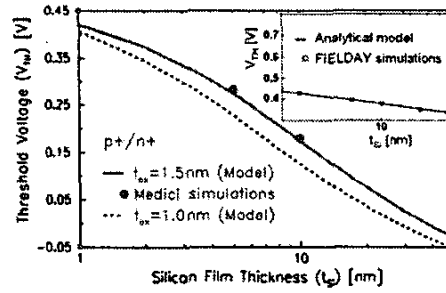


Figure 9: Long-channel V_{TH} vs. t_{Si} in p+/n+ ADG. The inset is for mid-gap SDG (Figure 6) [13].

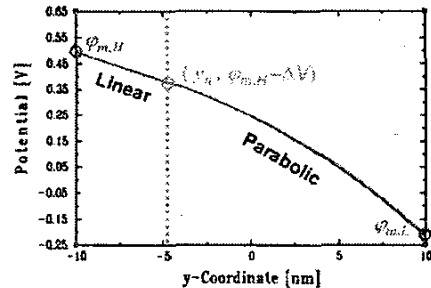


Figure 10: Bi-sectional approach to potential calculations at the virtual cathode in short-channel ADG MOSFETs [5].

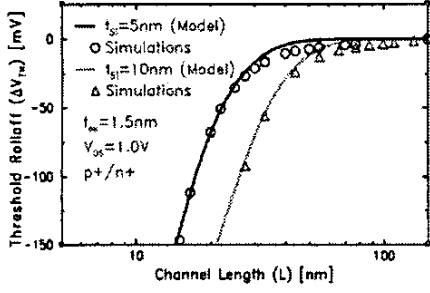


Figure 11: V_{TH} rolloff in p+/n+ ADG devices: model vs. Medici simulations [13].

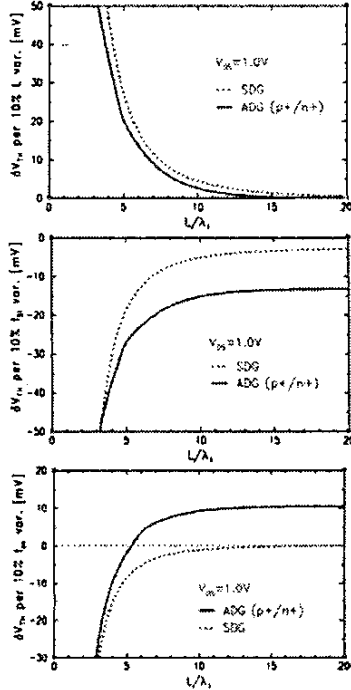


Figure 12: V_{TH} change per 10% increase of L , t_{Si} , and t_{ox} , respectively: p+/n+ asymmetric vs. symmetric devices [13].

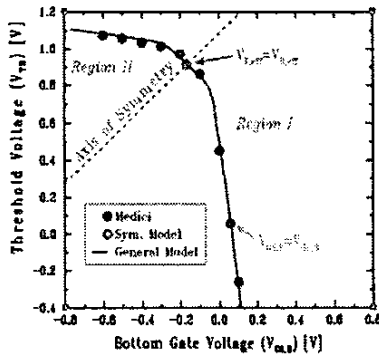


Figure 13: V_{TH} versus constant-bias gate voltage. $t_{Si}=20$ nm, $t_{ox}=1.5$ nm, and $L=30$ nm with p+/n+ polysilicon as front and bottom gates, respectively [5].

III.2 Asymmetric DG MOSFETs

The long-channel V_{TH} model for asymmetric devices is obtained by taking advantage of the linearity of the potential profile at the virtual cathode [13],

$$V_{TH} = \frac{1}{\beta} \ln \left(\frac{Q_{TH}}{n_i t_{Si}} \right) + \frac{1}{\beta} \ln \left(\frac{r}{r+2} \beta \Phi_{MM} \right) + \frac{\Phi_{FMJ} + \Phi_{BMJ}}{2} - \frac{r}{2(r+2)} \Phi_{MM} \quad (8)$$

Long-channel ADG MOSFETs exhibit a much stronger V_{TH} dependence on t_{Si} than their symmetric counterparts, and have a noticeable V_{TH} dependence on t_{ox} as well (Figure 9). Both dependences are well explained by the strong electric field in the channel thickness direction, similarly to bulk MOSFETs [13].

To alleviate analytical calculations of channel potential in short-channel asymmetric devices with mobile carriers taken into account, a bi-sectional approach is undertaken [5], which is based on observations that the potential profile at the virtual cathode can be partitioned into a linear region and a parabolic region (Figure 10), and the lower end of this distribution is closely described by the 2-D Laplace equation. As a result, a simple, although explicit, short-channel V_{TH} model is obtained [13],

$$V_{TH} = \Phi_{MS..F} + \phi_{MAX} + (kT/q) n_i t_{Si} \exp(q\phi_{MAX}/kT) / Q_{THr} \quad (9)$$

Model (9) is compared to Medici simulations with close agreement (Figure 11).

Applying the scale-length based V_{TH} variation analysis technique, V_{TH} sensitivities in ADG MOSFETs are investigated and compared to those in SDG devices (Figure 12). For practical designs of p+/n+ ADG devices, t_{Si} causes 35% to 100% more V_{TH} variation than L does for the same process tolerance. While ADG devices show a slightly smaller sensitivity to L than SDG devices, they may be more prone to t_{Si} and t_{ox} variations, particularly, in relatively long-channel designs.

III.3 Ground-plane MOSFETs

In GP MOSFETs, the threshold voltage essentially represents a pair of signal-gate voltage and constant-bias voltage [5]. Depending upon the gate voltage combinations, the potential profile under the threshold condition can be strongly asymmetric, moderately asymmetric, or symmetric. Therefore, the threshold voltage model for GP MOSFETs is developed as a hybrid of V_{TH} models for symmetric and asymmetric devices (Figure 13). Region I seen in Figure 13 is undesirable because of very weak control of the signal gate over the channel, which is explained by the fact that strong inversion is formed along the channel surface near the constant-bias gate. The moderate dependence of V_{TH} on constant-bias voltage found in Region II may be exploited to compensate for process induced V_{TH} variations.

IV. SCALING LIMITS PROJECTIONS

Scaling limits of DG MOSFETs are projected on the example of symmetric devices based on three scaling criteria: 1) an excellent turn-off behavior of $S=70$ mV/dec,

2) a moderate turn-off behavior of $S=100$ mV/dec, and 3) 70 mV maximum V_{TH} change caused by 30% L -equivalent process tolerance (to which all process variations are converted) [11]. As seen in Figure 14, individual DG MOSFETs with satisfactory turn-off characteristics are feasible with L as short as ~ 10 nm (~ 12 nm for $S=70$ mV/dec and ~ 7 nm for $S=100$ mV/dec). However, V_{TH} control, which is needed for gigascale integration of these devices, presents the biggest challenge for scaling, allowing L to be reduced only to ~ 16 nm.

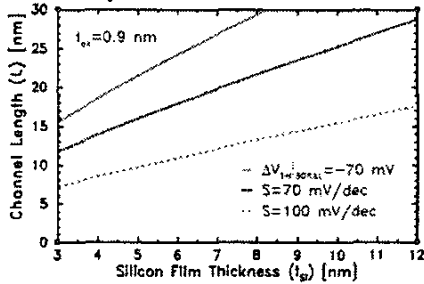


Figure 14: Scaling limits: L versus t_{Si} . [11].

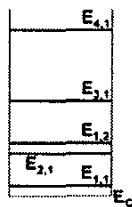


Figure 15: Subbands in nanoscale Si channel [14].

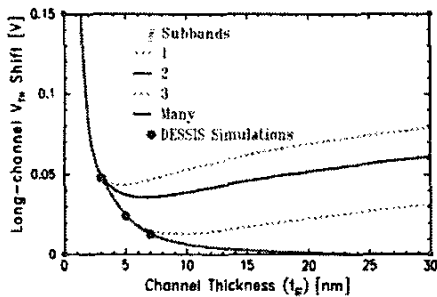


Figure 16: QM vs. classic long-channel threshold voltage shift versus silicon channel thickness [14].

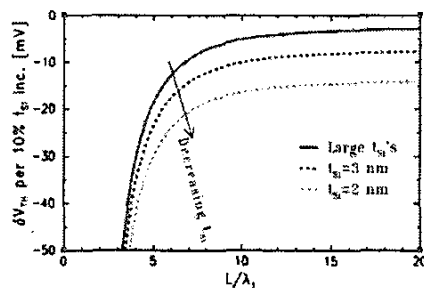


Figure 17: Overall V_{TH} change per 10% t_{Si} increase [14].

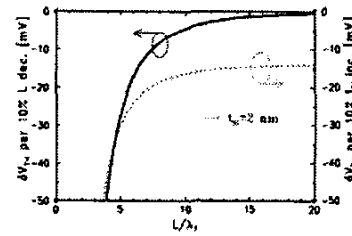


Figure 18: Overall V_{TH} change per 10% decrease of L (left) vs. that per 10% increase of t_{Si} (right) as unified functions of L/λ_1 [14].

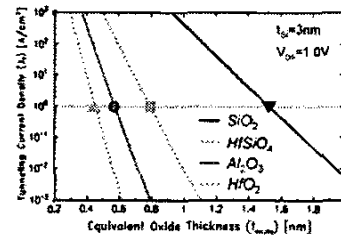


Figure 19: Gate direct tunneling current density vs. equivalent oxide thickness (EOT) [16].

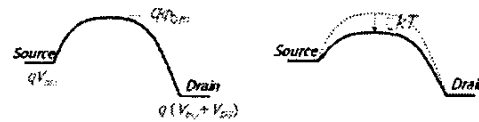


Figure 20: FIBL effect: energy band diagram along the channel with thin (left) and thick (right) gate dielectrics.

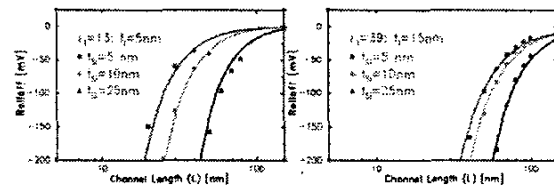


Figure 21: V_{TH} rolloff with different dielectric permittivity values in a variety of device designs [16].

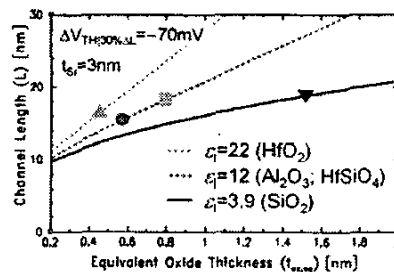


Figure 22: L versus EOT. Symbols mark minimum L 's determined by minimum EOTs (allowed for gate tunneling current): \blacktriangledown - SiO_2 ; \boxtimes - HfSiO_4 ; \bullet - Al_2O_3 ; \blacktriangle - HfO_2 [16].

V. QUANTUM MECHANICAL EFFECTS

It becomes clear in Figure 14 that 10 nm DG MOSFETs require ultra-thin silicon channel around 3 nm and ultra-thin gate oxide around 1 nm. Carrier confinement in such a thin silicon film becomes significant, leading to energy quantization (Figure 15) and carrier re-distribution. Taking into account both the band structure of silicon and the quantization effect, a quantum mechanical threshold voltage model has been developed for symmetric DG MOSFETs [14],

$$\Delta V_{TH} = \frac{E_g}{2q} + \frac{kT}{q} \ln(n_i t_{Si}) - \frac{kT}{q} \ln \left[\sum_{i=1}^2 g_i \frac{m_{D,i}^*}{\pi \hbar^2} kT \sum_j \exp\left(-\frac{E_{j,i}}{kT}\right) \right], \quad (10)$$

which represents the QM vs. classic threshold voltage shift. Parameter E_g is the band gap in Si, g_i 's are degeneracy factors $g_1=2$ and $g_2=4$, $m_{D,i}^*$ ($i=1,2$) are density-of-states (DOS) effective masses of an electron, given as $m_{D,1}^*=m_i^*$, and $m_{D,2}^*=(m_l^* m_t^*)^{1/2}$, where m_l^* and m_t^* are longitudinal and transverse effective masses of an electron, respectively. Parameter $E_{j,i}$ is the j -th subband in the i -th group of valleys, and is obtained by using the infinite-well approximation thanks to the weak coupling between the Poisson and Schrödinger equations,

$$E_{j,i} = \frac{j^2 (2\pi\hbar)^2}{8m_{m,i}^* t_{Si}^2} \quad (11)$$

where \hbar is the reduced Plank constant, $m_{m,i}^*$ are motion effective masses of an electron given as $m_{m,1}^*=m_l^*$ and $m_{m,2}^*=m_t^*$. Model (10) is compared to DESSIS numerical simulations with close agreement (Figure 16). In general, multiple subbands are needed for model calculations. As t_{Si} decreases below 3 nm, quantization becomes so strong that the lowest subband alone seems to suffice. Quantum mechanical effects dramatically increase V_{TH} 's sensitivity to t_{Si} as it decreases (Figure 17), and t_{Si} outgrows L as the largest source of parameter variations at $t_{Si}=2$ nm (Figure 18).

VI. IMPACT OF HIGH-K DIELECTRICS

The gate direct tunneling current increases exponentially as t_{ox} is reduced, and constitutes a considerable portion of the overall power consumption for t_{ox} smaller than 2nm. The tunneling probability of mobile carriers across the oxide layer can be obtained by solving Schrödinger equations in the channel/oxide/gate regions and applying a rectangle-barrier approximation,

$$D(E_y) = \exp\left(-\gamma\sqrt{E_B - E_y}\right), \quad (12)$$

where E_y is the carrier's energy in the tunneling direction, E_B is the average barrier height $E_B = \chi - q(V_{GS} - \Phi_{MSI} - \varphi_S)/2$, φ_S is surface potential with respect to the source Fermi level, χ is conduction band offset of gate oxide with respect to Si, $\gamma = 4\pi f(2m_i)^{1/2}/\hbar$, m_i is the carrier's effective mass in oxide, t_i is the thickness of gate oxide. The gate direct tunneling current density is then obtained as the net result of channel-to-gate and gate-to-channel tunneling components,

$$J_T = \frac{4\pi m_i^* q}{h^3} \int_0^{\infty} \left[f_s(E_y + E_t) - f_m(E_y + E_t) \right] D(E_y) dE_y dE_t, \quad (13)$$

where E_t is the carrier's energy transverse to the tunneling direction, and $E_y + E_t$ represents the carrier's total energy, f_s and f_m are occupancy probability functions in the silicon channel and gate, respectively. Under the strong inversion condition, (13) further reduces to [15],

$$J_T = \frac{4\pi m_i^* q}{h^3} (kT)^2 \left(1 + \frac{\gamma kT}{2\sqrt{E_B}} \right) \exp\left(\frac{q\varphi_S - E_g/2}{kT} - \gamma\sqrt{E_B} \right), \quad (14)$$

which gives close agreement to both experimental and simulation results.

To mitigate the increasingly large gate tunneling current through ultra-thin SiO₂, high-permittivity (high- κ) dielectrics have been proposed as replacement. Using (14), Figure 19 illustrates the effectiveness of using various high- κ dielectrics to drastically reduce the gate leakage at a given equivalent oxide thickness (EOT). A physically much thicker gate dielectric layer that results, however, leads to fringe fields in the non-ideal parallel-plate gate-insulator-channel structure, which weakens the gate control over the channel and consequently exacerbates SCEs. It is sometimes interpreted through additional (undesired) increase in the channel potential at the virtual cathode (Figure 20), known as the fringe-induced barrier lowering effect (FIBL). The short-channel V_{TH} model (6) can be readily extended to account for the FIBL effect by adding a barrier-lowering term, $\zeta kT/q$, to the minimum potential,

$$V_m = \Phi_{s,s} + \eta \frac{kT}{q} \frac{\cosh(\theta)}{\cosh(\theta/2)} \ln\left(\frac{Q_m}{n_i t_s}\right) - \left[\frac{\cosh(\theta)}{\cosh(\theta/2)} \eta - 1 \right] \left(\psi_{b,m} + \zeta \frac{kT}{q} \right) \quad (15)$$

Parameter ζ is determined through trend-line analysis matching closely a large set of simulation data (Figure 7, Figure 21) [16],

$$\zeta = 2.39 \frac{t_L}{t_s} \ln \frac{\epsilon_L}{\epsilon_{SiO_2}}, \quad (16)$$

where ϵ_L is the permittivity of gate dielectric. Applying a concerted analysis of FIBL-enhanced SCEs and gate direct tunneling current, candidate high- κ gate dielectrics are assessed on their impact on DG MOSFETs' scaling limits, shown in Figure 22 where symbols correspond to the minimum EOT for each dielectric determined by maximum allowable gate leakage (from Figure 19). High- κ gate dielectrics may extend DG MOSFET scaling beyond that with SiO₂, but the amount of channel length reduction is probably less than 20%.

VII. CONCLUSIONS

Compact, physics-based models of subthreshold swing and threshold voltage are presented for undoped double-gate MOSFETs. Using a unique, scale-length based methodology, threshold voltage variations are analyzed comprehensively and exhaustively. In symmetric DG MOSFETs, L causes 30% to 50% more V_{TH} variation than does t_{Si} for the same process tolerance. Contrarily, t_{Si} causes 35% to 100% more V_{TH} variation than L does in p+/n+ ADG devices. Quantum mechanical effect on threshold voltage has been analytically modeled, which reveals that t_{Si} becomes the largest source of V_{TH} variations at 2nm. A concerted analysis of FIBL-enhanced SCEs and

gate direct tunneling current shows that high-permittivity dielectrics may be helpful to reduce the channel length, but probably by less than 20% compared with SiO₂. Finally, scaling limits projections indicate that individual DG MOSFETs with good turn-off behavior are feasible at 10 nm scale; however, practical exploitation of these devices toward gigascale integrated systems requires significant improvement in process control.

REFERENCES

- [1] Int. Technol. Roadmap for Semiconductors: 2002, Semiconductor Industry Assoc., San Jose, CA, 2002, <http://public.itrs.net/>.
- [2] Q. Chen, B. Agrawal, and J. D. Meindl, "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs," IEEE Trans. Electron Devices, 49, 1086-1090, 2002.
- [3] B. Agrawal, "Comparative scaling opportunities of MOSFET structures for Gigascale Integration (GSI)," Doctoral thesis, Rensselaer Polytechnic Institute, 1994.
- [4] Y. Tosaka, K. Suzuki, and T. Sugii, "Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFETs," IEEE Electron Device Lett., 15, 466-468, 1994.
- [5] Q. Chen, "Scaling limits and opportunities for double-gate MOSFETs," Doctoral thesis, Georgia Institute of Technology, 2003.
- [6] Q. Chen, K. A. Bowman, E. M. Harrell, and J. D. Meindl, "Double jeopardy in the nanoscale court? – Modeling the scaling limits of double-gate MOSFETs with physics-based compact short-channel models of threshold voltage and subthreshold swing," IEEE Circuits and Devices Mag., 19, 28-34, 2003.
- [7] C. T. Lee and K. K. Young, "Submicrometer near-intrinsic thin-film SOI complementary MOSFETs," IEEE Trans. Electron Devices, 36, 2537-2547, 1989.
- [8] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, Y. Animoto, and T. Itoh, "Analytical surface potential expression for thin-film double-gate SOI MOSFETs," Solid-State Electron., 37, 327-332, 1994.
- [9] P. Francis, A. Terao, D. Flandre, and F. Van de Wiele, "Modeling of ultrathin double-gate nMOS/SOI Transistors," IEEE Trans. Electron Devices, 41, 715-720, 1994.
- [10] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," IEEE Trans. Electron Devices, 48, 2861-2869, 2001.
- [11] Q. Chen, E. M. Harrell, and J. D. Meindl, "A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs," IEEE Trans. Electron Devices, 50, 1631-1637, 2003.
- [12] H.-S. Wong, D. J. Frank, and P. M. Solomon, "Device design consideration for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFETs at the 25 nm channel length generation," in IEDM Tech. Dig., 1998, 407-410.
- [13] Q. Chen and J. D. Meindl, "A comparative study of threshold variations in symmetric and asymmetric undoped double-gate MOSFETs," in Proc. IEEE Int. SOI Conf., 2002, 30-31.
- [14] Q. Chen, L. Wang, and J. D. Meindl, "Quantum mechanical effects on double-gate MOSFET scaling," in Proc. IEEE Int. SOI Conf., 2003, 183-184.
- [15] K. A. Bowman, L. Wang, X. Tang, and J. D. Meindl, "A circuit-level perspective of the optimum gate oxide thickness," IEEE Trans. Electron Devices, 48, 1800-1810, 2001.
- [16] Q. Chen, L. Wang, and J. D. Meindl, "Impact of high- κ dielectrics on undoped double-gate MOSFET scaling," in Proc. IEEE Int. SOI Conf., 2002, 115-116.