

Sea of Polymer Pillars Electrical and Optical Chip I/O Interconnections for Gigascale Integration

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Abstract—Optical chip-to-chip communication is a promising technology that can mitigate some of the performance shortcomings of electrical interconnections, especially bandwidth. Moreover, future high-performance chips are projected to drain hundreds of amperes of supply current. To this end, it is important to develop a high-density and high-performance integrated electrical and optical chip I/O interconnection technology. We describe sea of polymer pillars (or polymer pins), which enables the simultaneous batch fabrication of electrical and optical I/O interconnections at the wafer-level. The electrical and optical I/O interconnections are designed to be laterally compliant to minimize the stresses on the die's low- k dielectric as well as to maintain optical alignment between the coefficient of thermal expansion (CTE)-mismatched board and die during thermal cycling. We demonstrate the fabrication and mechanical performance of various size and aspect ratio electrical and optical polymer pillars. We also describe methods of fabricating polymer pillars with nonflat tip surface area for optical interconnection.

Index Terms—Interconnections, optical waveguides, packaging, polymers.

I. INTRODUCTION

IN TRADITIONAL electronic systems, the role of input/output (I/O) interconnections is to provide electrical and mechanical interconnections between the die and the module/board. Due to the performance limitations of electrical interconnects however, not only have optical interconnects replaced electrical interconnects for long distance communication, but optical interconnects are also being developed for chip-to-chip communication [1]–[13]. Microphotonic devices and interconnects can potentially greatly enhance the performance of a microsystem by leveraging high-bandwidth, low-latency, cross-talk-resilient, and low power communication networks [1]–[13]. The projected off-chip communication speed for some chips I/Os is as high as 56.843 GHz at the 18-nm technology node [14]. Moreover, the projected current drain of high performance chips is greater than 300 A [14]. Such high current drain requires the development of high density and high performance electrical I/O interconnections. Today, providing electrical/mechanical I/O interconnections is both difficult and complex [14]. Introducing the new requirement of optical I/O interconnection adds new constraints and introduces

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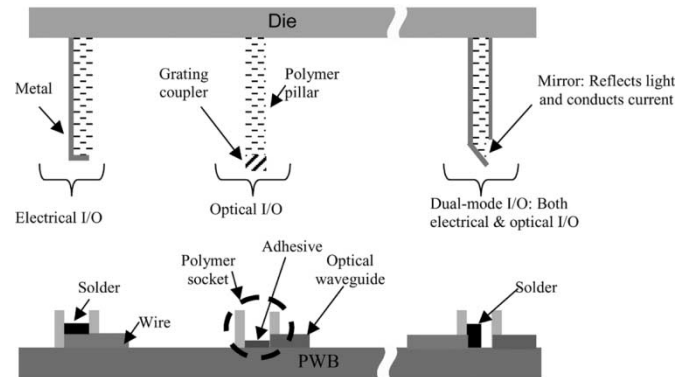


Fig. 1. High-level schematic of a set of polymer pillars that provide electrical, optical, and dual-mode I/O interconnections.

new problems. Some of the key attributes an integrated electrical and optical I/O interconnection technology must possess are the following: a relatively simple and low cost method of fabrication at the wafer level; simple assembly requirements; high performance and high reliability; high tolerance to offsets that may be induced by either coefficient of thermal expansion (CTE) mismatches between the chip and the module/board or misalignment due to assembly; compatibility with wafer-level testing and burn-in; and be implemented using low-temperature materials and processes to ensure process compatibility with structures fabricated by traditional semiconductor front-end and back-end processes. In addition, the use of compliant chip I/O interconnections offers unique solutions to interconnection and packaging of chips with low- k interlayer dielectric [15], [16] without inducing any damage to the on-chip interconnect networks [17].

Sea of polymer pillars (SoPP) is developed to address the need for high density, high performance, mechanically flexible (compliant), and wafer-level integrated electrical and optical I/O interconnections [18]–[21]. SoPP represents the second generation of sea of leads (SoL) chip I/O interconnection technology [17], [22]. The fundamental idea behind SoPP is to fabricate a set of highly mechanically compliant polymer pillars on the die at the wafer level. Depending on what structures are fabricated above them, the polymer pillars can be used to provide electrical, optical, or dual-mode electrical-optical interconnection, as illustrated in Fig. 1. A dual-mode polymer pillar (Fig. 1) is a single I/O interconnection that provides simultaneous electrical and optical interconnections. On the board, polymer sockets are batch fabricated to hold and align the polymer pillars to the board. For clarity, Fig. 2 illustrates a set of polymer pillars, and Fig. 3 illustrates a set of polymer sockets. SoPP, in

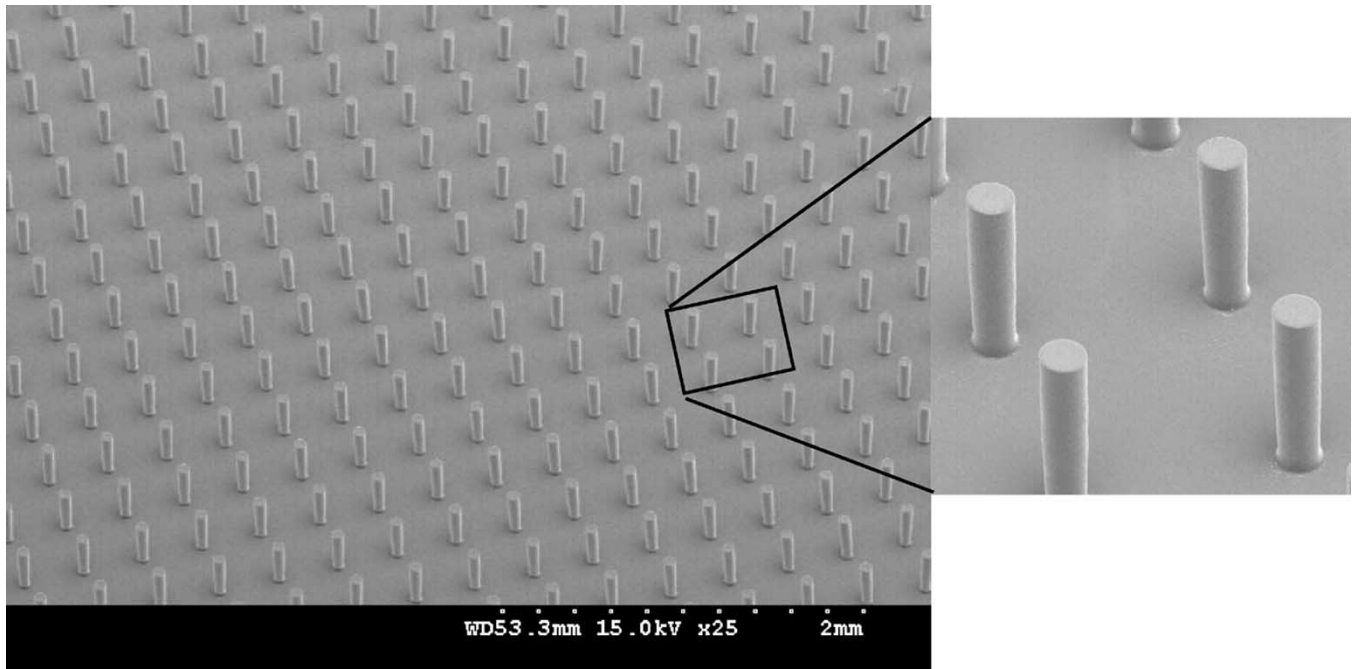


Fig. 2. SEM micrograph of a set of polymer pillars that are $\sim 325 \mu\text{m}$ tall and $60 \mu\text{m}$ in diameter.

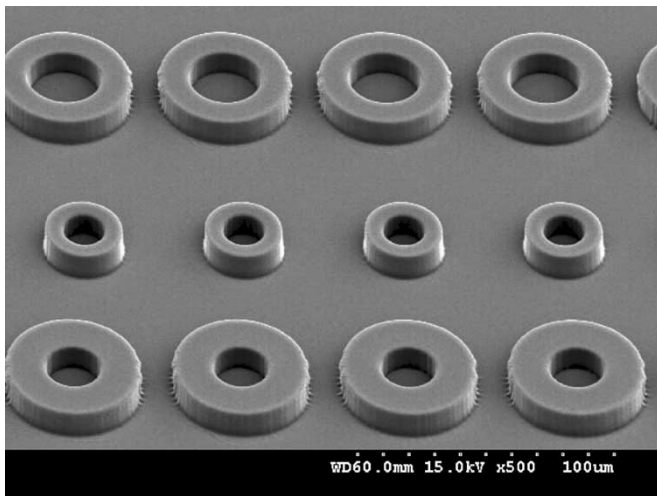


Fig. 3. SEM micrograph of a set of polymer sockets. The sockets are approximately $13 \mu\text{m}$ tall.

essence, extends wafer-level batch fabrication of semiconductor front-end and back-end multilayer interconnect networks to include wafer-level batch fabrication of high-density and compliant electrical and optical chip I/O interconnections, packaging, and testing.

This paper first describes the various electrical, optical, and dual-mode I/O interconnect configurations possible through SoPP in Section II. Section III describes the fabrication process of the polymer pillars (and polymer sockets) and their functionality. The benefits of mechanically compliant electrical and optical I/O interconnections are described in Section IV. The fabrication of polymer pillars with nonflat tip topology for optical interconnection is described in Section V. Finally, Section VI is the conclusion.

II. SOPP I/O INTERCONNECT CONFIGURATIONS

In this section, some of the chip I/O interconnect configurations possible through SoPP are described. While some scanning electron microscope (SEM) micrographs of the fabricated interconnect structures are illustrated for clarity, the fabrication details are not described until Sections IV and V.

A. Optical and Electrical I/O Interconnections

Following the patterning of a metal film on the surface of the polymer pillars, the pillars have been used for electrical interconnection. The sidewall surface area of the polymer pillars may be fully or partially metallized. The electrical and mechanical performance constraints will dictate the type and thickness of the metals that may be deposited on the polymer pillars. The metal films on the polymer pillars should be relatively thin ($0.5\text{--}5 \mu\text{m}$, total). Fig. 4 is an SEM micrograph of an array of polymer pillars with Ti-Au ($300 \text{ \AA}/1 \mu\text{m}$) sidewall metallization. The electrical resistance of the electrical pillars is a function of their aspect ratio and metal coverage. The calculated resistance of one of the pillars shown in Fig. 4 is $13 \text{ m}\Omega$. Since the pillars are compliant, underfill may be precluded during assembly of SoPP chips. The benefits of not requiring underfill include easier chip rework and cheaper and higher assembly throughput. Solder is assumed to be fabricated within the polymer sockets on the board. Fig. 5 is an SEM micrograph of a Si chip with polymer pillars that are Ti-Cu ($300 \text{ \AA}/1.5 \mu\text{m}$) metallized and bonded to a substrate containing a thin film of solder.

The polymer pillars also provide optical I/O interconnection. A polymer pillar is a transverse (perpendicular to the chip) optical waveguide: each polymer pillar acts as the waveguide core with the air surrounding it acting as the waveguide

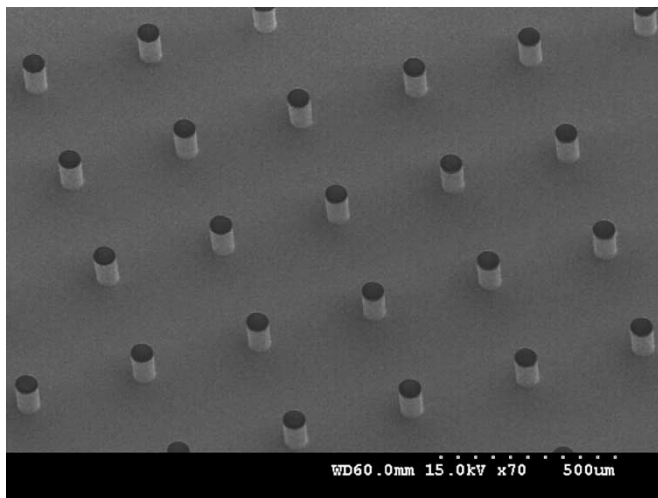


Fig. 4. SEM micrograph of a set of sidewall metallized polymer pillars. The tip surface area of each pillar is not metallized to permit optical transmission. Such pillars were fabricated by depositing a metal film on them followed by the selective etching of the metal from their tips.

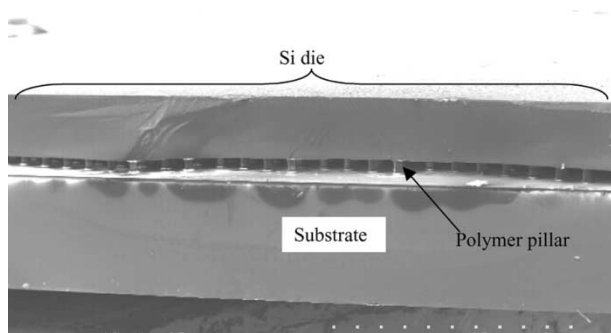


Fig. 5. SEM micrograph of a Si chip with $110\ \mu\text{m}$ tall and $55\ \mu\text{m}$ wide circular polymer pillars bonded to a substrate with a blanket film of Cu and solder (60 Sn/40 Pb). A glass substrate was used for this experiment. Organic, ceramic, and other substrates can also be used.

cladding (index mismatch > 0.5). In order to demonstrate the optical quality of the polymer pillar waveguides, optical transmission measurements were performed [21]. It has been shown that the polymer pillars act as precision waveguides thus verifying the cross-sectional uniformity, smoothness of surfaces, endface flatness, and optical quality of the material [21]. Unlike electrical interconnections, optical interconnections do not easily tolerate right-angle bends and thus, optical devices that mitigate right-angle bends (mirrors or grating couplers) are needed at those interfaces. This is true for both within-plane and out-of-plane right-angle bends. In this research, surface-normal right-angle bends are investigated. Right-angle bends in optical interconnections can be implemented with the use of mirrors and grating couplers. Pillars have been fabricated on mirrors [20] and they may also be fabricated directly on chip-level photodetectors and optical sources. The fabrication and testing of optical polymer pillars on Si MSM photodetectors has been demonstrated [29].

Fig. 6 is a schematic illustrating the ability to fabricate mirrors and volume/surface relief grating couplers at either the tips of the polymer pillars or within the planar polymer waveguides on the board. The latter has been demonstrated in the literature

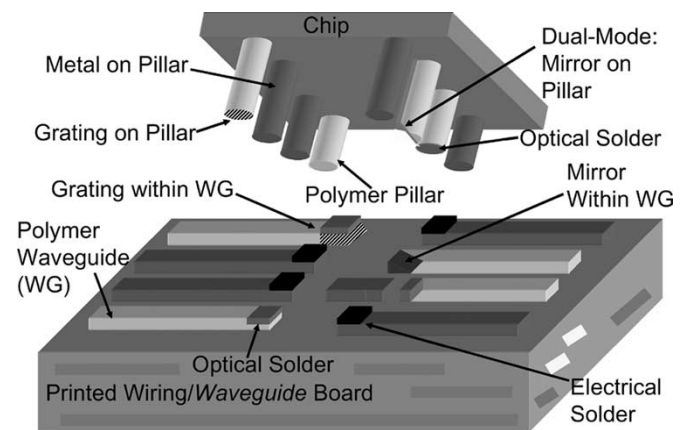


Fig. 6. Possible methods of attaining electrical, optical, and dual-mode I/O interconnections through SoPP. Grating couplers and mirrors may be fabricated either on the tips of the polymer pillars or within the optical waveguides on the printed wiring/waveguide board to implement surface-normal optical coupling. Polymer sockets on the board may be used to hold and align the pillars to the board.

[3]. The primary advantage of fabricating grating couplers directly on the tips of the polymer pillars is that nanolithography is readily available at the wafer level due to the lithography requirements of semiconductor front-end and back-end devices. Thus, the fabrication of nanoresolution optical devices directly on the polymer pillars potentially offers significant cost advantages over the fabrication of such devices on the board-level planar waveguides.

B. Dual-Function I/O Interconnections

Thus far, the discussion has been limited to using each polymer pillar for a single interconnect function—either electrical or optical. However, it is possible to use a single polymer pillar for multiple functions. A dual-mode polymer pillar is a single I/O interconnection device that provides simultaneous electrical and optical interconnections (Fig. 1). The pillars shown in Fig. 4 are dual-mode polymer pillars. In addition, polymer pillars with an optically designed nonflat tip-topology can be used to implement optical coupling between the planar waveguide and the polymer pillar. An example of such a structure, which was not optimized for maximum coupling between a planar waveguide and a polymer pillar, is shown in Fig. 7. The SEM micrograph shows a polymer pillar with a partially slanted tip that can be used as a mirror. Pillar diameter and mirror tip coverage have to be fabricated to maximize coupling between the polymer pillar and the planar waveguide and to minimize back reflections. When the sidewall metallization of the electrical polymer pillars is extended to such polymer pillars, each polymer pillar provides simultaneous electrical and optical interconnections: the mirror reflects an optical signal from the board-level planar waveguide into the polymer pillar while the sidewall metallization provides simultaneous electrical interconnection. This dual-mode electrical and optical polymer pillar, or heterogeneous I/O interconnect, allows for intimate process integration between the electrical and optical I/O interconnections. Nanoresolution surface relief diffractive grating couplers may be fabricated instead. Thus, a dual-mode polymer pillar is an I/O interconnection device that

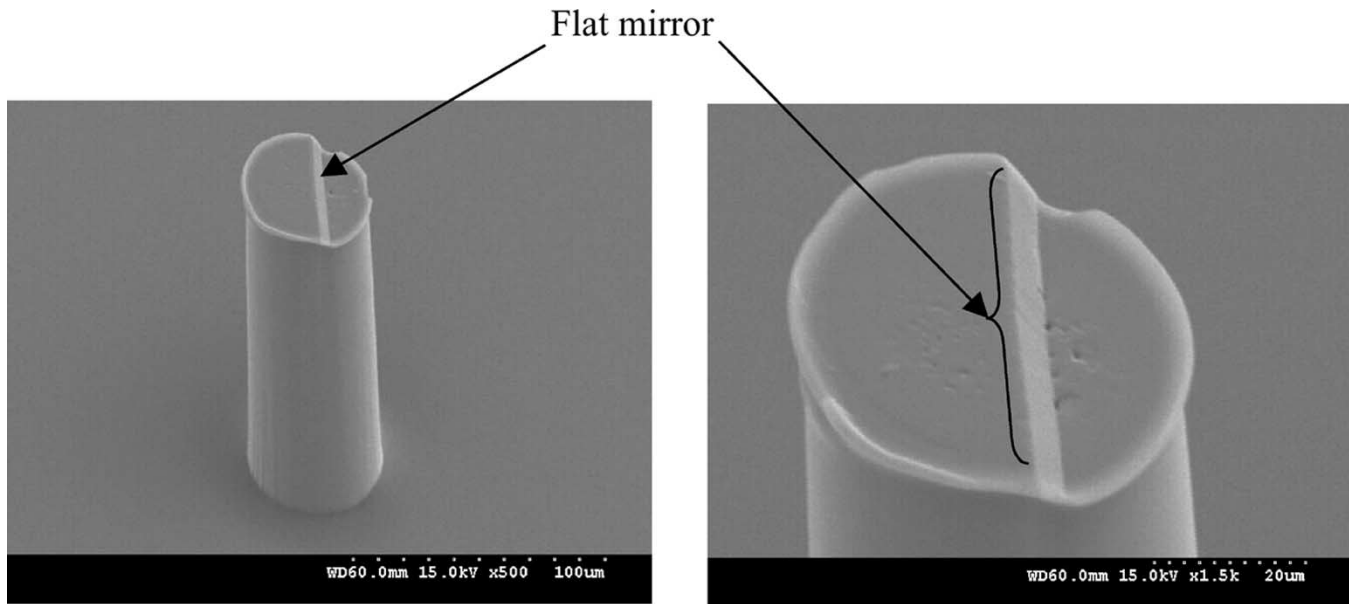


Fig. 7. SEM micrograph of $\sim 110 \mu\text{m}$ tall and $55 \mu\text{m}$ wide polymer pillar with a $6 \mu\text{m}$ tall flat mirror on its tip.

provides two orthogonal interconnect functions. The thickness of the metallic film has to be selected such that it yields low parasitic electrical interconnections without disturbing the high compliance of the intrinsic polymer pillars. Moreover, the metal has to be selected such that it provides high optical reflectivity at the wavelength of interest.

III. BENEFITS OF MECHANICALLY COMPLIANT INTEGRATED ELECTRICAL AND OPTICAL I/Os

The polymer pillars have been experimentally shown to be laterally compliant using a Hysitron TriboIndenter. A Si substrate containing the polymer pillars was mounted sideways in the nanoindenter. The pillars were indented at approximately their tips. The measured compliance of an approximately $55 \mu\text{m}$ diameter and $110 \mu\text{m}$ tall circular pillars was shown to be greater than $2 \mu\text{m}/\text{mN}$ at $5 \mu\text{m}$ displacement (Fig. 8). The compliance of an approximately $60 \mu\text{m}$ diameter and $295 \mu\text{m}$ tall circular pillar was greater than $20 \mu\text{m}/\text{mN}$. All tested polymer pillars returned to their original position following the measurements. The tested pillars were cured for 2 h in a 200°C nitrogen-purged furnace.

Since the optical polymer pillars are fabricated using the same low-modulus ($\sim 0.5 \text{ GPa}$) polymer used for the electrical I/O interconnections, the optical I/O interconnections are also mechanically compliant. This concept is schematically illustrated in Fig. 9. The optical polymer pillars can undergo strain, as needed, by bending and stretching, to compensate for the chip's and board's different thermo-mechanical expansion behaviors. This is significant because the polymer pillars reduce the optical losses due to offset between the chip and the board, which is induced during thermal cycling. Without a compliant optical I/O interconnection, offsets in alignment between the chip and the board can cause high optical losses. Thus, the polymer pillar waveguides help to maintain optical alignment during field service of the assembled system. This is a very

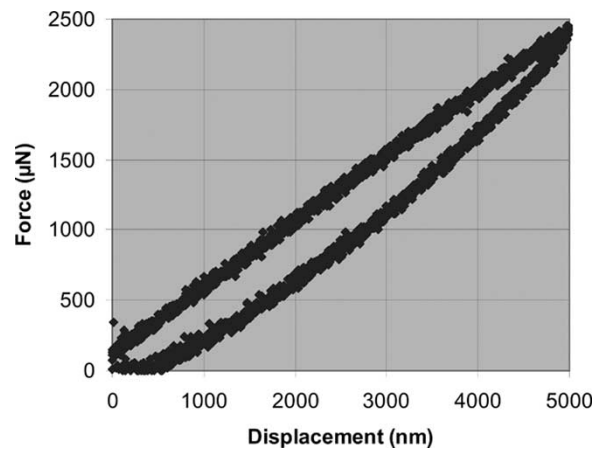


Fig. 8. Force-displacement characteristic curve of a sideways mounted polymer pillar that is $\sim 110 \mu\text{m}$ tall and $55 \mu\text{m}$ wide. Thus, the above plot describes the lateral compliance of the polymer pillar.

significant result. The International Technology Roadmap for Semiconductors (ITRS) states that “The key mechanical issues with optoelectronic packaging is aligning the optical path and maintaining this alignment under all service conditions ... [while] the main issue in assembly is how to automate the alignment process ... to reduce costs” [24]. The mechanically flexible polymer pillar waveguides help to maintain optical alignment. One of the key benefits of the sockets on the board is to enable chip-to-board self-alignment during assembly, as well be described in Section IV.

If the polymer pillars are too compliant, they can present many challenges. For example, wafer dicing and die bonding can clearly be very difficult to accomplish if the pillars are too mechanically compliant. Thus, the aspect ratio and height of the pillars has to within a certain range. A substrate with an array of $110 \mu\text{m}$ tall and $55 \mu\text{m}$ diameter circular polymer pillars was successfully diced using a diamond saw with high pressure deionized (DI) water. No visible damage was seen on the pillars.

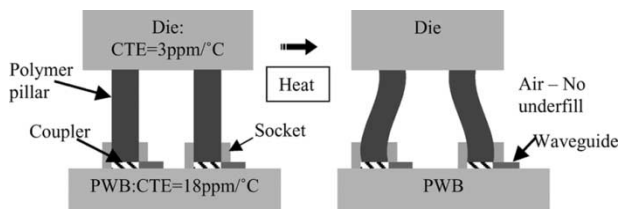


Fig. 9. Schematic illustrating how the polymer pillars compensate for the CTE mismatch between the board and the die to minimize optical losses due to offset. Thus, the polymer pillars can maintain a high degree of optical alignment during thermal cycling.

However, different aspect ratio pillars might require the pillars to be coated with a sacrificial material to prevent damage as a result of high pressure DI water used during dicing.

It should be pointed out that some of the material requirements for conventional optical interconnects do not necessarily apply for SoPP. For example, SoPP is not restricted to using ultralow absorption optical materials due to the short height ($<300 \mu\text{m}$) of the polymer pillars. In addition, it is known that when metal surrounds an optical waveguide, the optical losses in the waveguide may increase. In dual-mode SoPP, however, the short pillar heights are expected to mitigate such losses. The metal layer, however, should be highly reflective at the optical wavelength of interest to minimize such losses.

IV. POLYMER PILLAR AND POLYMER SOCKET FABRICATION

To date, the polymer pillars and polymer sockets have been fabricated using the photodefinable and negative tone polymer Avatrel 2000P (Promerus, LLC). The sockets could ultimately be fabricated using a material that has a lower index of refraction than the pillars. A schematic of the fabrication process is illustrated in Fig. 10. The fabrication process of the polymer pillars and the polymer sockets is similar. The general fabrication sequence is as follows: the first process step is to spin coat the polymer film (Avatrel 2000P) onto the substrate. The height of the polymer film will ultimately be the height of the polymer pillars (or sockets). If tall polymer pillars are desired, it may be necessary to spin coat multiple layers of the polymer film. The wafer is next placed on a hotplate (100°C) for a soft bake. Next, the polymer film is irradiated with a 365-nm ultraviolet (UV) light through a dark-field mask containing the cross-sectional geometry of the pillars (or sockets). Once exposed, the wafer is placed in a nitrogen-purged oven (100°C) for a hard bake for 20 min. Next, the polymer is spray-developed to yield the polymer pillars (or sockets). Finally, the substrate is placed in a nitrogen-purged furnace for a cure. The cure peak temperature is $160\text{--}200^\circ\text{C}$, and the time duration can be as short as 1 h. Thus, the fabrication of the polymer pillars is a low temperature process and allows for the integration with CMOS devices and low- κ /multilayer interconnect networks at the wafer level.

High magnification SEM micrographs of a $100 \mu\text{m}$ tall and $55 \mu\text{m}$ wide and a $180 \mu\text{m}$ tall and $55 \mu\text{m}$ wide polymer pillar fabricated on a Si wafer with a silicon nitride ($0.2 \mu\text{m}$) passivation are shown in Fig. 11. Very high aspect ratio (5) and tall ($325 \mu\text{m}$) pillar pillars were also fabricated, as shown in Fig. 2. The polymer Avatrel 2000P adheres well to either silicon nitride or silicon dioxide. When the pillars are fabricated directly on Si,

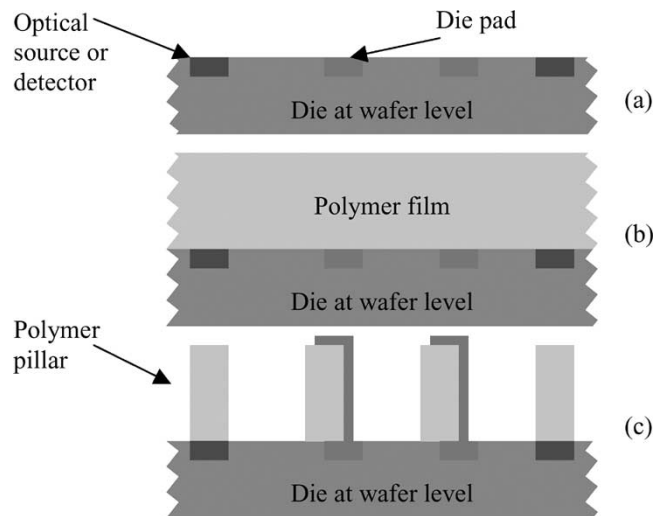


Fig. 10. Fabrication sequence of the polymer pillars: (a) Wafer, (b) Avatrel 2000P is spin coated to the desired thickness and placed on a hotplate (100°C) for a soft bake. The polymer film is next UV irradiated through a mask. The wafer is next placed in an oven (100°C) for a hard bake. Finally, (c) the polymer film is spray-developed to yield the final polymer pillars, and the wafer is placed in a furnace for a cure ($160\text{--}200^\circ\text{C}$). Metal is next deposited on the pillars serving electrical interconnection. Optical devices, such as surface relief gratings couplers and mirrors are fabricated, when needed, on the tips of the polymer pillars providing optical interconnection (Fig. 16).

the yield is typically low due to poor adhesion. Pillars with various aspect ratios and cross-sectional geometries have also been successfully fabricated, as shown in Fig. 12. This is important because the polymer pillar's geometry and aspect ratio dictate its mechanical compliance and optical transmission properties. The processes outlined in Section III have been used to fabricate polymer pillars at pitches almost equal to those of the top-most chip wiring level. For example, Fig. 12 illustrates a set of polymer pillars fabricated on a $12 \mu\text{m}$ pitch, thereby creating an area-array I/O density of $\sim 7 \times 10^5/\text{cm}^2$. The highest aspect ratio and smallest diameter polymer pillar successfully fabricated to date is a $20 \mu\text{m}$ tall and $4 \mu\text{m}$ wide polymer pillar with a circular cross section. The polymer material can resolve features with much higher aspect ratios. For example, Fig. 13 is an optical micrograph of a set of $100 \mu\text{m}$ tall and $10 \mu\text{m}$ wide polymer pillars that have collapsed onto the surface of the wafer following spray developing. This demonstrates that the polymer material exhibits the ability to photoimage structures with an aspect ratio of 10. However, the high aspect ratio polymer pillars do not have the mechanical stability to remain standing. This imposes one of the limitations on the fabrication of high aspect ratio polymer pillars. Another important parameter that imposes a limitation on the fabrication of high aspect ratio polymer pillars is the pitch. The closer the polymer pillars are to each other, the more difficult it is to fabricate perfectly standing polymer pillars.

Polymer sockets have been fabricated using the same polymer and process described above. Fig. 3 is an SEM micrograph of various aspect ratio polymer sockets. Ultimately, polymer sockets with positively slanted inner sidewalls should be fabricated to provide chip-to-board self alignment during assembly: if the pillars are misaligned with respect to their intended position on the board during assembly, the positive

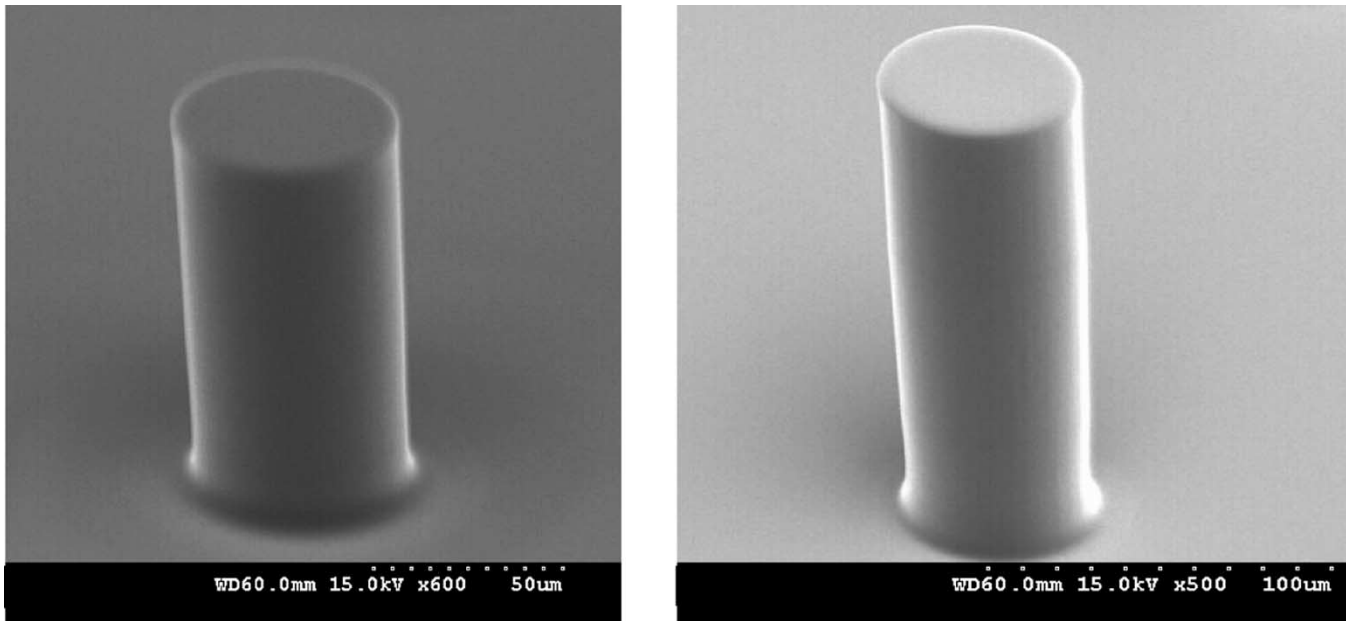


Fig. 11. SEM micrographs of a polymer pillar that is $\sim 100 \mu\text{m}$ tall and $55 \mu\text{m}$ wide (left), and a polymer pillar that is $\sim 180 \mu\text{m}$ tall and $55 \mu\text{m}$ wide (right).

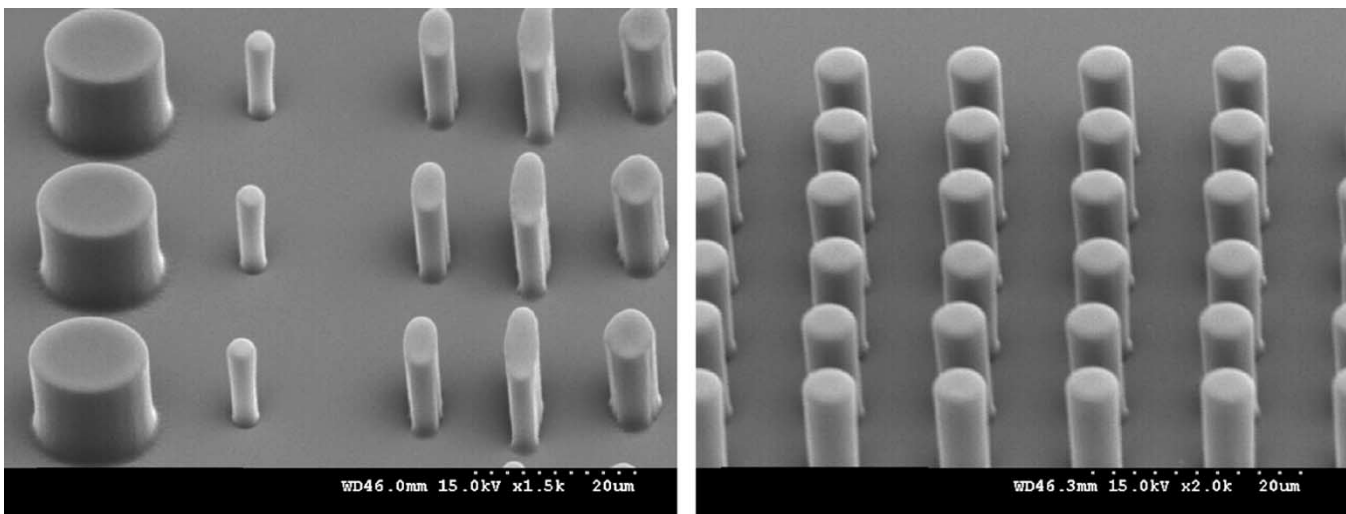


Fig. 12. SEM micrographs illustrating various shape and aspect ratio polymer pillars (left), and $13 \mu\text{m}$ tall and $5 \mu\text{m}$ wide circular polymer pillars distributed on a $12 \mu\text{m}$ pitch.



Fig. 13. Micrograph of a set of $100\text{-}\mu\text{m}$ tall and $10\text{-}\mu\text{m}$ wide circular polymer pillars after spray developing. Clearly, while the pillars were resolved, the very high aspect ratio polymer pillars were mechanically unstable and thus, collapsed.

slants on the sockets' sidewalls will cause the pillars to slide down to their intended position. Thus, the sockets help to improve the alignment tolerances of flip-chip bonders and enables passive high precision alignment between three-dimensional optical waveguides and devices. The height of the polymer sockets depends on the height of the polymer pillars. Ideally, only a small percentage of the pillar's height should be inserted into the socket.

V. FABRICATION OF POLYMER PILLARS WITH NONFLAT TIP TOPOLOGY FOR OPTICAL INTERCONNECTIONS

The tips of the polymer pillars can be patterned into any surface topology. In this section, two methods of fabricating polymer pillars with sloped tips are described. The fabrication

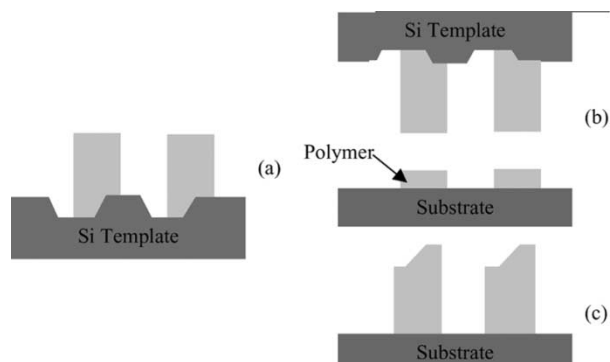


Fig. 14. Flip-pillar bonding: reverse molding process. (a) Polymer pillars are fabricated on template, (b) a substrate is coated with a thin layer of a polymer (without a soft bake). The template is flipped, and the polymer pillars are pressed on the polymer, which is in liquid form. The aggregate structure is next placed on a hotplate for a soft bake, (c) following soft bake, the template is mechanically removed leaving behind the tip-patterned polymer pillars.

processes described, however, appear to be applicable to fabricate polymer pillars with any other tip surface topology (surface relief gratings, diffractive lenses, concave and convex lenses and mirrors, etc.).

The first fabrication method is illustrated in Fig. 14. The polymer pillars are fabricated on a template and then flipped onto another substrate such that the template pattern at the base of the pillars becomes the tip of the final reversed polymer pillars. The process begins by fabricating polymer pillars on the slanted surface on a template, as shown in Fig. 14(a). For simplicity, the template used was Si. Next, the template is flipped and pressed against the substrate with the thin layer of Avatrel 2000P, as shown in Fig. 14(b). The aggregate structure is next placed on a hotplate for a soft bake. Following a soft bake, the aggregate sample is removed and allowed to cool down. Finally, the template is removed from the substrate to leave behind polymer pillars with slanted tips on the substrate, as shown in Fig. 14(c).

An alternative process used to fabricate polymer pillars with surface relief features on their tips is based on polymer imprinted. Specifically, the polymer film is imprinted prior (or after) photoimaging. More importantly, the polymer is imprinted while it undergoes plastic deformation. The polymer Avatrel 2000P plastically deforms prior to curing while it elastically deforms after curing. This was experimentally confirmed using a Hysitron TriboIndenter by compressing the polymer pillars. Fig. 15 illustrates the force-displacement characteristic curves of a cured and an uncured polymer pillar ($\sim 110 \mu\text{m}$ tall and $55 \mu\text{m}$ wide). Fig. 16 illustrates the fabrication process implemented to fabricate flat mirrors on a polymer film prior to photoimaging. Following polymer soft bake [Fig. 16(a)], the polymer film is imprinted with a template [Fig. 16(b)] at a temperature lower than the soft bake temperature. Following this process step, the process described in Fig. 10 follows beginning with UV irradiation. This process has been successfully used to fabricate polymer pillars similar to those shown in Fig. 7. Once again, for simplicity, the template used was Si. Such a process is potentially easier to implement at the wafer-level than the process described previously. While the molding process has been demonstrated previously for planar optical

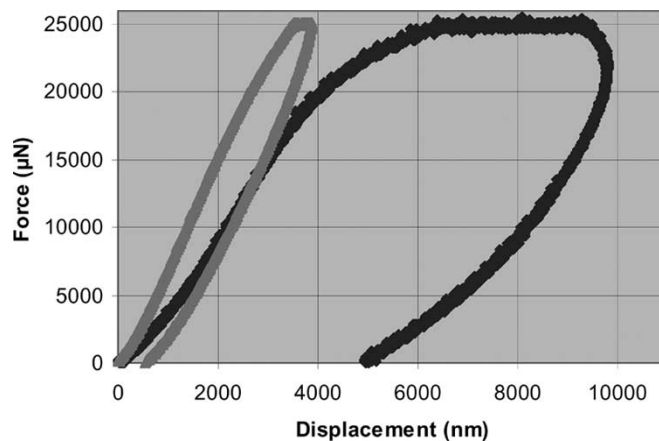


Fig. 15. Measured (compression) force-displacement characteristic curves of a cured and an uncured polymer pillar. It is clear that the uncured polymer pillar (right curve) undergoes plastic deformation while the cured polymer pillar (left curve) undergoes mainly elastic deformation. The plastic deformation prior to curing enables the fabrication of pillars with optical features on their tips at the wafer level such as those shown in Fig. 7.

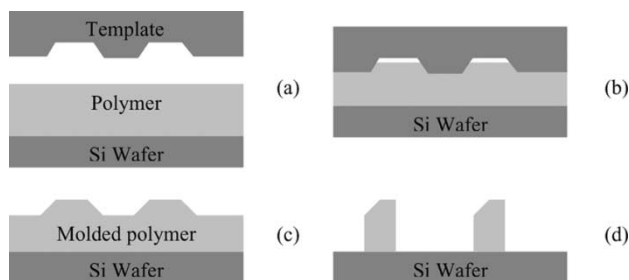


Fig. 16. Schematic of the fabrication process used to mold the top portion of the polymer film to ultimately yield polymer pillars with fine optical features on their tips (slanted tips is shown above). The key is to imprint the photosensitive polymer film while it is in the plastic (uncured) deforming state. (a) Template is prepared. A polymer film is spin coated and soft baked. (b) The template is pressed on the polymer film. (c) The template is removed to leave behind the molded polymer film. (d) The polymer film is UV irradiated through a mask containing the cross-sectional geometry of the polymer pillars followed by a hard bake and spray developing. The final structures are polymer pillars with nonflat tip topology. The wafer is finally placed in a furnace for a cure.

waveguides[25]–[27], the process just described permits one to perform the compression molding of the fine optical features at a temperature below the glass transition temperature (T_g) of the polymer ($T_g > 250 \text{ }^\circ\text{C}$) in order to preserve the polymer's photosensitivity, which is needed to yield the polymer pillar structure. Other methods of fabricating slanted surfaces may be integrated with the polymer pillars including directional RIE at oblique angles [28].

VI. CONCLUSION

This paper described the I/O interconnect configurations and fabrication details of the second generation of Sea of Leads (SoL) chip I/O interconnections, or Sea of Polymer Pillars (SoPP). The fundamental idea behind SoPP is to fabricate highly compliant, or mechanically flexible, polymer pillar waveguides at the wafer level and to fabricate polymer sockets on the board to hold and align the polymer pillars to the board. Depending on what structures are fabricated above the polymer

pillars and within their respective polymer sockets, the polymer pillars are used for electrical and optical I/O interconnections. One of the most significant attributes of SoPP is that all I/O interconnections (electrical and optical) are mechanically flexible. The compliant optical I/O interconnections maintain optical alignment between the chip and the board during thermal cycling to minimize optical losses due to offset as well as undergo strain to minimize the stresses generated at the die pads during thermal cycling. This is essential for chips with low- κ interlayer dielectric. The use of a single polymer pillar for simultaneous electrical and optical interconnections is also described. Such a structure, or a dual-mode polymer pillar, provides a very high level of electrical and optical I/O interconnect process integration.

Various fabrication processes have been developed to fabricate the interconnect structures described above. At the heart of all processes, however, is photoimaging of the low modulus and high quality optical polymer Avatrel 2000P. This polymer was used to fabricate all polymer interconnect structures. Polymer pillars as tall as 325 μm have been fabricated. Moreover, polymer pillars on a 12 μm area-array pitch have also been fabricated. Imprinted of the polymer film at the wafer level while preserving its photosensitivity (i.e., low temperature) is demonstrated to fabricate pillars with slanted tips. The low temperature processes ($<200\text{ }^\circ\text{C}$) required for the fabrication of the optical and electrical polymer pillar I/O interconnections are compatible with the temperature constraints imposed by CMOS devices and low- κ interlayer dielectrics in high performance chips.

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