Wafer-Level Packaging of Optoelectronic Chips using Sea of Leads Electrical and Optical I/O Interconnections

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As the complexity and hyper-integration of various devices increase on chips, the complexity and constraints imposed on packaging, assembly, and testing increase as well. As the feature sizes of Si transistors shrink, on-chip electrical interconnects begin to dominate the overall performance characteristics of a gigascale chip. The use of Cu interconnects and low-k dielectric was introduced to leverage the growing performance mismatch between transistors and interconnects. Similarly, electrical interconnects are foreseen to impose bandwidth limitation on chip-to-chip communication. At this interconnection level, mircophotonics technology will potentially be a key enabling technology for high bandwidth chip-to-chip communication. Not only is the design and manufacturing of novel optoelectronic devices compatible with Si-based technology necessary to leverage chip-to-chip high bandwidth communication, but advances in optical interconnection and packaging are also essential.

The packaging, alignment, and assembly of optoelectronic chips are complex and costly. Wafer-level packaging and testing of optoelectronic chips offer significant cost benefits. Our approach utilizes a 'Sea' of electrical and optical chip I/O interconnections. Sea of Leads (SoL) [1-3] provides wafer-level packaging and batch fabrication of mechanically compliant (flexible) and highly process integrated electrical (dc and high frequency signals) and optical (high bandwidth) chip I/O interconnections (Figs. 1-2). The optical I/O interconnections are polymer pillars with a mirror or a diffractive grating coupler fabricated on their respective tips. Specially tailored sockets on the board are fabricated to enable *self-alignment* onto the board, where waveguides are routed, to simplify flip-chip optical alignment and assembly. The electrical interconnects are fabricated by partially metallizing the polymer pillars. In another SoL configuration, the electrical interconnections are s-shaped Cu leads fabricated on a polymer film with embedded air gaps. The polymer pillars are designed to be compliant such that optical alignment between the chip and the board, which often have a different coefficient of thermal expansion (CTE), is maintained during thermal cycling. The latter has been identified by the International Technology Roadmap for Semiconductors as one of the key challenges facing optoelectronics [4]. The compliant electrical and optical I/O interconnections also reduce the stress on the chip's low-k dielectric, which is fragile, during thermal cycling between the CTE mismatched chip and board. Because of the compliant leads, underfill is not needed during assembly. The use of waveguide air cladding simultaneously enhances the optical (wave confinement) and mechanical (compliance) characteristics of the polymer pillars. The density of the electrical and optical interconnections can be as high as $10^6/cm^2$. All polymer materials used for SoL wafer-level packages and I/O interconnections exhibit low temperature processing and high glass transition temperature (T_g) to ensure process and assembly compatibility. The polymer pillars are batch fabricated using the low modulus (0.5 GPa), high T_g (greater than 250˚C), photodefinable, and low loss optical polymer Avatrel 2000P (supplied by Promerus LLC.).

This presentation will describe SoL, its processing, its process integration with optoelectronic devices, and its optical, electrical, and mechanical characteristics.

References:

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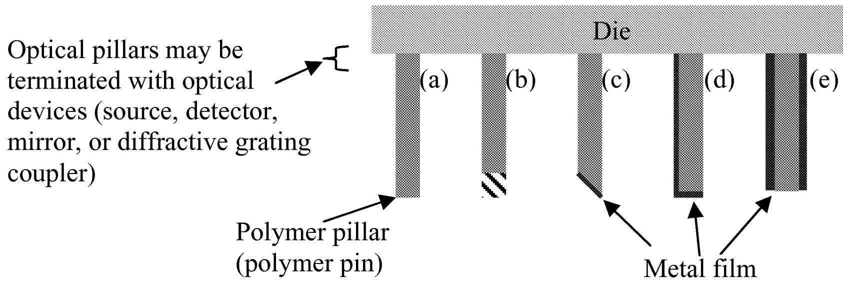

Fig. 1: Schematic illustrating five basic I/O interconnection configurations possible using polymer pillars: (a) polymer pillar: surface normal waveguide with air cladding, (b) polymer pillar terminated with a diffractive grating coupler, (c) polymer pillar terminated with a mirror, (d) partially metallized polymer pillar for electrical interconnection, (e) sidewall metallized pillar for simultaneous electrical and optical interconnection (may be terminated with mirror or diffractive grating coupler).

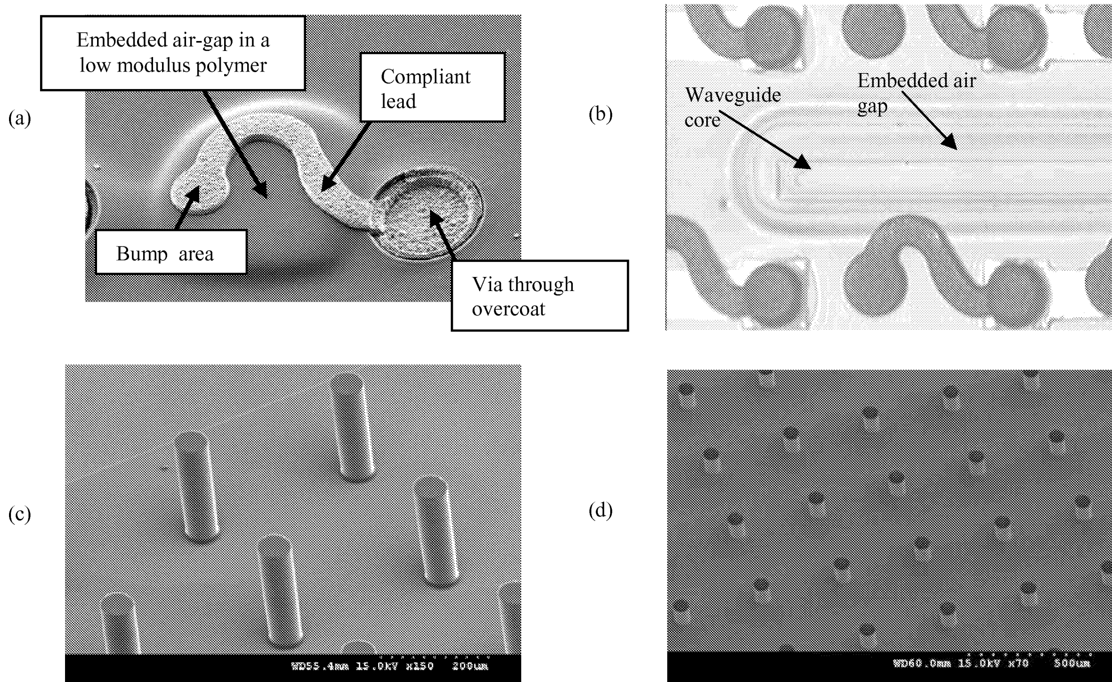

Fig. 2: SEM images of various wafer-level packages that offer mechanically compliant and highly process integrated electrical and optical Sea of Leads (SoL) chip I/O interconnections. (a) S-shape Cu lead above a polymer film with an embedded air gap for high lateral and transverse compliance. (b) Channel waveguides with air cladding embedded within SoL interconnections. (c) Sea of polymer pillars (waveguides) that provide surface normal optical interconnection and maintain optical alignment during thermal cycling (pillars shown are ~300 μm tall and ~60 μm in diameter). Polymer pillars with a mirror on their respective tips have also been demonstrated through a polymer imprinting process [1]. (d) Sidewall metallized polymer pillars that provide simultaneous electrical and optical interconnections. Polymer pillars on an array pitch of 12 μm have also been successfully fabricated.