

21.3 Sea of Dual Mode Polymer Pillar I/O Interconnections for Gigascale Integration

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Sea of Leads (SoL) input/output (I/O) interconnection technology provides the capability to batch fabricate an area array of ultra-high density ($>10^9/\text{cm}^2$) high performance three-dimensional compliant I/O interconnects immediately following back-end-of-the-line (BEOL) wafer processing to enhance performance of gigascale integration (GSI) [1]. Fabrication of highly compliant in-plane 'slippery' leads and embedded air-gaps under the leads for high transverse compliance have been demonstrated and mechanically/electrically characterized [2]. The next generation of SoL I/O interconnection technology is introduced. On the chip side, highly compliant electrical, optical, RF, and dual-mode polymer pillar I/O interconnects are batch fabricated to offer a substantially higher I/O density ($>10^9/\text{cm}^2$) as schematically illustrated in Figs. 21.3.1 and 21.3.2. To facilitate the interconnection of the Sea of Polymer Pillars (SoPP), complementary polymer cups (or sockets) are fabricated on the substrate to align and hold the pillars.

With only three masking steps following BEOL, high-density integrated electrical, optical, and RF polymer pillar I/O interconnects are batch fabricated. The thickness of the metal deposited on the sidewalls of the pillars serving as electrical interconnects (Fig. 21.3.3) is selected to provide low electrical parasitics and to preserve the highly compliant nature of the polymer pillars. Solder may be fabricated either on the tips of the pillars or in the polymer cups (Fig. 21.3.4). The polymer cups help to contain the solder during assembly of ultra-fine SoPP I/O interconnects.

It is possible to create a transverse optical I/O interconnection between the chip and the substrate using SoPP. Instead of metalizing a pillar, either a surface relief or a volume grating coupler is fabricated at the tip of the pillars facilitating light coupling into the pillar. Thus, the pillar acts as a physical transverse optical I/O waveguide. The pillars are fabricated directly above photodetectors/VCSELs or on an optical element such as a mirror or a grating (Fig. 21.3.5). When the pillars are inserted into their respective substrate polymer cups, where substrate-level optical waveguides terminate, the grating coupler at the tip of the pillar couples light from the substrate-level waveguide into the pillar and the light is routed vertically to the chip. Since the optical I/O pillars are fabricated using the same low-modulus polymer used for the electrical I/Os, the optical I/Os are also mechanically compliant. Therefore, optical misalignment due to different thermo-mechanical behavior between the chip and the substrate is minimized because the compliant polymer pillar optical waveguides bend to compensate for offset. Since no underfill is required for SoPP chips, the pillars are surrounded by air. This allows the pillar waveguide to have a high index of refraction difference (>0.5) between the core (polymer pillar) and the cladding (air) thereby providing a high degree of confinement of the optical signal. Another method of routing the optical signal from a substrate waveguide into a polymer pillar is through the use of a micromirror at the tip of the pillar (Fig. 21.3.2). If the sidewall metalization of the electrical I/O pillars is extended to the slanted region at the tip of the pillar, then each polymer pillar is both a potential electrical and optical interconnection since the mirror can reflect the optical signal from the slab waveguide into the pillar waveguide and the sidewall metallization is used for elec-

trical interconnection. This dual function pillar, or heterogeneous I/O interconnect, allows for an intimate integration of electrical and optical I/O interconnects. Mirrors may also be fabricated on the substrate and mated with the pillars.

SoPP also facilitates RF I/Os interconnects based on near-field capacitive coupling similar to those proposed in [3]. A pillar with one of the two parallel plates forming the capacitor is brought into very close proximity to the complementary metal plate at the substrate to form a near-field capacitor (Fig. 21.3.1).

SoPP is fabricated at pitches close to those of the top-most chip wiring level. For example, Fig. 21.3.6 illustrates polymer pillars fabricated on a $12\mu\text{m}$ pitch thereby creating an area array I/O density of $\sim 7 \times 10^9/\text{cm}^2$. If dual-mode electrical-optical polymer pillars are used, then it is possible to attain $7 \times 10^9/\text{cm}^2$ electrical I/Os and $7 \times 10^9/\text{cm}^2$ optical I/Os from $7 \times 10^9/\text{cm}^2$ polymer pillars. These I/O numbers exceed those projected by the ITRS by more than three orders of magnitude [4]. SoPP I/O interconnects offer circuit and system designers essentially unlimited I/O bandwidth at potentially the lowest cost. Moreover, since the polymer pillars are short in height ($<200\mu\text{m}$), and thus in interconnection length, the pillars will exhibit high electrical and optical performance. As a result, SoPP I/O interconnects offer the most intimate electrical, optical, and RF I/O wafer-level process integration at the lowest cost and highest performance. Preliminary testing and measurements have shown that light can be reflected off the mirrors fabricated beneath the pillars and light in-coupling through a $200\mu\text{m}$ layer of polymer by a volume grating coupler. The polymer material used to make the pillars is shown to have minimal optical losses.

Benefits of SoPP I/O interconnects for a microsystem are numerous. High-density electrical I/Os are essential for reducing simultaneous switching noise, power losses, and total wiring area for global on-chip power distribution networks [5]. Improved isolation and reduced interference in mixed-signal systems resulting from the use of separate power/ground I/O leads for analog and digital signals are possible. The integration of optical and electrical I/Os is essential because microphotonic interconnects have the long-term potential to reduce latency, power dissipation, and crosstalk while increasing bandwidth enormously [6]. Polyolithic [6] and hybrid integration of heterogeneous chips are both enabled through SoPP. As a result, SoPP offers long term I/O interconnection solutions for GSI.

Acknowledgements

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References

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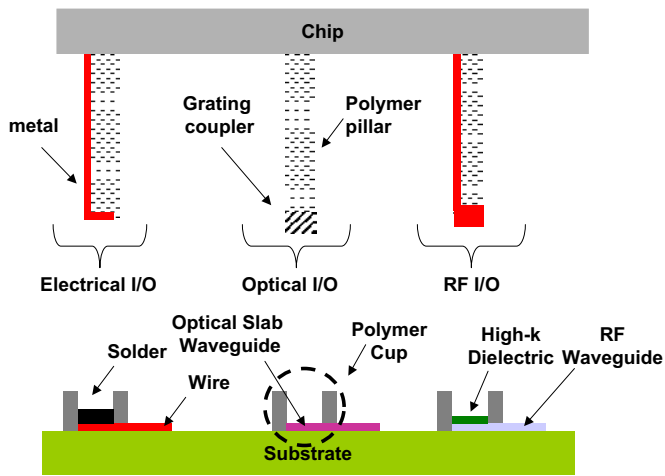


Figure 21.3.1: Possible interconnection technologies feasible through wafer-level Sea of Polymer Pillars I/O interconnects.

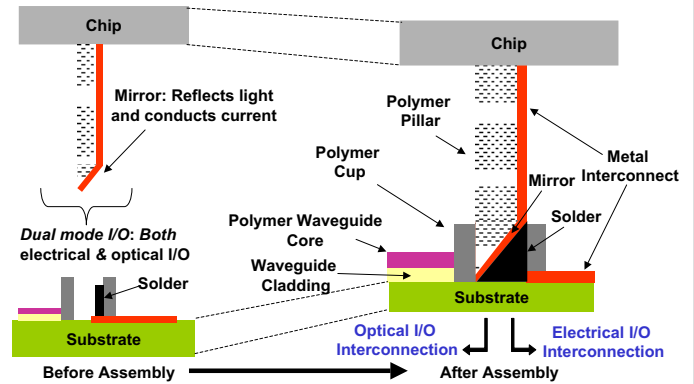


Figure 21.3.2: Illustration of dual-mode (heterogeneous) electrical-optical I/O interconnect. The left side of the pillar allows for optical interconnection while the right side allows for electrical interconnection.

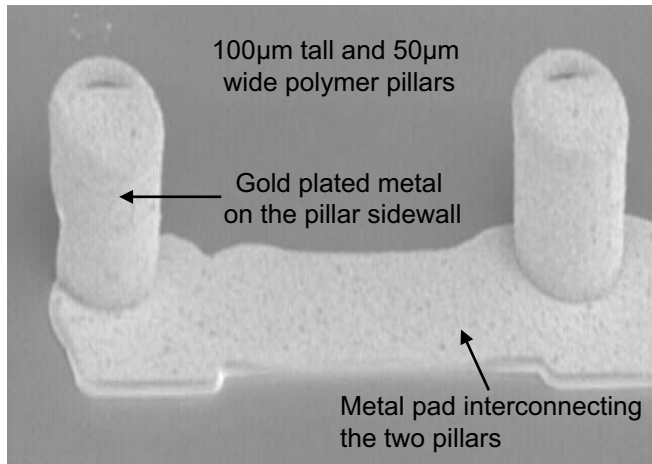


Fig. 21.3.3: SEM micrograph of a pair of interconnected polymer pillars metallized with gold plating.

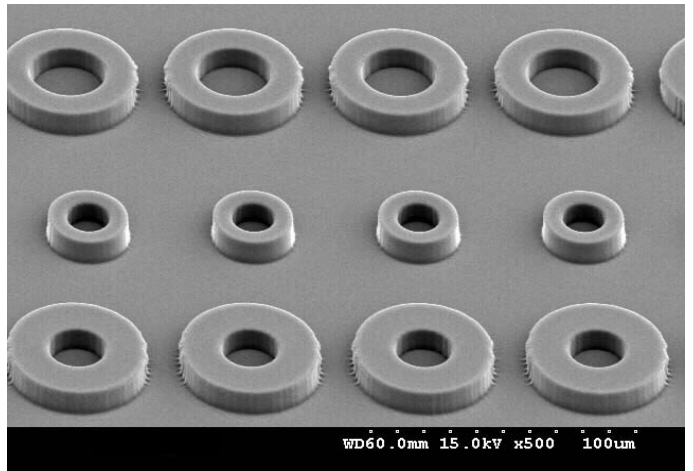


Figure 21.3.4: SEM micrograph of a set of polymer cups with various dimensions.

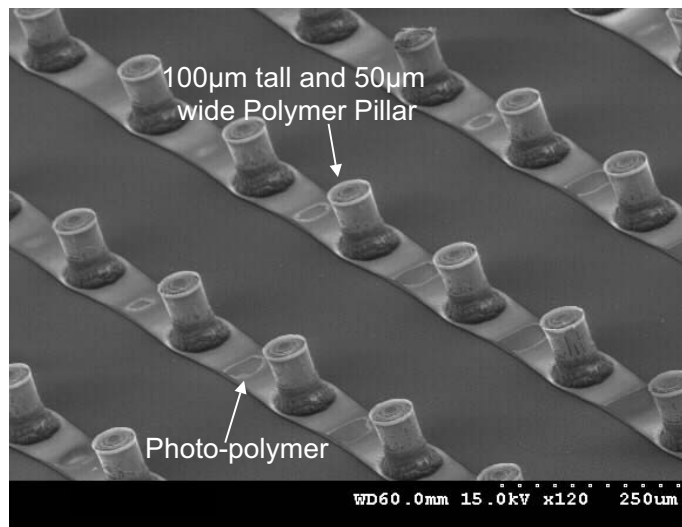


Figure 21.3.5: SEM micrograph of polymer pillars fabricated on the photo-polymer (material used to fabricate a volume grating coupler).

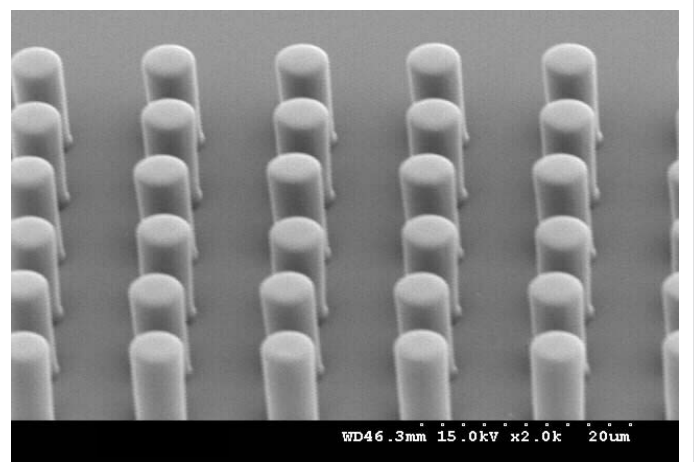


Figure 21.3.6: SEM micrograph of 5µm wide polymer pillars distributed on a 12µm pitch (<10µm pitches are possible). Pillars are photo-defined using the polymer Avatrel.

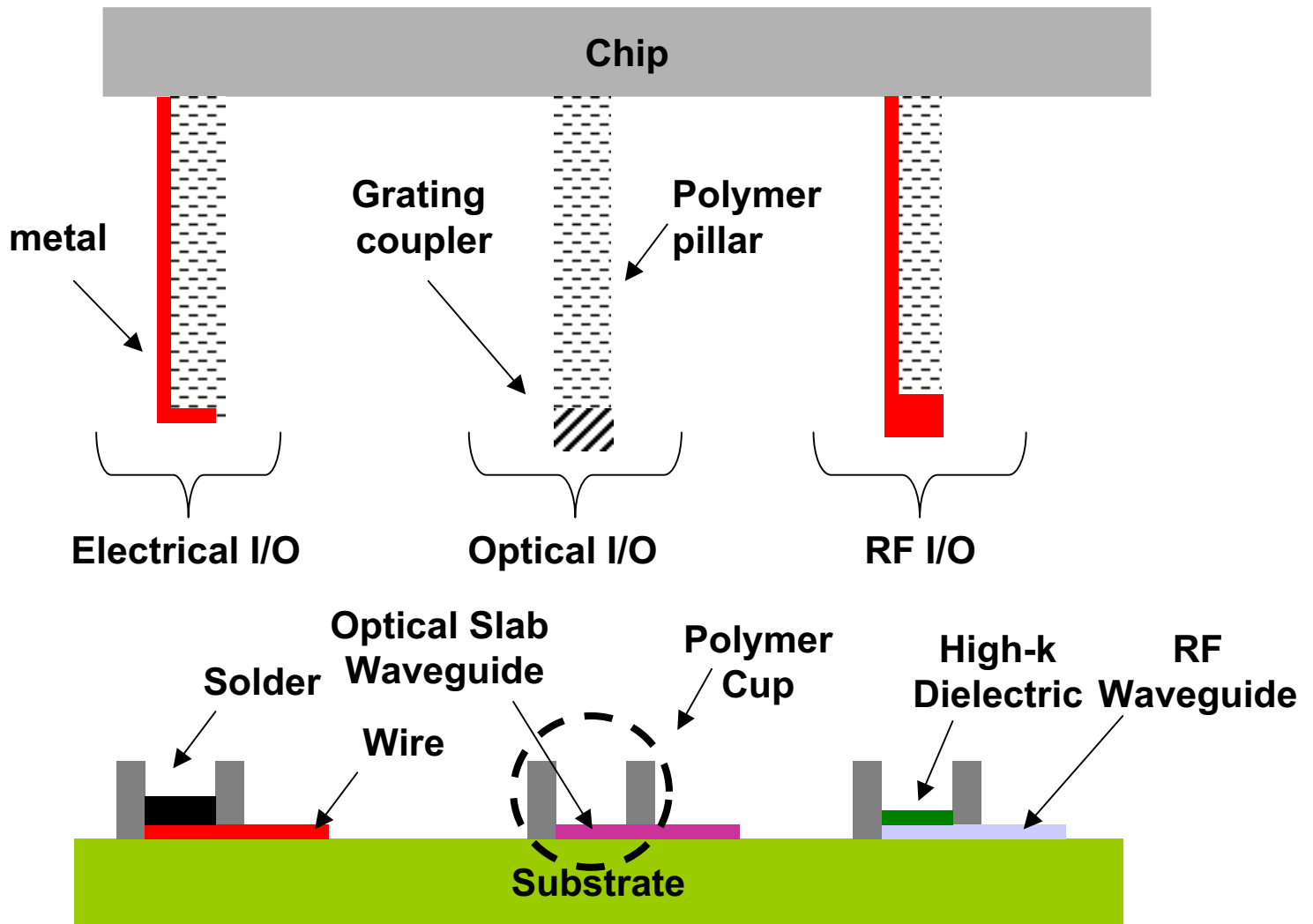


Figure 21.3.1: Possible interconnection technologies feasible through water-level Sea of Polymer Pillars I/O interconnects.

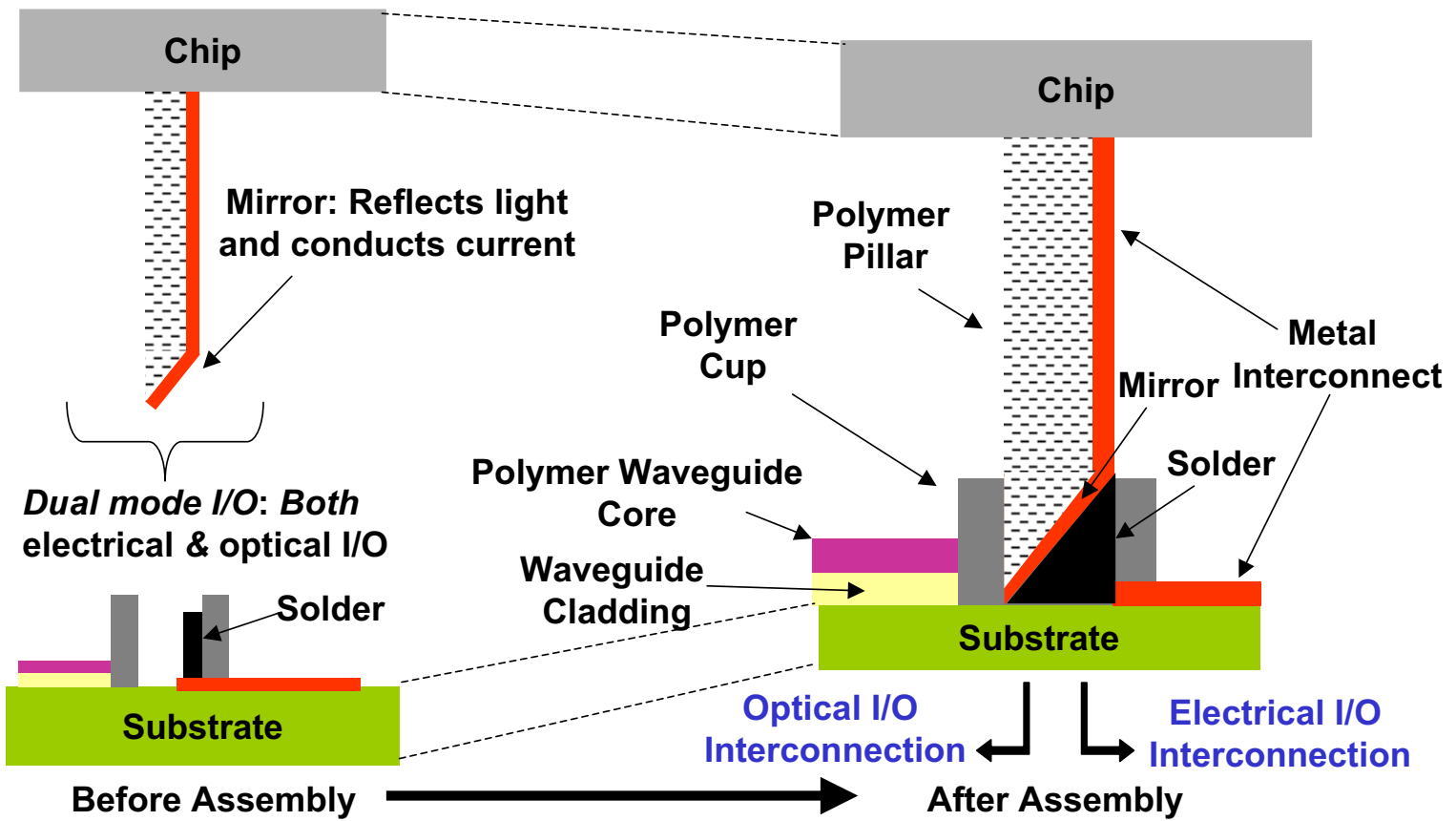


Figure 21.3.2: Illustration of dual-mode (heterogeneous) electrical-optical I/O interconnect. The left side of the pillar allows for optical interconnection while the right side allows for electrical interconnection.

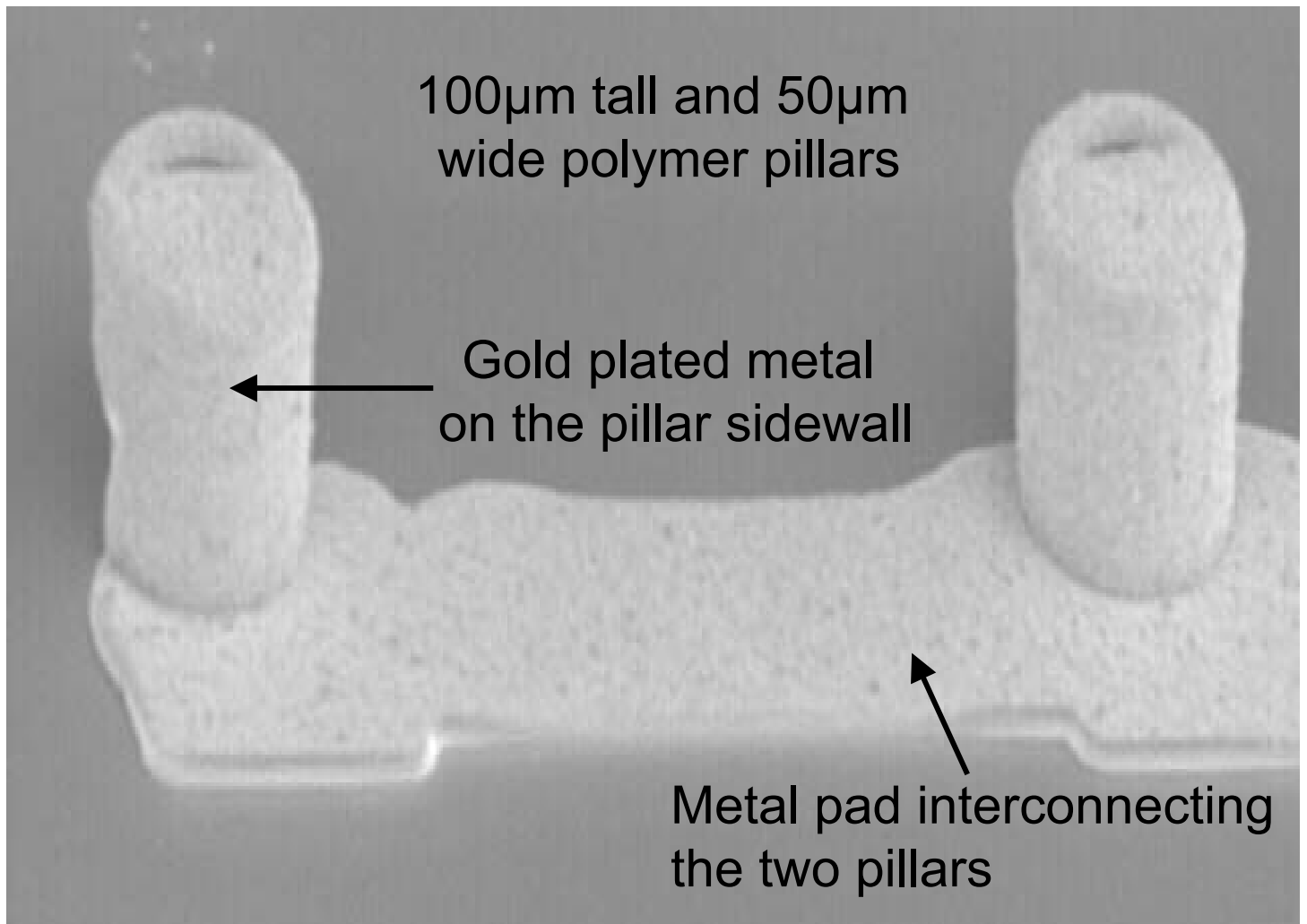


Fig. 21.3.3: SEM micrograph of a pair of interconnected polymer pillars metalized with gold plating.

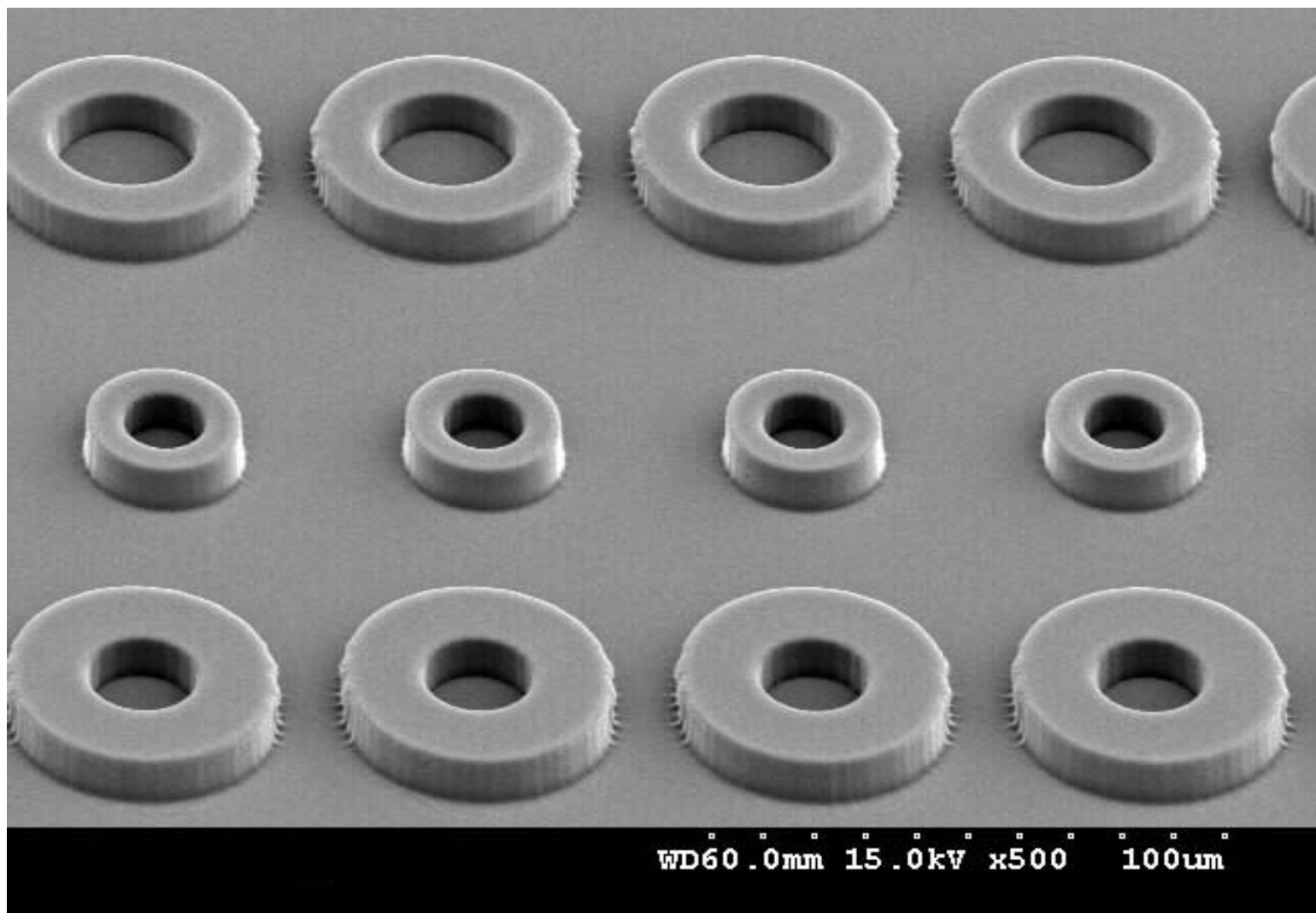


Figure 21.3.4: SEM micrograph of a set of polymer cups with various dimensions.

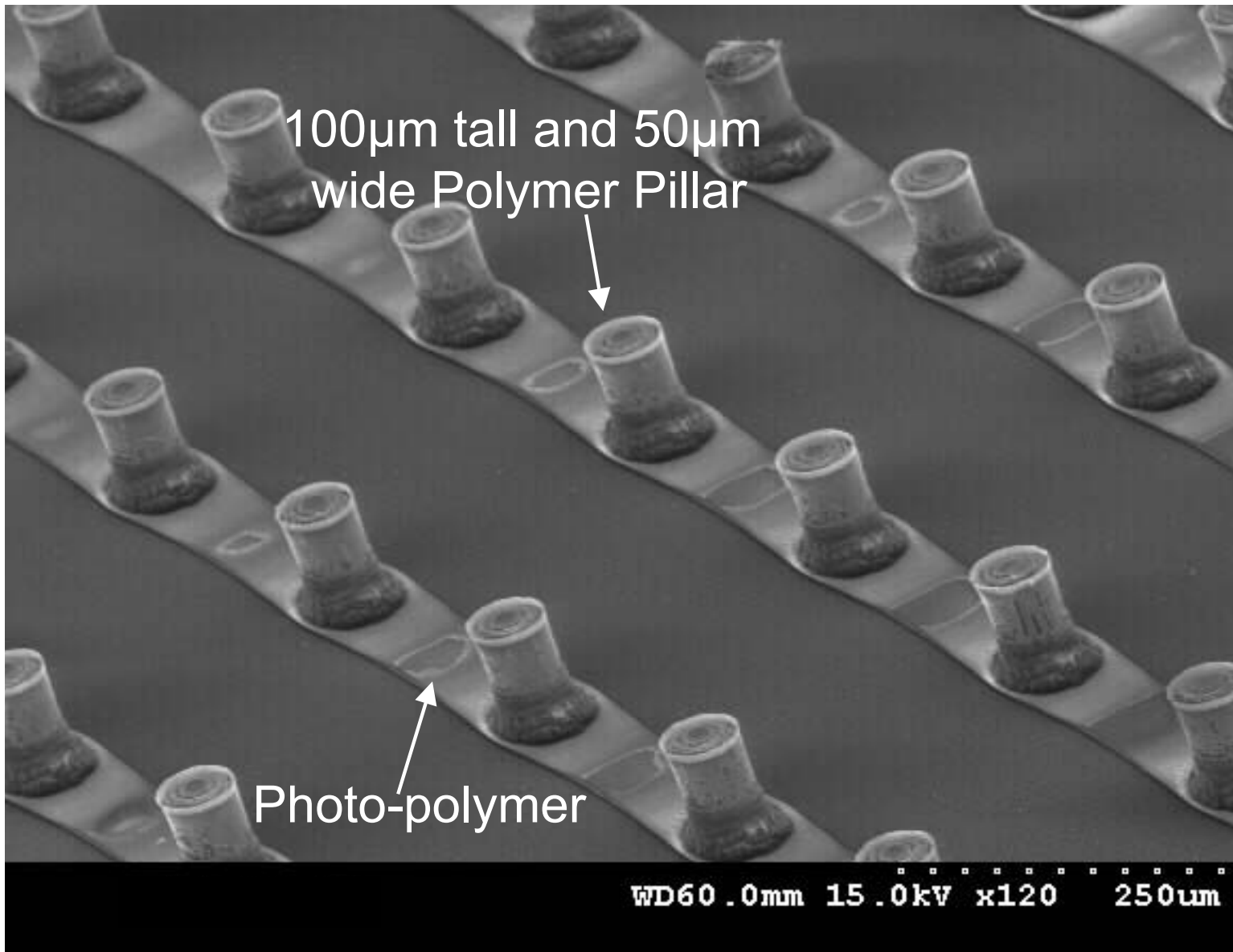


Figure 21.3.5: SEM micrograph of polymer pillars fabricated on the photo-polymer (material used to fabricate a volume grating coupler).

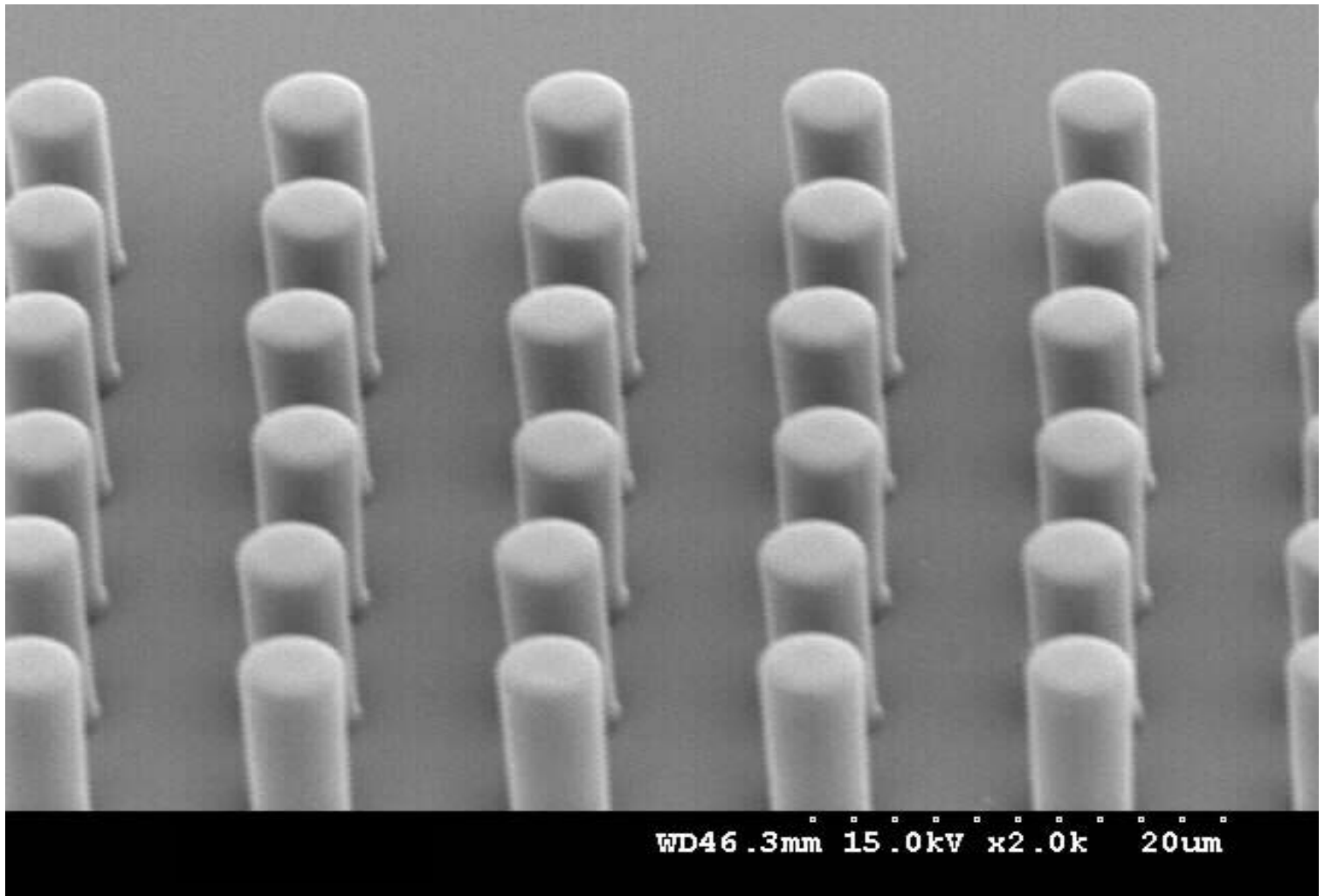


Figure 21.3.6: SEM micrograph of 5 μ m wide polymer pillars distributed on a 12 μ m pitch (<10 μ m pitches are possible). Pillars are photo-defined using the polymer Avatrel.