Ultra High I/O Density Package: *Sea of Leads* (*SoL*)[1]

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Abstract

Sea of Leads (SoL) is a novel ultra high input/output (I/O) density package (>10^4 x-y-z compliant leads per cm^2) that provides high bandwidth and high current distribution capacity for a system-on-a-chip (SoC). A prototype SoL with 12,000 leads per cm^2 has been designed and fabricated using our compliant wafer level package (CWLP) processing approach. The I/O density of the package is maximized by designing various lead lengths as a function of the necessary in-plane mechanical compliance, which increases linearly from the center. In addition, the leads are oriented along the die's local directions of expansion providing a higher degree of compliance. Two different lead lengths (53 μm leads on a 80 x 80 μm square lattice and 106 μm leads on a 80 x 160 μm rectangular lattice) totaling 12,000 leads per cm^2 are distributed across a 1 cm^2 die. SoL promises the capability of meeting high current (>350 A) and high I/O bandwidth requirements as far ahead as the 35 nm generation node (year 2014) SoC. In essence, SoL extends wafer level batch processing of multilevel interconnects networks to include chip I/O leads.

Key Words: sea of leads (SoL), compliant wafer level package (CWLP), system-on-a-chip (SoC).

I. Introduction

High power and high input/output (I/O) bandwidth requirements of future chips will place stringent demands on packages. For example, the 1999 International Technology Roadmap for Semiconductors (ITRS) projects that 35 nm generation (year 2014) high performance and cost performance chips will dissipate 183 W and 115 W, respectively, from a 0.5 voltage power supply [1]. This fact translates into requiring the package to deliver 366 A and 230 A for these two generic chips, respectively. In addition, the package must support the propagation of high frequency electrical signals (>2 GHz), which is an important requirement since the overall system performance will be a function of how well the package and interconnects perform at very high frequencies. Finally, not only do future packages have to be high performance but they must also be low cost.

Sea of leads (SoL) is proposed as an enabling packaging technology for current and future semiconductor packaging demands. SoL is an array of x-y-z compliant leads (>10^4 per cm^2) characterized by minimal electrical parasitics suitable for high frequency and high current transmission. In addition, SoL fabrication utilizes wafer level processing for low cost manufacturing. This paper will also present a novel mechanical design methodology that enabled the fabrication of an SoL with 12,000 leads per cm^2 using compliant wafer level package (CWLP [2]) processing. Using SoL, this package is projected to far exceed the 1999 ITRS 35 nm generation projection for any packaging technology in both I/O density and cost [1].

This paper will begin by discussing the fabrication and manufacturing of SoL as well as highlight its cost advantages in Section II. Section III will present a detailed description of the novel mechanical design methodology that enabled fabrication of the 12,000 leads per cm^2 package. The section will address how the x-y-z compliant lead density was maximized based on mechanical (compliance) constraints as well as the orientation of

[1] This work was sponsored by the Interconnect Focus Center (IFC) and funded in part by MARCO contract B-12-M00 and DARPA grant B-12-D00.

the leads perpendicular to the die's contour of expansion for higher degree of compliance. Section IV will discuss the electrical opportunities of SoL. Finally, Section V is the conclusion.

II. SoL and CWLP Manufacturing and Fabrication

Every CWLP fabrication step involved in manufacturing SoL is a monolithic process step [2]. The fabrication of SoL promptly begins following conventional wafer level front-end and back-end processing as is schematically depicted in Figure 1. With only three masking steps, SoL is fabricated and is ready for wafer level functionality testing and burn-in . As a result, an SoL can be manufactured and tested in the same foundry where the wafer is fabricated. The first step in the packaging process is to spin coat a compliant interposer on the wafer to a typical thickness of 25 µm. For this package, BFGoodrich's Avatrel^{TM} 2000P photodefinable polymer was used. This polynorbornene type polymer provides a low stretch tensile of 0.5 GPa and a coefficient of expansion (CTE) of 50 ppm. In addition, its low electrical dielectric constant of 2.6 permits minimal signal degradation due to minimal lead parasitic capacitance. Following the polymer cure, vias are etched in the polymer to expose the die pads using the first masking step. Next, a titanium/copper/titanium (Ti/Cu/Ti) or a titanium/gold/titanium (Ti/Au/Ti) seed layer is deposited on the wafer. The top and bottom Ti layers provide strong adhesion between the Cu or Au and the surrounding material. A thick photoresist layer is then deposited on the Ti layer to pattern the compliant leads. Using the second masking step, the in-plane x-y-z compliant leads are monolithically patterned in the photoresist across the wafer. Thus, using a 300 mm (12 inch) wafer, fabricating 12,000 leads per cm^2 translates into fabricating more than 8.75 million leads in a massively parallel fashion across the wafer in a series of batch processing steps. The leads could either be copper (Cu) or gold (Au), the latter being more ductile and reliable. The 10 µm thick leads are fabricated by electroplating on the exposed Cu or Au seed layer. After electroplating, the photoresist is removed and a new layer of resist is deposited and patterned with the solder bump pattern using the third and final masking step. The tin/lead (67Sn/33Pb) alloy bumps used for this package are 30 µm in diameter and 30 µm in thickness. The solder bumps are electroplated on the board side of the leads. Next, the wafer is placed in a reflow oven to wet the solder. Finally, the sacrificial layer is removed and the exposed Ti/Cu/Ti or Ti/Au/Ti seed layer is etched away. This concludes the fabrication of SoL. It should be noted that the final package is a chip-*size*-package (CSP).

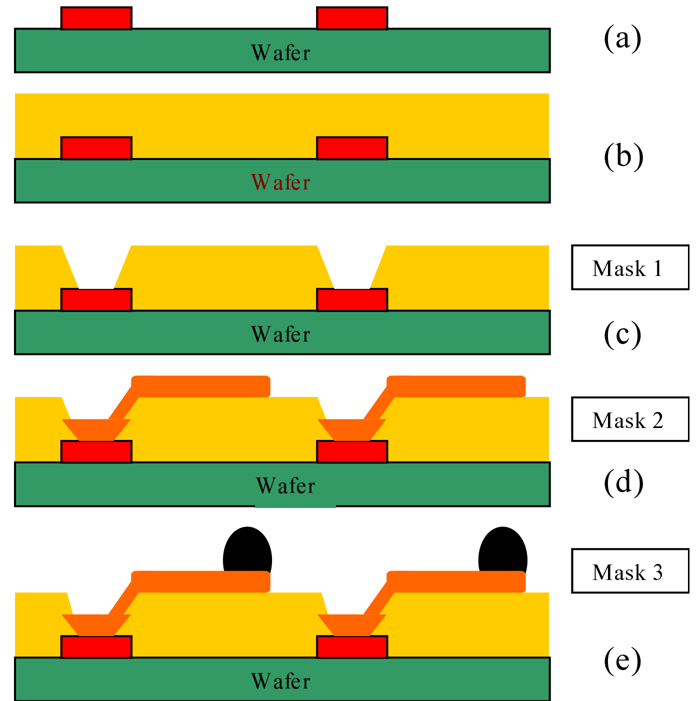

Figure 1: SoL fabrication using CWLP processing. After conventional wafer fabrication and on-chip metalization, the die pads are exposed (a). Next, a compliant polymer in spin coated (b) and etched using the first masking step (c). The compliant leads are next plated on the wafer using the second masking step (d). Finally, the bumps are plated in the leads using the third and final masking step (e).

At this point, the wafer is ready for *wafer level* functionality testing and burn in [2] to identify the known good packaged die (KGPD) while still intact to the wafer. With a low enough modulus polymer, there is enough transverse compliance to allow good electrical contact between the leads and the pads on the testing board. Once all testing is complete, the wafer is finally ready for scribing and the individual CWLPs are ready for assembly. No underfill is needed during assembly because the x-y-z compliant leads in SoL are designed to stretch and contract during thermal cycling to provide the necessary in-plane (x-y) compliance due to the CTE mismatch between the IC and the printed circuit board (PWB). The CTE of the polymer can be neglected because of its low modulus.

III. Mechanical Design of the 12,000 Leads per cm^2 SoL Package

As stated earlier, SoL is fabricated with only three masking steps after IC manufacturing. As a result, this allows the fabrication of ultra high I/O density leads (>10^4 per cm^2) with little change in manufacturing time, processing, and cost [3]. As a result, manufacturing a CWLP with 12,000 leads per cm^2 will demand little more than a CWLP with 100 leads per cm^2. This presents a strong motivation for designing and fabricating ultra high I/O density packages to meet the electrical demands of a SoC. However, the I/O density of a CWLP is constrained by the in-plane mechanical compliance necessary to accommodate the CTE mismatch problem.

This section will begin by illustrating how the I/O density of this package was maximized based on mechanical constraints and discussing the benefits gained when the leads are orientated along the die's directions of expansion. Before this discussion, it is expedient at this point to examine the CTE mismatch problem between the chip and PWB/substrate, which may be modeled with the following equation

$$\mu = \Delta T(\alpha_{pwb} - \alpha_{si})x \qquad (1)$$

where μ is the net displacement (compliance) a lead will flex in microns, α is the CTE of the material noted in subscript (PWB or silicon), ΔT is the change of temperature, and *x* is the radial distance from the center of the die. Notice that this model assumes that the board and the chip will be at the same temperature and thus accounts for the worst case situation. Equation (1) vividly illustrates that compliance is a linear function of position, which is a very important observation because it indicates that leads placed on the perimeter of the package will undergo more flexing from thermal mismatch than leads placed around the center of the package. The general lead geometry is shown in Figure 2 and its compliance is determined by L, linear length, r, radius, and θ, the angle between the via and solder bump, and its width.

In general, larger leads provide more compliance than smaller ones. With this in mind, the number of leads placed on a chip of a specific area can be increased by placing smaller less compliant leads at the inner region of the package and larger more compliant leads at the outer region of the package. This task was accomplished by dividing the chip area into three regions as shown in Figure 3 and calculating the maximum compliance needed in each region as shown in Table 1. Based on these numbers, it was determined that the leads in regions 1 and 2 of Figure 3 could be designed to be 53 μm in length while the leads in region 3 to be 106 μm in length.

This design procedure maximized the I/O density by allowing the design of smaller leads in the inner region of the package and larger leads near the perimeter. If this design procedure was not followed, the leads in region 1 and 2 of Figure 3 would have one half the total number of leads and thus the maximum package density would be 7,000 leads per cm^2 instead of 12,000 leads per cm^2. Figure 4 illustrates and SEM image of one quadrant (3,000 leads) of the fabricated SoL.

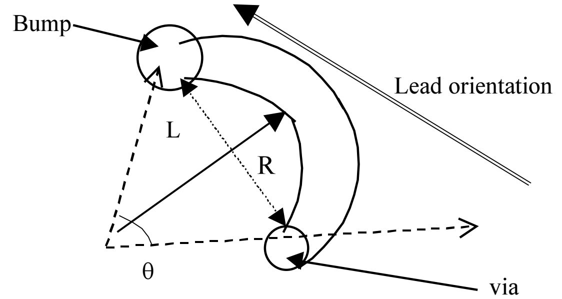

Figure 2: General compliant lead geometry. R, radius, L, linear length, and θ, angle between bump and via dictate the compliance of the lead.

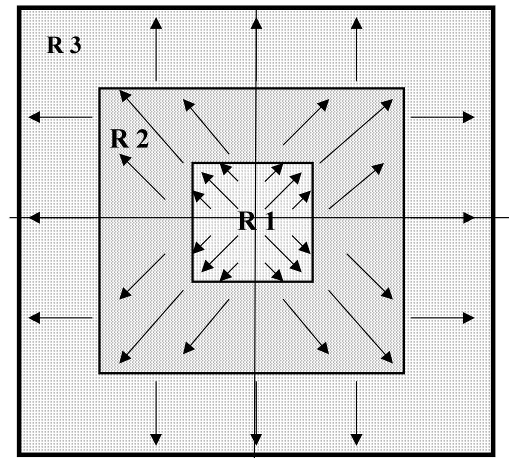

Figure 3: Patitioning the package into three regions (R1, R2, R3) to maximize the I/O density. Also, the arrows point along directions of chip expansion and lead orientation.

Another feature of this package is orientation of the leads perpendicular to the die's/PWB's contours of expansion to achieve a higher degree of compliance flexing radially outward. Figure 2 defines the lead orientation as a vector pointing from the via to the bump. Placing the leads perpendicular to the contours of expansion utilizes the most compliance out of the lead. Figure 5 is an SEM image showing how the leads are oriented at the chip's center. Although the package has different

lead sizes and various orientations, the final package has 12,000 I/O leads per cm^2 on 80 x 80 μm square lattice and 80 x160 μm rectangular lattice and two different lead lengths of 53 and 106 μm for simple PWB layout as shown in Figure 6. The package is also less than 70 μm in thickness providing an ultra thin and light weight package. Table 2 summarizes the various dimensions on the package.

Table 1: Summary of the mechanical properties in each of the three package regions of the SoL 12k leads per cm^2 pasckage.

	Region 1	Region 2	Region 3
Dimension (mm x mm)	4 x 4	8 x 8	10 x 10
Maximum Compliance (μm)	8.5	17	23
Lead Pitch (μm)	80	80	80 & 160
Number of Leads	5,000	5,000	2,000

Table 2: Various dimensions of the fabricated package.

Pad Size	20 x 20 μm	Lead Width	22 & 19 μm
Pad Pitch	80 μm	Lead Length	53 & 106 μm
Via Diameter	18 μm	Bump Diameter	30 μm
Polymer Thickness	23 μm	Bump Height	30 μm

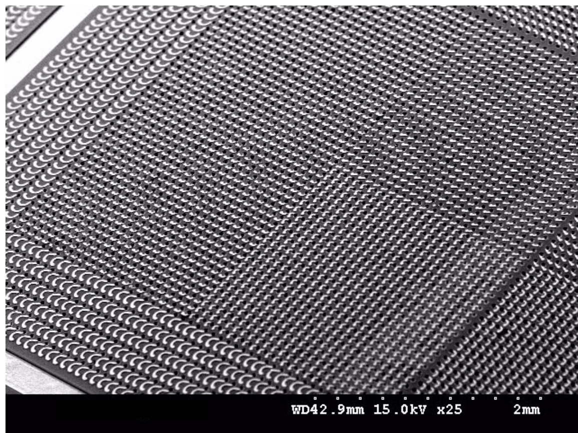

Figure 4: SEM image of one quadrant (~3,000 leads) in the fabricated SoL 12k leads per cm^2 package.

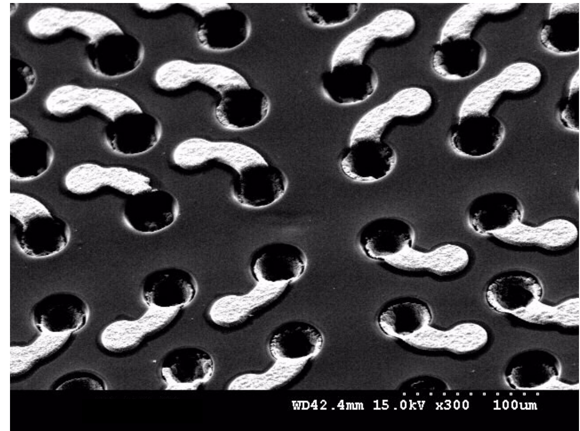

Figure 5: SEM image illustrating the orientation of the leads (before plating solder bumps) perpendicular to the contours of expansion for higher degree of compliance.

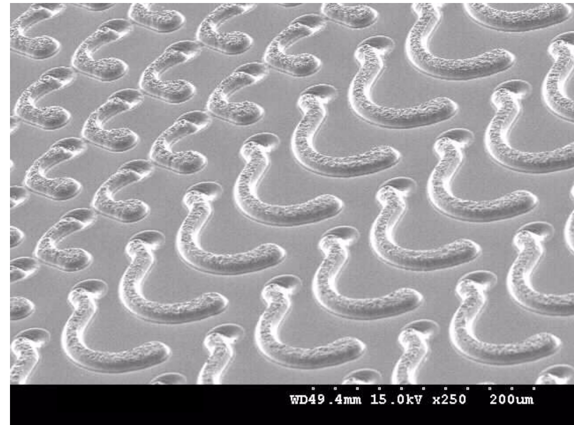

Figure 6: SEM image showing the 53 μm leads on a 80 x 80 μm square lattice and the 106 μm leads on a 80 x 160 μm rectangular lattice. The 106 μm leads are placed in region 3 of Figure 3 and the 53 μm leads are placed in regions 2 and 1. This distribution maximized the package's I/O density.

IV. SoL Application to 35 nm Generation Node SoC

Table 3 summarizes some of the projected 35 nm generation chip characteristics for hand held, cost performance, and high performance chips [1] and the new number of I/Os that could be attained based on SoL with 12k leads per cm^2. Clearly, the number of I/Os available by using SoL is more than ten times greater than the projected I/O count. This density of leads would provide better power distribution by substantially decreasing on-chip IR voltage drops

Table 3: Projected chip parameters of various market sectors and new I/O count based on SoL 12k leads per cm^2.

Market Sector	Hand Held	Cost Performance	High Performance
Size (cm^2) [1]	0.9	3.51	9.37
Power (W) [1]	2.7	115	183
Voltage (V) [1]	0.3	0.5	0.5
Current (A) [1]	9	230	366
I/O Count [1]	1,167	3,541	8,758
I/O Count Using SoL	10,800	42,120	112,440

and reducing the on-chip wiring area resource needed for power distribution [4]. In addition, SoL could more easily support the capability of more than one voltage supply which many be required for a mixed signal SoC. Because the x-y-z compliant leads are short, they provide minimal parasitics (<15 mΩ, < 4 pF, < 0.1 nH) further improving power distribution. The leads exhibit a self resonance frequency in the tera-hertz range proving the capability of supporting very high frequency signals and large on/off chip bandwidth. As a result, SoL is a packaging technology that intends on *enhancing* SoC performance by using ultra high I/O interconnection density.

V. Conclusion

A package with 12,000 leads per cm^2 has been designed and fabricated based on Compliant Wafer Level Package (CWLP) processing approach. This results in an ultra high density array of I/O interconnections called Sea of Leads (SoL). Novel mechanical design methodologies were used to maximize the compliance and I/O density this package. The I/O density was maximized based on the required in-plane mechanical compliance as well as the orientation of leads with respect to the die's contours of expansion for a higher degree of compliance. SoL fabrication requires only three masking steps after the completion of IC fabrication. As a result, SoL is a low cost packaging solution for the 35 nm generation node (year 2014) high power and high performance System-on-a-chip (SOC). The small electrical parasitics present in SoL permits the package to distribute more than 350 A and high frequency signals with minimal ground bounce and signal degradation. In addition, SoL can reduce on-chip IR voltage drops and on-chip interconnect area for power distribution. As a result, SoL *enhances* SoC performance by utilizing ultra high I/O interconnection density.

References

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Acknowledgements

The authors wish to thank the Interconnect Focus Center (IFC), supported by MARCO and DARPA, for funding this work (http://www.ifc.gatech.edu). In addition, the authors wish to thank BFGoodrich and Ed Elce of BFGoodrich's microelectronics material division for supplying the polymer samples and technical assistance.