# Chip Integration of Sea of Leads Compliant I/O Interconnections for the Ultimate Enabling of Chips with Low-k Interlayer Dielectrics

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## Abstract

This paper describes the process and assembly integration of Sea of Leads (SoL) with an Intel chip. A primary goal of the research was to study the issues involved in reconciling the fabrication and assembly requirements of compliant leads, such as SoL, with those of standard semiconductor processes and standard chip assembly techniques. The study was motivated in-part by the potential failure of the low-k interlayer dielectric in microprocessors as a result of high mechanical stresses due to the coefficient of thermal expansion (CTE) mismatch between the chip and the board. SoL, and other compliant interconnections, mitigate this problem by mechanically decoupling the chip and the board. We show that while the compliant leads offer advantages over C4 technology, there is much to consider during the series of steps needed to transform the fully intact dice at the wafer level to dice that are assembled onto the board. The use of an encapsulation film over the leads during wafer sawing is shown to be necessary for slippery leads and other free-standing compliant leads. Compliant leads on the edges of the chip tend to extend beyond the active region of the dice. The use of the correct flux when the leads are encapsulated with nickel-oxide nonwettable layer is shown to be essential for a successful wafer-level solder reflow. Thermo-compression bonding is shown to be a promising assembly technique for SoL because it can overcome the problem of non-uniform height of the solder bumps on the board.

## I. Introduction

In order to improve the electrical performance of microprocessors, semiconductor manufacturers are seeking to reduce the dielectric constant of the interlayer-dielectric separating the Cu conductors that form the chip's multilayer interconnect network. The processes employed to produce this low interlayer dielectric constant material (low k) also tend to reduce its mechanical strength. In present technology, the mechanical strength of the dielectric is low enough that is can cause failure during microprocessor use. The driving force for this failure is the mechanical stress imparted on the dielectric due to the thermal expansion mismatch between the silicon die and the composite substrate (often engineered to be expansion-matched to copper) as the system goes through thermal excursions. Therefore, architectural changes that minimize this stress are industrially attractive.

This paper presents the key results from the process integration of Sea of Leads (SoL) [1-3] compliant I/O interconnections with an Intel chip. SoL provides compliant electrical I/O interconnects, which act to interconnect the die to a substrate while decoupling the deformations of the two. This decoupling is accomplished by designing the interconnections to behave as mechanical springs [1-10]. A primary goal of the research was to study the issues involved in reconciling the fabrication and assembly requirements of compliant leads, such as SoL, with those of standard semiconductor processes and standard chip assembly techniques. The chips used for these experiments are one of Intel's test chips used to characterize the reliability of various interconnections. The on-chip interconnects were Cu, and the uppermost layer on the chips was a polymer.

The details of process integration of SoL with the Intel chip are described in Section II. Section III describes the issues involved in selecting the correct flux for SoL. Wafer sawing issues are described in Section IV. Finally, the use of thermo-compression bonding to mitigate the solder height variation on the board is described in Section V. Section VI is the conclusion.

## II. Fabrication Details

The details of SoL fabrication on the Intel wafers are described in this section. Intel supplied several 8" Si wafers. Each 8" wafer was sawed into rectangular pieces to accommodate the substrate size limitation of the mask aligners at Georgia Tech. SoL (without embedded air gaps) was fabricated on the Si pieces using the processes described in [1-3]. However, there were some important differences. First, the only polymer film under the leads was the Intel polymer. Thus, the first process step was to sputter a seed layer. All but one Si piece was coated with a Ti/Au/Ti (300 Å/0.2 μm/300 Å) seed layer using a dc sputterer. The other Si piece was coated with a seed layer that yielded slippery leads. The method used to fabricate the slippery leads is identical to the one described in [1] where Ti islands were first patterned over the vias followed by Au blanket coating. Following seed layer deposition and resist patterning, the leads were electroplated. The total thickness of the leads was 10 μm. The leads were electroplated Au and Ni. The Au layer was 8 μm thick, and the Ni layer was 2 μm thick. This was accomplished by first electroplating Au to an 8 μm thickness. Next, Ni was electroplated to a 2 μm thickness. The same resist layer (or mold) used to electroplate the Au layer was used to electroplate the Ni layer. This fabrication process yielded Au leads with Ni coating only at their upper surface. Ni was not plated on the sidewalls of the leads. The purpose of the Ni layer was to ultimately provide a non-wettable surface for the solder and thus, contain the solder during reflow and assembly. However, the use of a polymer on the leads for such a function was previously described [1]. After the leads were plated, the rectangular Si pieces were placed in the RIE and exposed to an $O_2$ rich plasma for approximately 10 min. This process oxidized the Ni layer making it a good non-wettable solder layer. The seed layer was not etched prior to this step. This is important because the seed layer protected the chip's underlying polymer during RIE. Figure 1 is a die micrograph of the Intel chip after the leads were electroplated, and Figure 2 is a higher magnification micrograph of one region on the chip.

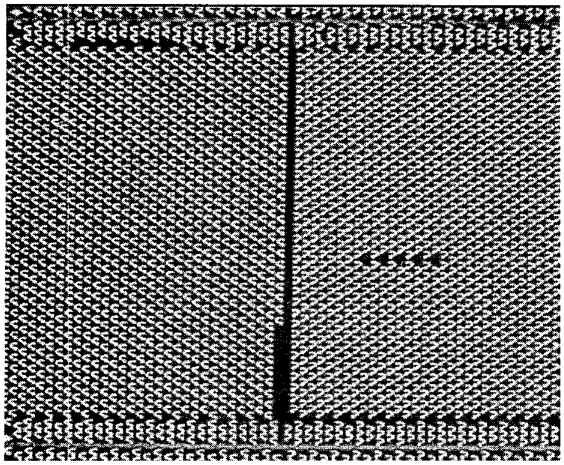

Figure 1: Die micrograph of the Intel chip after electroplating the compliant leads (no solder bumps).

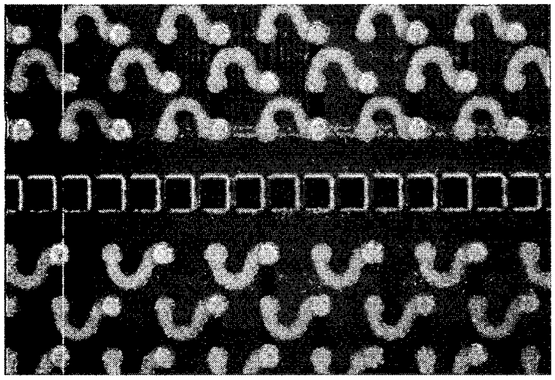

Figure 2: Higher magnification micrograph of an Intel chip with SoL.

A resist layer was spin coated next on the rectangular Si pieces and patterned such that vias were fabricated at the bump end of the leads. Next, the Ni oxide layer was wet etched. Following the etch, the samples were placed in a solder plating solution where 60/40 Sn/Pb solder bumps were plated to an approximate height of 30 µm. Following the plating process, the seed layer was etched. Figure 3 is an SEM micrograph of a lead with a solder bump on its tip.

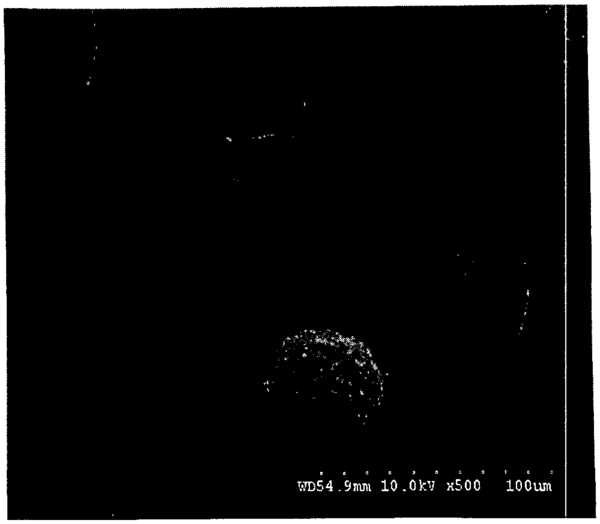

Figure 3: SEM image of a lead with a solder bump on an Intel chip.

### III. Selection of Flux

The fabrication of the leads on the Intel chip was not a difficult task. Once SoL was fabricated, the Si pieces were shipped back to Intel where dicing of the individual chips and assembly took place. The first task was to experiment with solder reflow. A successful solder reflow process requires the use of a correct flux. If the flux is too aggressive, the oxide on the Ni will be removed, and the solder will wick the entire lead. Thus, it was important to select the correct flux for SoL interconnections when Ni oxide is used as the non-wettable surface around the solder bumps. Figure 4 is a micrograph of a set of leads after being placed in a reflow oven when no flux was dispensed on the sample. The bumps do not show evidence of a good reflow. On the other hand, Figure 5 is a micrograph illustrating the bumps when an organic flux was used during the reflow process. The bumps are spherical in shape and confined to the tips of the leads, as desired. Finally, Figure 6 is a micrograph illustrating the consequences of using a more aggressive flux. It is clear that the new flux is too aggressive to be used with the fabricated SoL interconnections because it managed to remove the nickel oxide layer from the Ni surface. This caused the solder to wick most of the lead. Such a scenario would prevent the successful assembly of chips.

Even when the more aggressive flux was only coated on the printed wiring board (PWB), after assembly, the solder somehow managed to wick most of the lead. Figure 7 and Figure 8 are micrographs of the chip and the board, respectively, after assembly and subsequent die detachment from the board. It is clear from the micrographs that the solder wicked the leads. This effect caused essentially no solder bumps to make contact with the pads on the PWB. Another important factor that contributed to the poor contact between the chip and the PWB is height variation (non-uniformity) of the organic board and bumps. Because of these factors, the SoL chip shown in the figure was not assembled successfully. Later in the paper, we will describe how good bonding was attained.

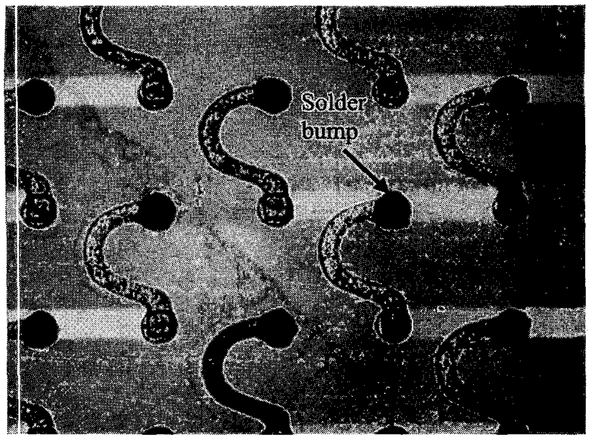

Figure 4: Micrograph of solder bumps on the tips of the leads after reflow. No flux was used in this case.

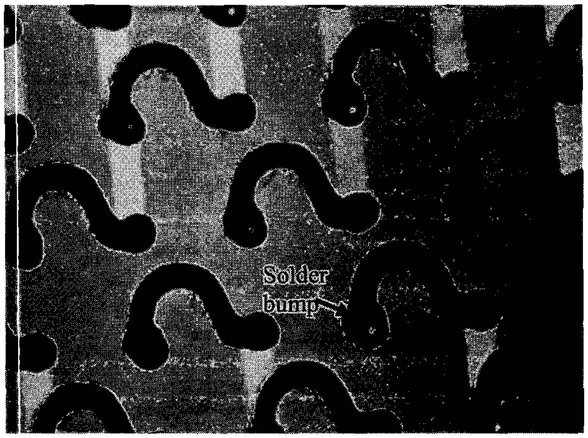

Figure 5: Micrograph of solder bumps on the tips of the leads after reflow. An organic flux was dispensed on the sample prior to reflow. It is clear that the solder is confined to the tips of the leads.

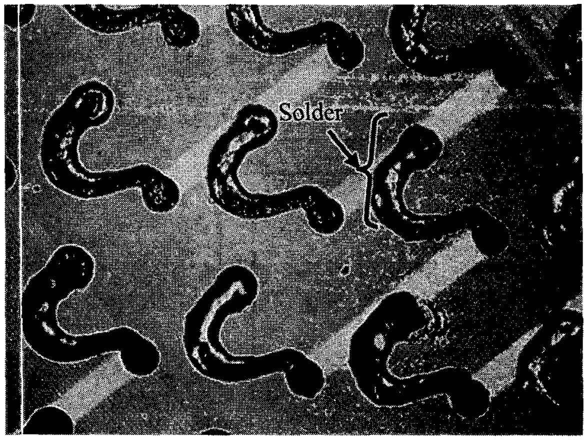

Figure 6: Micrograph of solder 'bumps' on the tips of the leads after reflow. A more aggressive flux was dispensed on the sample prior to reflow. It is clear that the solder wets most of the lead.

The above discussion underscores the difficulty of controlling solder when metallic compliant leads are used. The metal used to fabricate the leads is typically selected from mechanical and electrical performance perspectives. A promising method to control solder during reflow and assembly for planar compliant leads is by surrounding the solder bumps with a dielectric barrier [1].

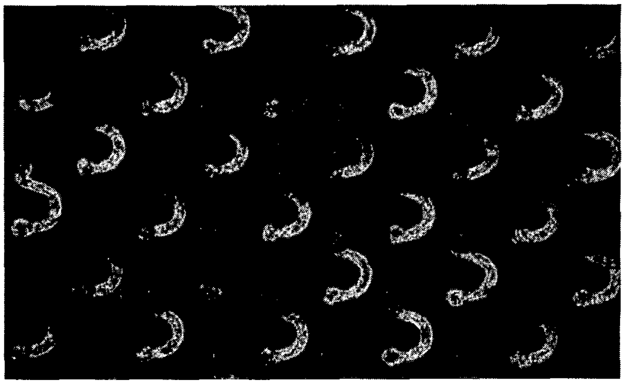

Figure 7: Assembled die showing clear evidence of solder wicking due to the use of a flux that is too aggressive.

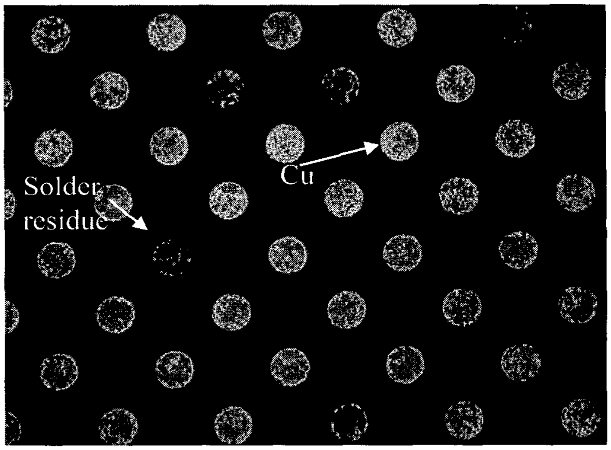

Figure 8: Micrograph of a portion of the PWB after chip detachment (Figure 7). The image illustrates that most of the Cu pads on the board made little to no contact with the solder on the leads.

## IV. Compatibility with Wafer Sawing

### A. Encapsulation of the Leads

Once the proper flux was selected, the next issue was dicing: how to dice a wafer with compliant leads on its surface. The challenge is that high pressure deionized (DI) water is used during the sawing process. As a result, it was important to somehow protect the leads from such a high pressure water stream. This led to encapsulating the leads with a material during the sawing process. This material had to meet the requirements of being transparent to mitigate the alignment of the saw to the saw streets on the wafer. Moreover, the material had to facilitate easy removal. Some of the thick resists used in typical MEMS fabrication were the first candidates for use as the encapsulating material. However, most were not sufficiently transparent to the vision system used on the sawing equipment. In addition, most could only be removed through a dry etch.

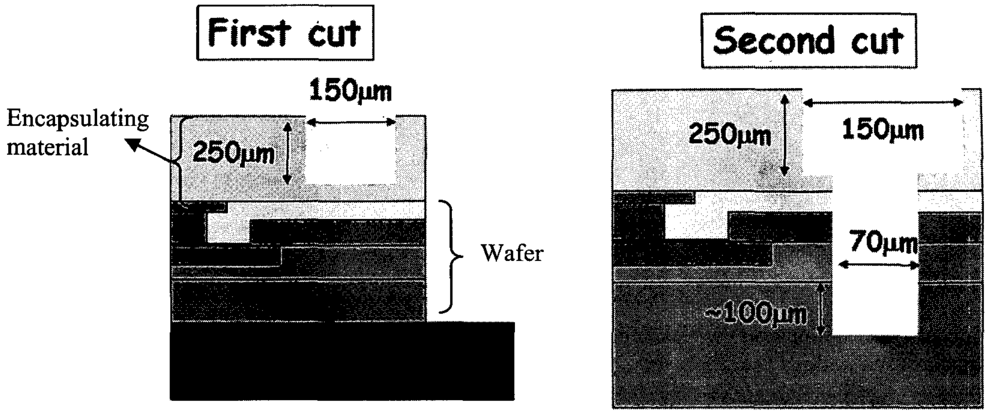

Figure 9: Wafer sawing details.

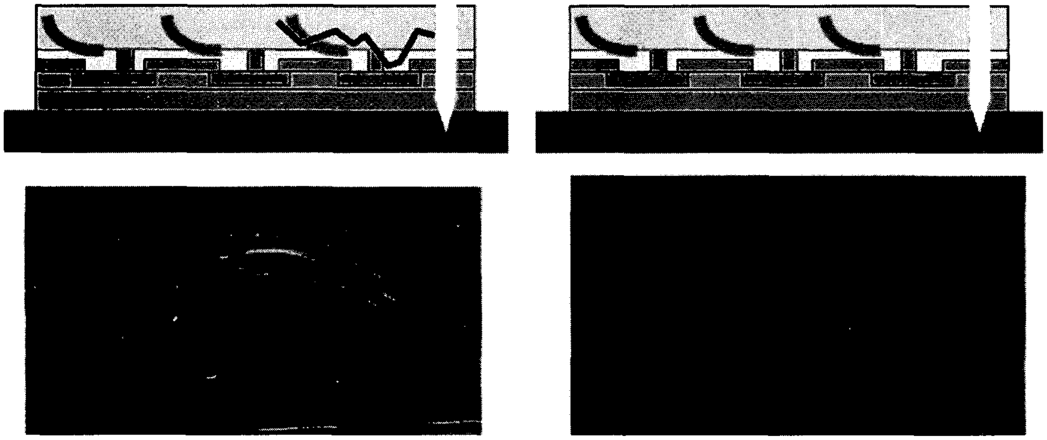

Figure 10: This figure illustrates the importance of selecting the proper encapsulating material during wafer sawing. The figure on the left illustrates results from using one material. It is clear that severe damage was caused to the material. The figure on the right illustrates the results of sawing using a different material.

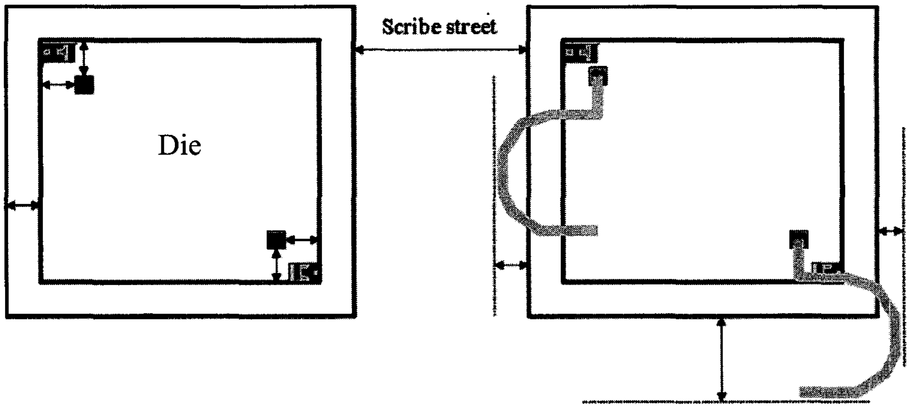

Figure 11: Schematic illustrating the saw street reduction problem.

Figure 9 is a schematic illustrating how the dice were sawed after being encapsulated. First, the saw was used to cut through most of the encapsulating material. Next, the saw was used to scribe 70 μm into the wafer. Finally, a third saw singulated the dice. It was important to also select a material that is soft enough to absorb the stress induced during the sawing process. Figure 10 compares the results of sawing on two different encapsulating materials. The material shown on the right in the figure was selected as the best material to encapsulate the wafer with.

Based on these experiments, it was determined that the encapsulating material was not needed for the 'adhered' leads [1-3] but was necessary for the partially slippery leads [1-3]. When the encapsulating film was not used, some of the slippery leads delaminated off the wafer.

### B. Saw Street Reduction Problem

An issue encountered during the sawing process was saw street reduction. This problem is illustrated in Figure 11 and can be described as follows: the compliant leads at the edges of the die extend beyond the active region of the die. As a result, they extend well into the saw streets between the dice. This problem was discovered during the sawing process. As a result, it was not possible to compensate for it during layout design. The position of the saw streets were slightly shifted to compensate for this effect. Figure 12 is a micrograph of the sawed streets after being shifted.

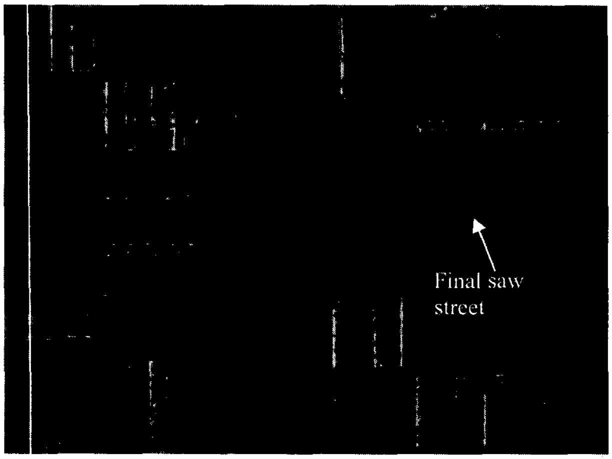

Figure 12: Micrograph of the sawed streets.

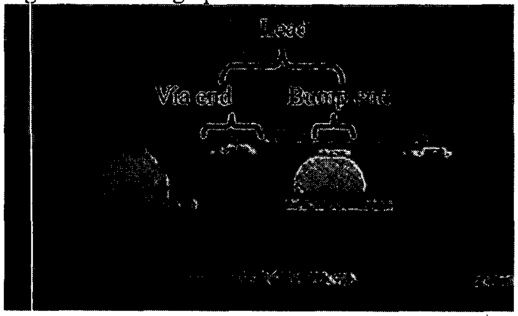

Figure 13: Micrograph illustrating the problem associated with solder bump height non-uniformity on the board. The bump on the left makes good contact to the tip of the compliant lead while the bump on the right does not.

## V. Assembly Related Challenges

Now that the solder reflow process was optimized, and the wafer sawing process was established, the next task was assembly. There were two types of boards used for SoL attachment (one with and one without solder bumps). The height variation of the solder bumps on the board was relatively large. Even the boards without solder bumps were non-planar. As a result, when the chips were flip-chip bonded (with no applied force during solder reflow), only a few leads managed to make contact with the solder/pads on the board. This yielded the poorly bonded sample shown in Figure 8. Figure 13 illustrates that some of the leads made good contact. In order to mitigate this problem, thermo-compression bonding was used. The assembly flow diagram of this process is shown in Figure 14. First, the organic flux described previously was coated on the PWB. Next, the SoL chips were bonded using thermo-compression. The SoL chips used for this experiment contained leads without solder bumps on their tips. Instead, a patch of Au film equal in width to the bump was fabricated on the tip of each lead. A proper bonding profile, which consists of both temperature and force, had to be identified. As a result, two different bonding profiles were tested and are shown in Figure 14. The difference between the two profiles is the time duration at the peak temperature.

In order to characterize the mechanical interconnection of the leads and thus, the chip to the solder bumps on the PWB, a shear force was applied on the chips following their attachment. Figure 15 illustrates the die and board after detachment. Each lead broke into two segments as a result of the applied shear force. Other similar experiments yielded similar results. These experiments are significant because they demonstrate that good mechanical interconnection was attained between the SoL chip and the highly non-uniform solder bumps.

## VI. Conclusion

This paper described the process integration of Sea of Leads (SoL) chip I/O interconnections with an Intel chip. The primary objective of this research was to illustrate some of the key issues required to reconcile the fabrication and assembly requirements of compliant leads, such as SoL, with those of standard semiconductor processes and standard chip assembly techniques. The leads were fabricated using the processes described in [1-3]. Au leads with a nickel oxide non-wettable top surface were fabricated to confine the solder bumps to the tips of the leads. It was experimentally verified that the use of the proper flux during solder reflow and assembly was essential in preventing solder from alloying the entire surface of the leads. In addition, it was shown that the leads fabricated on the edges of a die tend to extend beyond the active region of the die. This problem was mitigated by shifting and reducing the width of the saw streets. The use of an encapsulating film over the leads during wafer sawing was necessary for the slippery leads. Finally, using thermo-compression bonding, SoL dice where successfully attached to the non-planar boards.

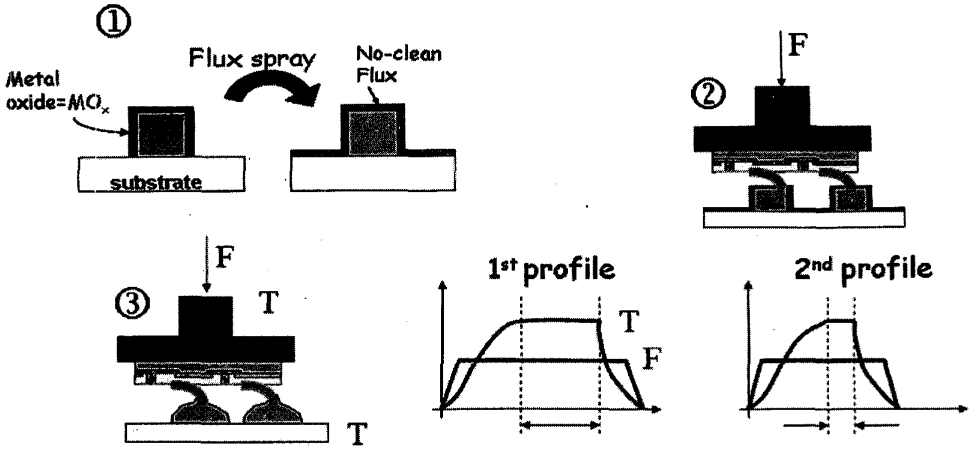

Figure 14: Schematic illustrating the process flow diagram of thermo-compression bonding and the two bonding profiles used.

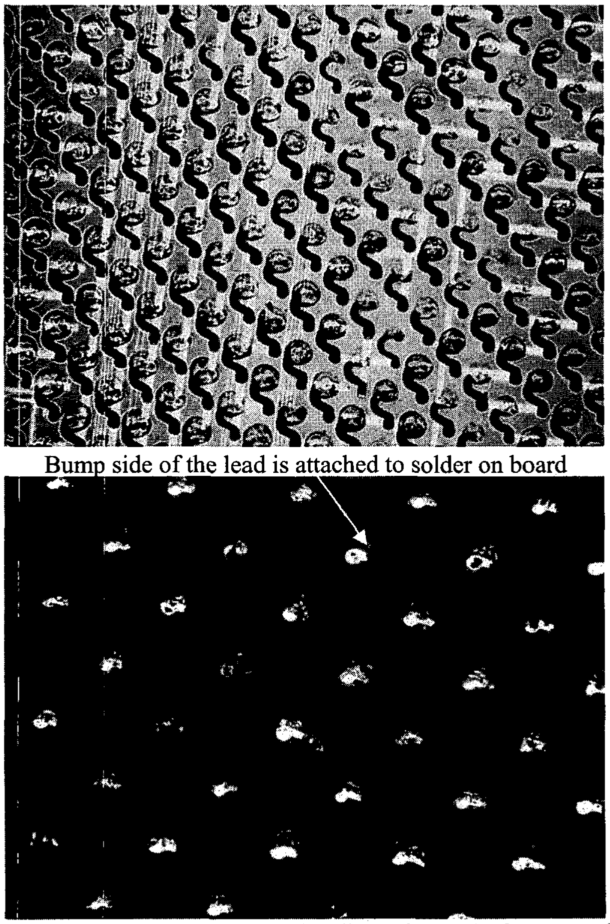

Figure 15: Micrographs of the die and board after assembly and application of shear force on the assembled die under the second bonding profile of Figure 14. The micrographs illustrate that the leads made good contact with the bumps on the board (a segment of each lead remained attached to the bumps on the PWB after the die were sheared off).

## Acknowledgments

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