Integrated Electrical, Optical, and Thermal High Density and Compliant Wafer-Level Chip I/O Interconnections for Gigascale Integration

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Abstract:

The integration of more than a billion transistors on a chip, or gigascale integration (GSI), imposes significant constraints on interconnection and packaging of such chips. Specifically, the need for hundreds of amperes of dc current, very high Input/Output (I/O) bandwidth, high heat removal capability, and the interconnection of Si chips with low-k interlayer dielectric to boards with higher coefficient of thermal expansion (CTE) will challenge all aspects of conventional packaging and interconnection. A solution to the above described system level demands is the batch fabrication of high density and mechanically compliant electrical, optical, and thermal chip (I/O) interconnections at the wafer level. Such I/O interconnections are described in this paper.

I. Introduction

Chip Input/Output (I/O) interconnections are crucial in any high performance microsystem: they provide the interface between the chip and board. Not only do these I/Os interconnect the chip to the board mechanically, but they also provide a path for supply current, high frequency signals, and heat to a lesser extent. Each of the four identified interconnection functions (mechanical, dc, signal, thermal) presents a different set of challenges and requires the I/O interconnections to provide a unified solution to these challenges. Today, the chip I/O interconnections are spherical solder bumps, which have replaced wire bonds, and the primary heat removal path is achieved through a back side heat sink.

As the semiconductor industry continues to follow Moore's Law and progresses towards the 18 nm technology node and gigascale integration (GSI) [1], high performance chips will demand higher supply current and bandwidth. To this end, a larger number of power and ground leads will be required, and the integration of microphotonics technology with Si chips will be essential to leverage high I/O bandwidth. Moreover, providing the mechanical interconnection between the chip and the board becomes more challenging as low-k dielectrics are integrated in high performance chips. The coefficient of thermal expansion (CTE) mismatch between the Si chip and the board can cause damage in the low-k interlayer dielectric. Moreover, with the integration of microphotonics technology, it is difficult to maintain optical alignment between the optical devices on the chip and the board during thermal cycling as a result of the CTE mismatch. Problems caused by CTE mismatch may be overcome with the use of mechanically compliant I/O interconnections [2-3]. Finally, the use of heat sinks and fans will no longer be sufficient to remove heat, and thus, new heat removal strategies are required for both single and stacked chips [4].

In this paper, opportunities for integrated electrical, optical, and thermal compliant wafer-level chip I/O interconnections are described. The work presented here is an extension of previously reported results [5-6]. While the primary focus of the paper is the electrical and optical chip I/O interconnections using Sea of Polymer Pillars (SoPP), as shown in Figure 1, the integration and fabrication of surface-normal micropipes for heat removal is explored.

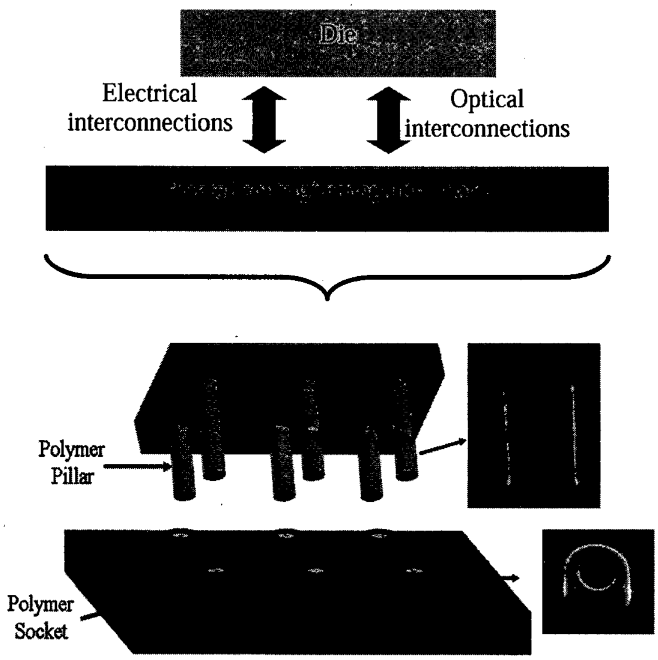

Figure 1: Schematic illustration of the basic principles of SoPP chip I/O interconnection technology.

II. Implementation of Electrical and Optical I/O Interconnections

A schematic illustration of SoPP chip I/O interconnections is shown in Figure 2. The principal idea is to batch fabricate polymer pillars, or polymer pins, on dice at the wafer level and to fabricate polymer sockets on the board. The sockets are designed such that they hold the pillars and assist during assembly by passively aligning the chip to the board, which is essential for microphotonics technology. The polymer pillars act as surface-normal waveguides and enable the optical waveguide interconnection of two planar surfaces, such as a die and a board [5-6]. Metallization of the polymer pillars yields electrical interconnections. Finally, the use of a single polymer pillar for simultaneous electrical and optical I/O interconnections has been described previously [5].

Polymer pillars with various aspect ratios, pitches, and cross-sectional geometries have been successfully fabricated (Figure 3). Figure 4 illustrates two scanning electron microscope (SEM) photomicrographs of polymer pillars with very differing geometrical dimensions: the first photomicrograph is of polymer pillars that are ~60 µm in diameter, ~300 µm tall, and fabricated on a 325 µm pitch, while the second is that of pillars that are ~5 µm in diameter, ~13 µm tall, and fabricated on a 12 µm pitch. The polymer pillars are fabricated using the photodefinable polymer Avatrel 2000P (Promerus, LLC). The photomicrographs illustrate to the reader that the photodefinable process and polymer used to fabricate the pillars easily accommodates the fabrication of a very wide range of dimensions.

The photomicrographs shown in Figure 4 illustrate polymer pillars that have a flat tip topology. The optical transmission characteristics of such pillar waveguides have been tested. Results indicate that the polymer pillars act as precision many-moded waveguides [6]. In order to couple light into and out of a polymer pillar using a planar waveguide, a mirror or a waveguide grating coupler is needed at such interfaces. These optical elements may be fabricated either on the waveguide [7] or directly on the polymer pillar. For example, Figure 5 is an SEM photomicrograph of a polymer pillar with a partially slanted surface. In order to reflect a light beam from such a surface, the slant is either metallized or used as a total internal reflection mirror.

The sidewall surface topology of the pillars has also been successfully patterned. For example, low aspect ratio polymer pillars with gear teeth sidewall pattern have been fabricated, as shown in Figure 6. The ability to control the sidewall topology is beneficial for the electrical pillars as well as other applications. The adhesion between the metal and the polymer can be increased.

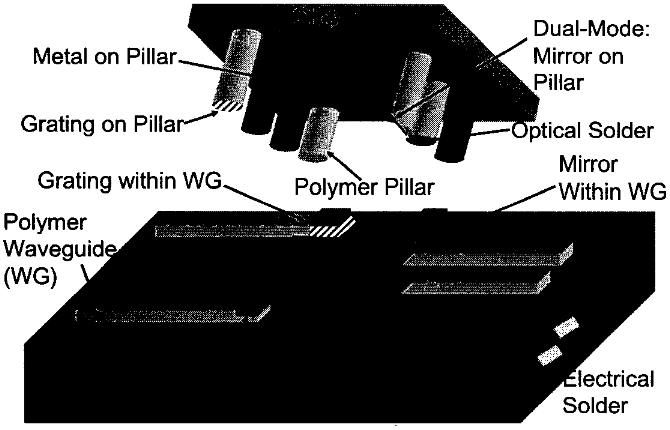

Figure 2: Schematic of electrical and optical chip I/O interconnections using SoPP [5].

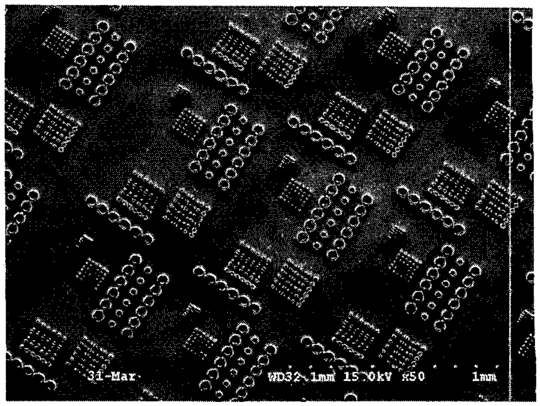

Figure 3: SEM photomicrograph of polymer pillars and sockets with various cross-sectional geometries, aspect ratios, and pitches.

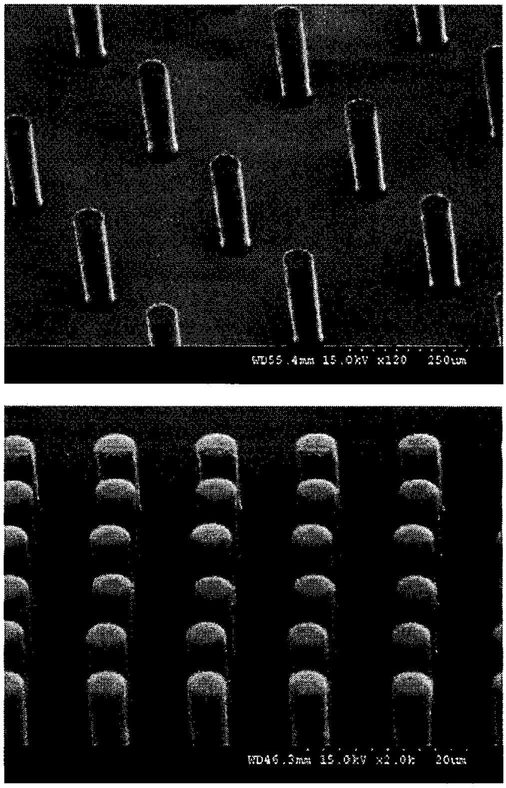

Figure 4: SEM photomicrographs of polymer pillars with a wide range of dimensions.

Figure 7 is a schematic of one of the fabrication processes that is used to fabricate optical and electrical I/O interconnections using polymer pillars. The process begins by spin coating the polymer Avatrel 2000P on the wafer (Figure 7a-b). The regions where the optical pillars are desired, the polymer film is molded with the optical feature of interest (mirror, surface relief grating, or lens, for example), as illustrated in Figure 7c. If the coupling element is fabricated on the planar waveguide, the polymer film can be left flat.

Next, the polymer is photoimaged and spray developed (following a hard bake) to yield the polymer pillars (with desired tip topology). The wafer is next placed in a furnace for a cure (Figure 7d). Finally, a metal film is deposited on the pillars providing electrical interconnection.

A detailed schematic of the electrical I/Os is shown in Figure 8. Both the optical and the electrical I/O interconnections are mechanically compliant to minimize stresses imparted on the chip's low-k interlayer dielectric and to maintain optical alignment between optical devices on the chip and the board.

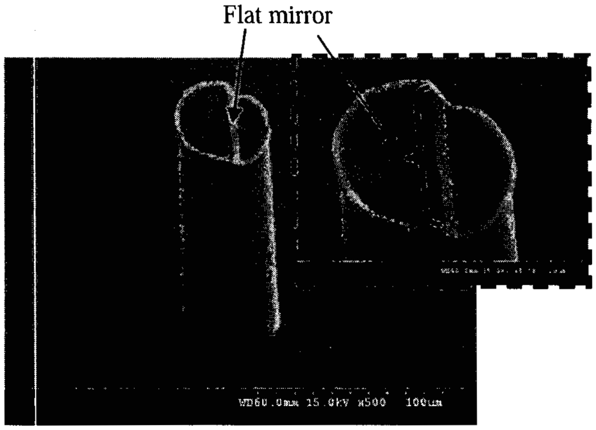

Figure 5: SEM photomicrograph of ~100 µm tall and 55 µm wide polymer pillar with a 6 µm tall flat mirror on its tip.

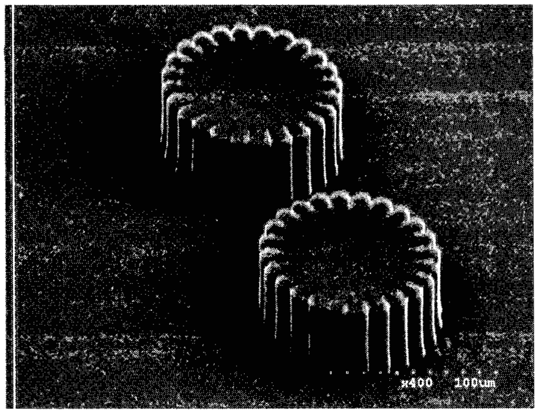

Figure 6: Pair of low aspect ratio polymer pillars that were photoimaged such that they attained the very distinctive sidewall profile shown. The gear teeth pattern was part of the cross-sectional pattern of the pillars on the mask.

Polymer pillars that are fully metallized have been attached to a board using solder. In order to eliminate the need for alignment between the die and the board, and simplify the experiment, the pillars were bonded to a blanket thin film of solder. The results of this experiment are illustrated in Figure 9 and Figure 10. The complement of this experiment for the optical I/Os is illustrated in Figure 11. In this experiment, the 'solder' used was prepared by spin coating a thin layer of the polymer Avatrel 2000P on a second substrate (without a soft bake) followed by the flip-chip attachment of a die containing the polymer pillars. The assembled system was next placed on a hotplate for a soft bake and finally placed in a furnace to cure the polymer film and anchor the pillars in the film. The assembled chips were probed to confirm the mechanical interconnection. The above discussion assumes that separate materials (solder and an optical adhesive) are needed to mechanically hold the electrical and optical pillars. However, it is possible to fabricate a thin and narrow metallic ring around the tip of the optical polymer pillars such that electrical solder can be used to hold the optical pillars as well. This is significant because it simplifies the processing required on the board. Such pillars are shown in Figure 12. A dielectric may separate the metal ring and the polymer. Figure 13 is a schematic illustrating how these pillars would be interconnected. Optical characterization of such interconnections is being pursued.

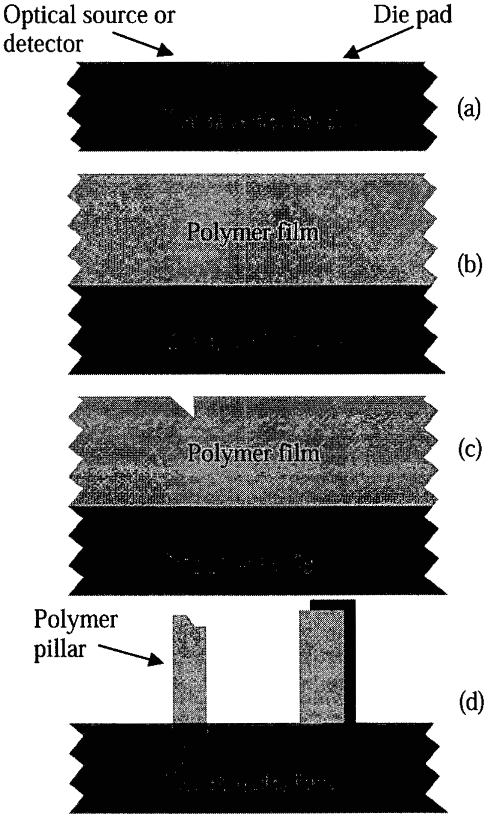

Figure 7: The fabrication sequence of the polymer pillars: (a) Wafer, (b) Avatrel 2000P is spin coated to the desired thickness and placed on a hotplate for a soft bake. The polymer film is next (c) plastically deformed (imprinted) and UV irradiated through a mask containing the cross-sectional geometry of the polymer pillars. The wafer is next placed in an oven for a hard bake. Finally, (d) the polymer film is spray-developed to yield the final polymer pillars, and the wafer is placed in a furnace for a cure (<200 C). Metal is next deposited on the pillars providing electrical interconnection.

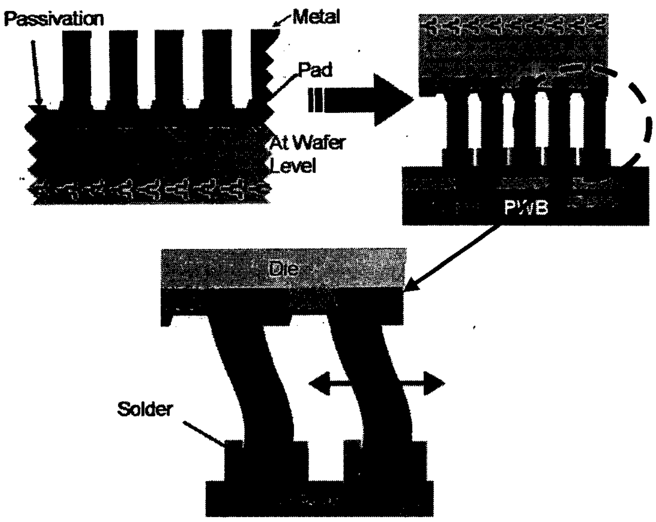

Figure 8: Detailed schematic of SoPP electrical chip I/O interconnections. The lower illustration describes the compliant nature of the interconnections during thermal cycling.

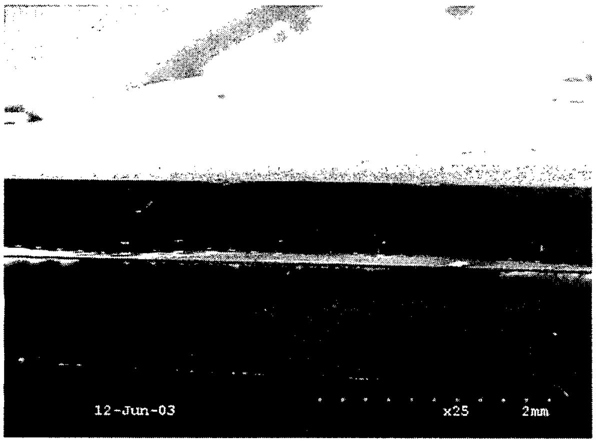

Figure 9: SEM photomicrograph of a Si die with fully metallized polymer pillars (~100 µm tall and 55 µm in diameter) bonded to a substrate containing a thin layer of solder.

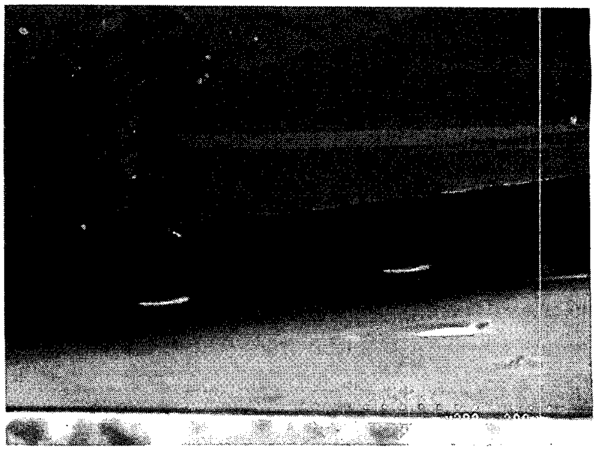

Figure 10: Higher magnification photomicrograph of the assembled chip shown in Figure 9.

Figure 11: Photomicrograph of a Si die with optical polymer pillars (~100 µm tall and 55 µm in diameter) bonded to a substrate containing a polymer film.

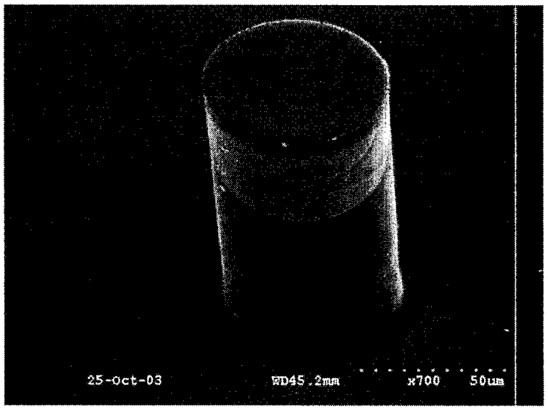

Figure 12: Photomicrograph of a polymer pillar with a metallic ring around its tip. Such a structure permits the use of electrical solder to mechanically hold the optical I/O interconnections.

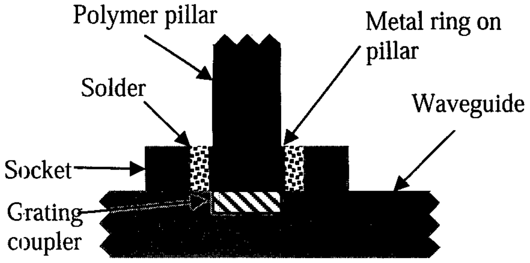

Figure 13: Illustration of an optical pillar with a metallic ring around its tip bonded to a planar waveguide using solder.

III. Surface-Normal Hollow I/O Interconnect Structures

I/O interconnections that resemble a micropipe can be integrated with the polymer pillars. The shell of the micropipe may either be polymeric or metallic. The latter is shown in Figure 14 and Figure 15. Such structures may find application as optical, electrical, and thermal I/O interconnections. When these micropipes are fabricated between two planar microchannels on the chip and the board, fluid may be pumped through the two channels, as schematically illustrated in Figure 16. These micropipes can be used for heat removal (spot cooling) as well as potentially for biological applications. Heat removal is a major concern for future chips, and thus, these micropipes can be used in conjunction with die back side heat removal strategy to permit heat removal from both surfaces of the chip. In addition, such micropipes may potentially be significant during wafer-level testing and burn-in, where heat removal is a bottleneck. In order to facilitate microfluidic flow, a slanted surface may be fabricated below and above the micropipes to mitigate microfluidic flow at right-angle bends. This idea parallels the requirements of the optical I/O interconnections. Finally, it is clear that the micropipes must be sealed once bonded to the board to prevent leakage.

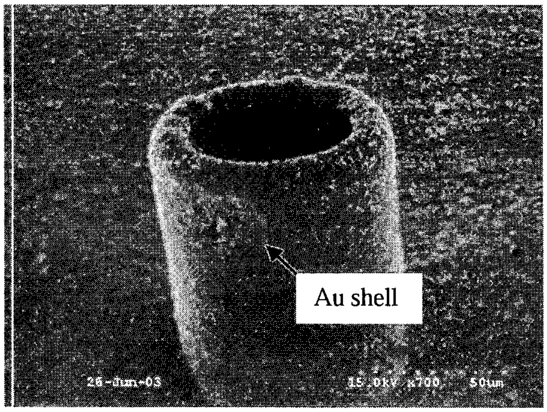

Figure 14: SEM photomicrograph of a hollow metallic cylinder, or micropipe. The metal is approximately 10 µm thick electroplated Au. The height of the micropipe is approximately 100 µm, and its inner diameter is 55 µm. Width and height can span a wide range of dimensions.

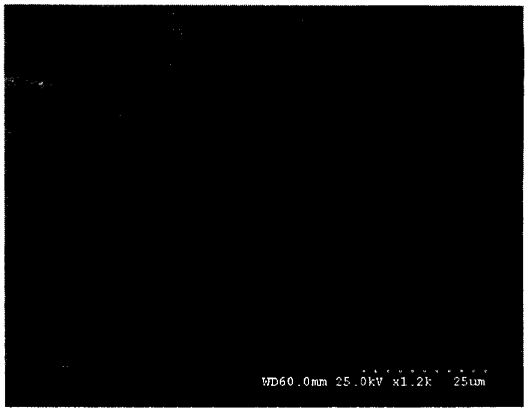

Figure 15: Higher magnification SEM photomicrograph of a metallic micropipe.

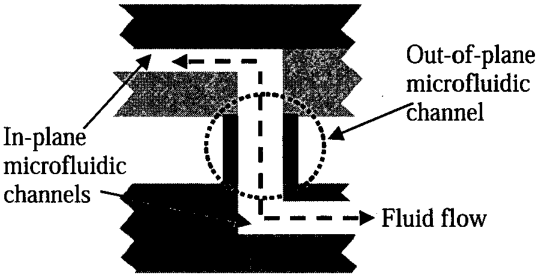

Figure 16: A schematic illustrating how an out-of-plane microfluidic channel (or micropipe) can be used to connect two planar microfluidic channels on separate planes.

Such micropipes can be fabricated through many methods. One promising method for integration with optical and electrical I/O interconnections based on polymer pillars is to metallize the sidewalls of the polymer pillars followed by the selective etching of the polymer pillars. The micropipes shown in the figures were fabricated by thermally (>350 C) decomposing the polymer pillar.

IV. Measurements

The lateral compliance of the pillars has been measured. Measurements indicate that the polymer pillars exhibit high compliance and elastically deform [5]. Optical measurements confirm the high quality of the pillars as waveguides [6] and their functionality with grating couplers [5].

V. Conclusion

Integrated wafer-level, compliant electrical and optical chip I/O interconnections for gigascale integration (GSI) have been described. The fabrication of a wide range of polymer pillar dimensions and the fabrication of pillars with mirrors on their tips have been demonstrated. Moreover, surface-normal hollow metallic micropipes for potential optical, electrical, and thermal chip I/O interconnection have been fabricated. When these results are coupled with previously reported mechanical and optical measurements, Sea of Polymer Pillars (SoPP) represents a promising I/O interconnection technology potentially capable of meeting the I/O interconnect performance demands of a GSI chip.

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