

Impact of Interconnect Parameter Variations on Wire-tree Delay

Azeez J Bhavnagarwala, Ashok Kapoor[‡] and James D Meindl

Microelectronics Research Cntr. and the School of Elec. and Comp. Eng., Georgia Inst. of Tech., Atlanta GA 30332

[‡] LSI Logic Corporation, Milpitas, CA 95035

Abstract[†]

New distributed wire-tree and stochastic delay distribution models are proposed to assess the impact of interconnect process parameter variations on fluctuations in interconnect delay. Closed-form expressions for distributed wire-tree delay reported are accurate to within 5% of HSPICE simulations. These are used in tandem with stochastic models for delay distributions to estimate deviations in interconnect delay. Deviations in interconnect delay are reported to increase as the square of interconnect length and inversely with interconnect width.

Introduction

With scaling of minimum feature size, although interconnect delay increases can be limited to 30% per generation by reverse scaling of metal and insulator dimensions [1], interconnect delay and variations in interconnect delay increasingly limit chip speed and delay variation margins [2,3,4]. While interconnect delay imposes constraints on maximum interconnect length, variations in interconnect delay that increase sharply at smaller line widths [5] also impose constraints on minimum interconnect width along RC limited paths. Accurately estimating interconnect delays and variations in interconnect delay along arbitrary wire tree networks, due to interconnect parameter variations is thus essential to optimizing wire geometries and repeater circuitry along RC limited paths. First-order path-tracing RC tree methods [6] based on the Elmore delay model [7] lack in accuracy in estimating delays across distributed wire-tree networks. The Qth order and more accurate Asymptotic Waveform Evaluation (AWE) extensions [8,9] require formulating and solving nodal matrices where computational effort and memory requirements increase with chip and wire-tree complexity even though these techniques are more efficient than real-time HSPICE simulations. Recent attempts to estimate the impact of interconnect process variations on clock skew and interconnect delay [3] employ Monte Carlo simulations using a finite-difference solver. Any of the above methodologies to estimate wire-tree delay and/or variations in wire-tree delay would incur increasing costs in accuracy or in computational time and effort with increase in chip and interconnect complexity. Sakurai's accurate (<3% error) closed-form analytical models for distributed interconnect delay [10] that apply only to the case of step excitations at the input of a buffer driving a 2-pin net are extended in this work to the more commonly encountered and complex cases

of branched network topologies and linear ramp/exponentially saturating input waveforms. These new models permit fast, accurate and early estimates of delay and stochastic variations in delay along arbitrary wire-tree networks with immediate applications to the design and optimization of clock signal distribution nets for minimum skew.

Interconnect response to non-zero rise time

The frequency-domain interconnect response to a step input function [10] given by (1a) in the Appendix, may be analytically extended to the case of a ramp input (1b), (2) by making a Taylor expansion (3a) of the first term on the RHS of (2). This expansion translates the time-domain interconnect response to a step *by exactly half the ramp time* using the Laplace operator in (4b). Comparison of Sakurai's interconnect response model (5a) shifted by half the ramp time (5b) with HSPICE simulations are shown to be in excellent agreement in Figs. 1 and 2 for different cases of ramp time and wire geometry. The *50%-50% propagation delay* between buffer input and interconnect response at the far-end of the distributed line is thus *independent of rise time at input*. For the case of an exponentially saturating waveform driving the input of a buffer, since short-channel devices behave as a constant current source for most of the transition at the output, for reasonably fast input transitions, the 20-80% rise time of the exponentially saturating input waveform can be replaced with a linear ramp of identical 20-80% transition time centered around the 50% points [11]. For the case of an interconnect driving another interconnect (as encountered at a branch or between levels in a multilevel interconnect architecture), the frequency-domain response of the interconnect downstream is modeled by (7b), (8b) where a Taylor expansion of the first term in the RHS of (7b) yields the result that the step-input response is shifted *exactly by the time constant of the exciting waveform* (9). Comparison of (9) with HSPICE in Fig. 3 demonstrates excellent agreement of this model as well. Expression for propagation delay (10) shows dependencies on the time constant of the exponentially saturating exciting waveform unlike the case of a linear ramp input.

Response at intermediate nodes in a chain of nets

Exact time-domain solutions for voltage and current waveforms at any arbitrary intermediate position along a uniform distributed 2-pin wire are given by (11) from [10]. This exact solution assumes C_T and R_T given by (6) to be zero. Using the approximations in (12b) and (12c), addition of driver resistance and load capacitance is included into (11) to yield (12a) in the same way that (5a) was derived in [10]. The higher order terms ($k>1$) in the multi exponential

[†] This work was supported by LSI Logic Corporation, the Defense Advanced Research Project Agency (Contract: F3361595C1623) and the Semiconductor Research Corporation (SJ-374-002)

expansion of the time domain solution in (12a) make insignificant contributions. The equivalent of position x in (11) and (12a) along the 2-pin wire is modeled as the ratio of resistance seen upstream (for the chain of nets in Fig 4a) to total path resistance (13b). Excellent agreement is observed between (13) and HSPICE for point 'A1' in the schematic of the wire chain shown in Fig 4.

Propagation delay across arbitrary wire tree networks

The response at the end node (C) of the longest path in an arbitrary tree network (Fig. 5) may be modeled accurately by replacing the network between the driver and the node of interest with a 'black box' (dotted lines in Fig 5). The interconnect response given by (14) describes the waveform at the end of the longest path for a given network. The total resistance seen between terminals A and C of the 'black box' given by (15b) and the total capacitance (15c) seen between the same terminals replace the distributed wire resistance and capacitance - R and C used in (5). The accuracy of (14), applicable only to the longest path, deteriorates if the tree network has *many short* branches to one of which the above model is applied. This is so because the 'effective capacitance' seen at branch points with high fan-outs would be lower than predicted by (15c). To remedy the inaccuracies due to the shielding of wire capacitance by its resistance, resulting from applying (14) to nodes closer to the source (say, X, D or B in Fig 5), we apply the model for intermediate nodes (13a) to node X in Fig 5 and calculate the propagation delay from node X to node D in the same example using the model for exponentially saturating inputs given by (10). The propagation delay to nodes closer to the source: D, B and X in the example in Fig. 5 can thus be calculated very accurately using (16) and (17). Table I compares the above model with calculations using Elmore's model and HSPICE for the same circuit in Fig 5. Fig. 6 compares the waveform seen at node C with HSPICE simulations.

Stochastic variations in wire-tree delay

Variations in interconnect delay (18a) are mostly caused by variations in wire width/spacing, wire height and IMD thickness [2]. Variations in lithographic linewidth, RIE bias and dielectric CMP cause the above variations [4]. Each of the above three sources of variations are mutually independent and are gaussian (18b) in their distribution [3]. The cumulative impact of these variations to interconnect delay fluctuations may be estimated by convolving the independent distributions (18c) of interconnect delay due to variations in each of the above parameters to obtain a joint PDF of interconnect delay (18d). Fig 7 plots the individual distributions of interconnect delay per mm^2 of interconnect length and also the joint PDF. Deviations in the joint PDF of interconnect delay increase as the square of interconnect length because variations in wire resistance (or capacitance) per unit length due to the above three factors, multiplies with the square of interconnect length. The joint PDF (18d) yields more realistic estimates on $\pm 3\sigma$ variations corresponding to

extremes in interconnect delay variation than do the best case/worst case interconnect parameter decks [3]. Interconnect delay dependence on interconnect width is shown in Fig. 8. Interconnect delay variations increase sharply at smaller line widths corresponding to cases when wire packing densities are high and chip size is wire limited, because variations in wire width/spacing become larger fractions of wire width, at smaller widths. For RC limited paths, variations in interconnect delay contribute larger fractions to variations in total path delay with scaling due to shielding by interconnect resistance. Shielding shrinks the delay [2] and delay variability contributions by device parameters, making interconnect process parameter variations increasingly significant in any analysis of delay fluctuations.

Conclusions and Summary

New, accurate, simple and readily usable models are reported to predict variations in interconnect delay across arbitrary, distributed wire-tree networks. The models for interconnect delay are shown to be accurate to within 5% of HSPICE simulations and require much less computational effort than the commonly used AWE numerical techniques. Variations in interconnect delay are shown to increase quadratically with interconnect length, inversely with reductions in wire widths, and are projected to increasingly limit clock skew and wiring pitch.

References:

- [1] M. T. Bohr, "Interconnect scaling - the real limiter to high performance ULSI," *Solid State Tech.* v 39 n 9 pp. 105-108, Sep 1996.
- [2] K. Bernstein et al, "*High Speed CMOS Design Styles*", Norwood MA, Kluwer Academic, 1998, chapter 4.
- [3] O.S. Nakagawa et al, "Circuit Impact and Skew-Corner Analysis of Stochastic Process Variation in Global Interconnect," *1999 IITC Tech. Dig.*, pp. 230-232 Jun 1999.
- [4] V. Mehrotra et al, "Modeling the Effects of Manufacturing Variation on High-Speed Microprocessor Interconnect Performance," *1998 Tech. Digest, IEDM*, pp. 767-770
- [5] A. K. Stamper et al, "Sub-0.25-micron interconnection scaling: Damascene copper versus subtractive aluminum," *IEEE SEMI Adv. Semi. Mfg. Conf Workshop 1998* IEEE Piscataway NJ USA pp. 337-346.
- [6] P. Penfield et al, "Signal Delay in RC Tree Networks," *Proc. of the 19th DAC, 1981*, June 1981.
- [7] W. C. Elmore, "The transient response of damped linear networks with particular regard to wideband amplifiers," *J. App. Phys.*, Vol. 19, pp. 55-63, Jan 1948.
- [8] L. Pillage et al, "Asymptotic Waveform Evaluation for Timing Analysis," *IEEE Trans. On CAD*, pp. 352-366, April 1990
- [9] C. Ratzlaff et al, "RICE: Rapid Interconnect Circuit Evaluation Using AWE," *IEEE Trans. On CAD*, Vol. 13, No. 6, pp. 763-776, Jun. 1994.
- [10] T Sakurai, 'Approximation of Wiring Delay in MOSFET LSI', *IEEE Journal of Solid State Circuits*, Vol. SC-18, No. 4, pp. 418-426, Aug 1983.
- [11] T. Sakurai et al, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE J. of Solid State Circuits*, Vol. 25, No. 2, pp. 584-594, Apr. 1990.

Appendix: Interconnect response models:

(A) Step [8] and ramp input response of 2-pin net in s-domain: (Figs 1 & 2)

$$(1a) V_{step}(s) = V_{in}(s)H(s) = \frac{1}{s}H(s); (1b) V_{ramp}(s) = V_{in}(s)H(s) = \frac{(1 - e^{-st_{ramp}})}{s^2 t_{ramp}} H(s); (2) V_{ramp}(s) = \frac{(1 - e^{-st_{ramp}})}{st_{ramp}} V_{step}(s)$$

Approximation: (3a) $\frac{1 - e^{-x}}{x} \cong e^{-\frac{x}{2}}$; (3b) $V_{ramp}(s) \cong e^{-\frac{st_{ramp}}{2}} V_{step}(s)$

Laplace Transform pairs: (4a) $e(t) \leftrightarrow E(s)$; (4b) $e(t - t_o) \leftrightarrow e^{-st_o} E(s)$

$$(5a)[8] \frac{V_{step}(t)}{V_{dd}} = 1 - e^{-\left(\frac{\frac{t}{RC} - 0.1}{R_T C_T + R_T + C_T + 0.4}\right)}; (5b) \frac{V_{ramp}(t)}{V_{dd}} = 1 - e^{-\left(\frac{\frac{t - \frac{t_{ramp}}{2} - 0.1}{RC}}{R_T C_T + R_T + C_T + 0.4}\right)}$$

(6a) $R_T = \frac{R_{tr}}{R}$; (6b) $C_T = \frac{C_L}{C}$; (6c) $R_{tr} = \frac{V_{dd}}{I_{dsat}[V_{dd}, V_{dd}, 0]}$

(C) Interconnect response at intermediate nodes along chain of distinguishable nets (Fig 4)

$$(11) [8] \frac{v(x, t)}{V_{dd}} = 1 + \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{(-1)^k}{k - \frac{1}{2}} \cos\left[\left(k - \frac{1}{2}\right)\pi\left(1 - \frac{x}{L}\right)\right] e^{-\left[\left(k - \frac{1}{2}\right)^2 \pi^2\right]\left(\frac{t}{RC}\right)}$$

For loaded nets driven by non-zero driver resistance :

$$(12a) \frac{v(x, t)}{V_{dd}} = 1 + \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{(-1)^k}{k - \frac{1}{2}} \cos\left[\left(k - \frac{1}{2}\right)\pi\left(1 - \frac{x}{L}\right)\right] e^{-\left[\frac{1}{\left(k - \frac{1}{2}\right)^2 \pi^2 + R_T C_T + R_T + C_T}\right]\left(\frac{t}{RC}\right)}$$

; for k=1 only, (12b) $\frac{1}{\left(k - \frac{1}{2}\right)^2 \pi^2} \cong 0.4$ and (12c) $\frac{2}{\pi} \sum_{k=1}^{\infty} \frac{(-1)^k}{k - \frac{1}{2}} \cong -e^{0.4}$

For node A1 in Fig 4

$$(13a) \frac{V_{A1}(t)}{V_{dd}} = 1 - \cos\left(\frac{\pi}{2}\left(1 - \frac{R_{upstream}}{\sum R_{path}}\right)\right) \times \exp\left(-\frac{\frac{t - \frac{t_{ramp}}{2}}{\sum R_{path} \sum C_{path}} - 0.1}{R_T C_T + R_T + C_T + 0.4}\right); (13b) \sum R_{path} = R_{int1} + R_{int2} + R_{int3}; (13c) \sum C_{path} = C_{int1} + C_{int2} + C_{int3}$$

(13d) $R_{upstream} = R_{int1}$

(D) Wire-tree networks: (Fig 5), At node C in the example of Fig. 5:

$$(14a) \frac{V_{ramp}(t)}{V_{dd} \text{ nodeC}} = 1 - \exp\left(-\frac{\frac{t - \frac{t_{ramp}}{2}}{\left(\sum R_{path}\right)\left(\sum C_{path}\right)} - 0.1}{R_T C_T + R_T + C_T + 0.4}\right)$$

At node X in the example in Fig. 5:

$$(16) \frac{V_{ramp}(t)}{V_{dd} \text{ nodeX}} = 1 - \cos\left(\frac{\pi}{2}\left(1 - \frac{R_{upstream}}{\sum R_{path}}\right)\right) \times \exp\left(-\frac{\frac{t - \frac{t_{ramp}}{2}}{\left(\sum R_{path}\right)\left(\sum C_{path}\right)} - 0.1}{R_T C_T + R_T + C_T + 0.4}\right)$$

(16b) $R_{upstream} = R_{int1}$

$$(17b) t_{pd} = \sum R_{path} \times \sum C_{path} \left[(R_T C_T + R_T + C_T + 0.4) \ln\left[2 \cos\left(\frac{\pi}{2}\left(1 - \frac{R_{int1}}{\sum R_{path}}\right)\right)\right] + 0.1 \right] + 0.3\tau_x + R_{int3} C_{int3} \left[\left(\frac{C_3}{C_{int3}} + 0.4\right) \ln 2 + 0.1 \right]$$

(B) Exponentially saturating input response of 2-pin net driven by interconnect: (Fig. 3)

$$(7a) V_{in}(t) = V_{dd} \left(1 - e^{-\frac{t}{\tau}}\right)$$

$$(7b) V_{exp}(s) = V_{in}(s)H(s) = \frac{1}{s(\tau + 1)} H(s) = \frac{1}{(\tau + 1)} V_{step}(s)$$

Approximation: (8a) $\frac{1}{\tau + 1} \cong e^{-\tau}$ (8b) $V_{exp}(s) = e^{-\tau} V_{step}(s)$

Time-domain response: (9) $\frac{V_{exp}(t)}{V_{dd}} = 1 - \exp\left(-\frac{t - \tau - 0.1}{RC} - \frac{t}{C_T + 0.4}\right)$

Propagation delay:

$$(10) t_{pd_A \rightarrow B} = 0.3\tau + RC[(C_T + 0.4) \ln 2 + 0.1]$$

For node C (longest path) in Fig 5

$$(14b) R_T = \frac{R_{tr}}{\sum R_{path}}; (14c) C_T = \frac{C_L}{\sum C_{path}}$$

$$(15a) t_{pd} = \left(\sum R_{path}\right) \left(\sum C_{path}\right) (R_T C_T + R_T + C_T + 0.4) \ln(2) + 0.1$$

$$(15b) \left(\sum R_{path}\right) \text{ (for node C in Fig 5) } = R_{int1} + R_{int2} + R_{int5};$$

$$(15c) \left(\sum C_{path}\right) \text{ (for node C in Fig 5) } = C_{int1} + C_1 + C_{int2} + C_{int3} + C_3 + C_{int4} + C_4 + C_{int5}$$

Propagation delay to node D in Fig 5:

$$(17a) t_{pd_A \rightarrow D} = t_{pd_A \rightarrow X} + t_{pd_X \rightarrow D}$$

$$(18a) \Delta t_{pd}^{wire-tree} = \sum_{all_nets} \Delta t_{pd}^{W/S} + \Delta t_{pd}^H + \Delta t_{pd}^{IMD} \quad (18b) f(x_i) \equiv \frac{1}{\sqrt{2\pi\sigma_{x_i}^2}} e^{-\frac{(x_i-x_{i0})^2}{2\sigma_{x_i}^2}} \quad (18c) f(t_{pd}^i) = \frac{f(x_i)}{\frac{\partial(t_{pd}^{wire-tree})}{\partial x_i}}$$

index $i=1 \rightarrow N$ corresponds to each independent interconnect process parameter in a multi-level wire-tree network

$$(18d) f(t_{pd}^{wire-tree}) = f(t_{pd}^1) * f(t_{pd}^2) * \dots * f(t_{pd}^i) * \dots * f(t_{pd}^N)$$

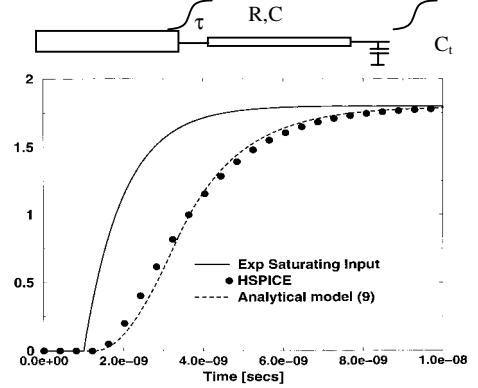
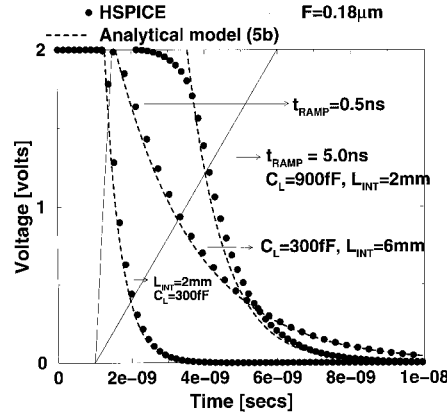
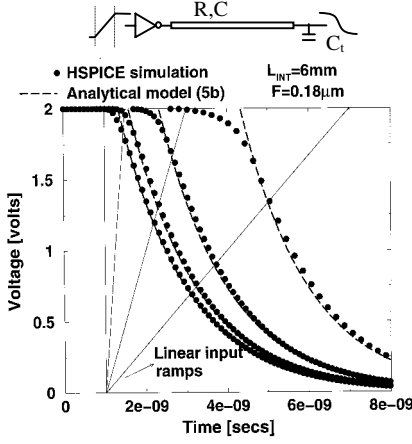


Figure 3: Interconnect response to exponentially saturating inputs

Figures 1 & 2: Comparison of 2-pin interconnect response model (5b) with HSPICE for different wire geometries and ramp times

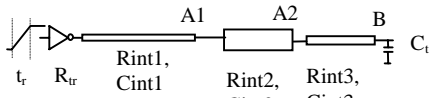


Figure 4a,b (at left): Intermediate nodes along a chain of loaded and distinguishable nets

node	HSPICE	Propagation delay (ns)			
		New model		Elmore model	
			Error %		Error %
B	19.05	18.4	3.41	27.2	42.8
C	22.35	22.2	0.70	28.9	29.3
D	14.47	13.7	4.86	21.9	51.3

Table 1: Comparison of HSPICE with new model and the Elmore delay model for the circuit in Fig. 5.

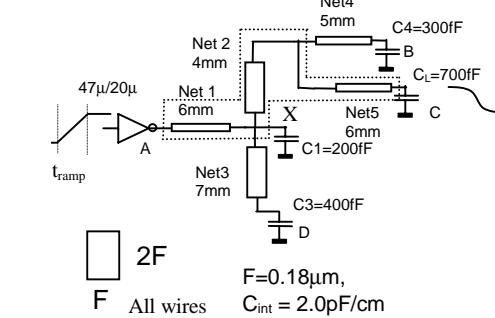
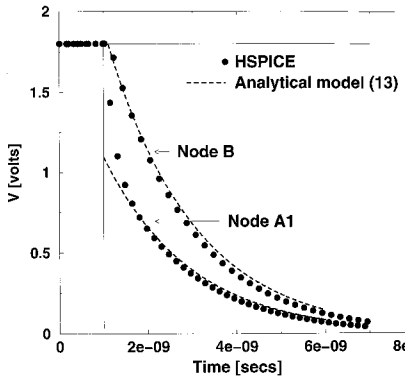


Figure 5: Arbitrary wire-tree network example

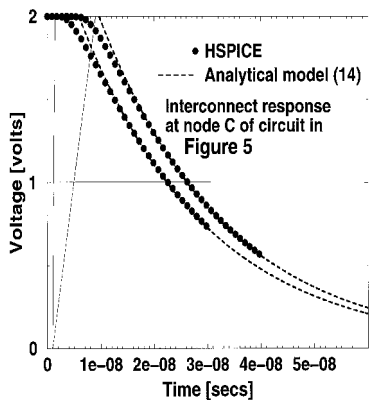


Figure 6: Comparison of (15a) with HSPICE at node C

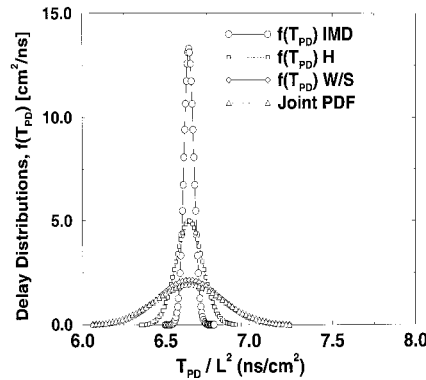


Figure 7: Joint PDF in interconnect delay/ L^2 due to interconnect parameter variations (18d). Interconnect delay is most sensitive to variations in line width and spacing and least sensitive to variations in IMD

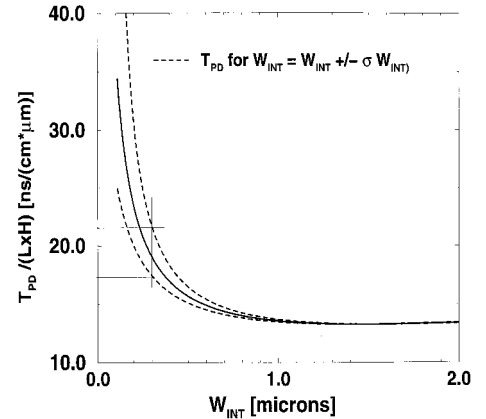


Figure 8: Increase in interconnect delay variability with reductions in interconnect width and spacing. For a 0.3um wide M3 net in a 0.18um process, interconnect delay varies in excess of 25% due to standard deviations in wire width alone.