The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability

Azeez J. Bhavnagarwala, *Student Member, IEEE*, Xinghai Tang, *Member, IEEE*, and James D. Meindl, *Life Fellow, IEEE*

***Abstract*—Reductions in CMOS SRAM cell static noise margin (SNM) due to intrinsic threshold voltage fluctuations in uniformly doped minimum-geometry cell MOSFETs are investigated for the first time using compact physical and stochastic models. Six sigma deviations in SNM due to intrinsic fluctuations alone are projected to exceed the nominal SNM for sub-100-nm CMOS technology generations. These large deviations pose severe barriers to scaling of supply voltage, channel length, and transistor count for conventional 6T SRAM-dominated CMOS ASICs and microprocessors.**

***Index Terms*—MOSFET fluctuations, SRAM scaling, SRAM stability projections, static noise margin.**

I. Introduction

With scaling of MOSFET dimensions, microscopic variations in number and location of dopant atoms in the channel region of the device induce increasingly limiting electrical deviations in device characteristics [1]–[3]. These atomic-level intrinsic fluctuations cannot be eliminated by external control of the manufacturing process and are most pronounced in minimum-geometry transistors commonly used in area-constrained circuits such as SRAM cells [4]. Furthermore, intrinsic fluctuations are independent of transistor location on a chip. The threshold mismatch between neighboring cell transistors due to intrinsic fluctuations typically contributes to larger reductions in static noise margin (SNM) than the threshold voltage mismatch due to macroscopic manufacturing-related variations in scaled CMOS SRAM cells [4]. Previously developed analytical SNM models for 6T CMOS SRAM cells [5] would be unsuitable for assessing the impact of intrinsic fluctuations on cell stability since these models assume long-channel square-law device behavior. The SNM model in [5] also assumes identical device threshold voltages across all cell transistors, making it unsuitable for predicting the effects of threshold voltage mismatch between adjacent transistors within a cell on SNM.

In Section II, an analytical model for the SNM of a 6T CMOS SRAM cell is derived and verified with HSPICE. This SNM model, derived using the physical *Transregional* MOSFET drain current model [6], [7] identifies the individual contributions of each cell transistor to the cell SNM, permitting an assessment of the cumulative impact of simultaneous fluctuations in all cell transistors on its stability. Its physical rather than empirical origin enables greater insight into MOSFET parameters that are most critical to cell stability. This model considers 1) vertical and lateral high field effects on carrier mobility; 2) short-channel threshold voltage roll-off [8]; and 3) temperature dependencies of carrier mobility, threshold voltage, and carrier saturation velocity. In Section III, a methodology to calculate the joint probability density function (pdf) of cell SNM is described, given the pdf of threshold voltage variations of each minimum geometry cell transistor due to random placement of dopant atoms. This methodology permits a stochastic assessment of reductions in cell SNM due to the independent intrinsic fluctuations in each of the cell transistors. Section IV applies this methodology across the 1997 NTRS technology nodes [9] to project standard deviations in SNM due to intrinsic fluctuations.

II. A 6T CMOS SRAM SNM Model

The SNM of a CMOS SRAM cell is defined [10] as the minimum dc noise voltage necessary to flip the state of a cell. The SRAM cell circuit schematic and static transfer characteristics during standby mode and during a read access are shown in Fig. 1. Graphically, as seen in Fig. 2, the SNM equals the noise voltage necessary at each of the cell storage nodes to shift the static characteristics of the two cell inverters vertically or horizontally along the side of the maximum nested square so that they intersect at only one point [10]. The cell is most vulnerable to noise during a read access since the "0" storage node rises to a voltage higher than ground due to a voltage division along the access and inverter pull-down NFET devices between the precharged bitline (BL) and the ground terminal of the cell. The ratio of the widths of the pull-down transistor to the access transistor, commonly referred to as the *cell ratio* or *beta ratio*, determines how high the "0" storage node rises during a read access. Smaller cell ratios translate into a bigger voltage drop across the pull-down transistor, requiring a smaller noise voltage at the "0" node to trip the cell. During a read operation, the conducting access transistors lie in parallel to the pull-up PFETs, lowering the gain of the static transfer characteristic [5] and further decreasing cell immunity to noise. The side of the maximum square nested between the inverter characteristics *during a read access* thus equals the SNM of the cell.

Using the Transregional MOSFET drain current model [6], [7] analytical expressions for the static transfer characteristics,

Manuscript received January 11, 2000; revised December 18, 2000. This work was supported by the Semiconductor Research Corporation under Contract SJ-374 and by the Defense Advanced Research Projects Agency under Contract F3361595C1623.

The authors are with Microelectronics Research Center and School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0269 USA (e-mail: azeez@ee.gatech.edu; james.meindl@ee.gatech.edu).

Publisher Item Identifier S 0018-9200(01)02410-6.

0018–9200/01$10.00 © 2001 IEEE

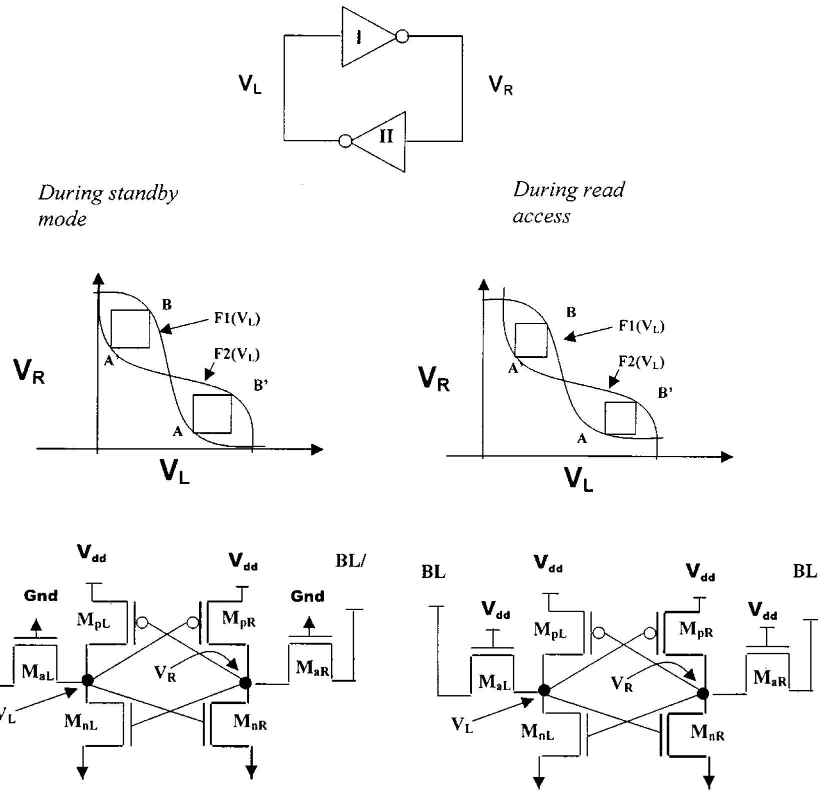

Fig. 1. Circuit schematics of a CMOS SRAM cell during standby mode and during read access. The cell is most vulnerable to noise during a read access.

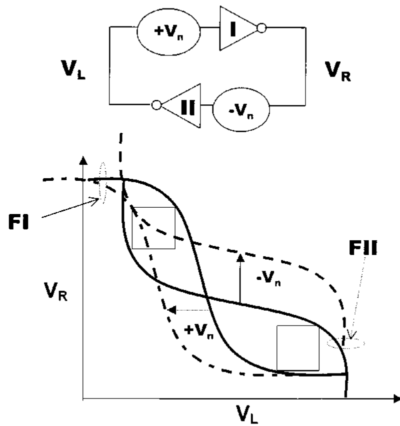

Fig. 2. The static noise margin is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell. Graphically, this may be seen as moving the static characteristics vertically or horizontally along the side of the maximum nested square until the curves intersect at only one point.

$F1$ and $F2$ of the two cell inverters (Fig. 1) in the neighborhood of the corners **B**, **A′** and **B′**, **A** of the maximum squares can be derived by solving Kirchoff's current law at the cell storage nodes V_R and V_L, respectively:

$$I_{nR} = I_{pR} + I_{aR} \tag{1a}$$

$$I_{nL} = I_{pL} + I_{aL}. \tag{1b}$$

The subscript "R" is indicative of the right-hand side of the cell and the subscript "L" indicative of the left-hand side. Subscript "p" indicates the pull-up PFET device and subscripts "n" and "a" correspond to the inverter pull-down NFET and the access NFET, respectively. This notation will be used in the remainder of this paper to identify any device parameter unique to a cell transistor.

In the neighborhood of corner **B** (Fig. 1), (1a) can be approximated by neglecting the current I_{aR}, through transistor M_{aR} whose gate–source voltage at **B** is below threshold. In the neighborhood of **A**, (1a) may be approximated by neglecting the current I_{pR}, through transistor M_{pR}, whose gate–source voltage is approximately equal to the threshold voltage. Similarly, (1b) may be approximated in the neighborhoods of **B′** and **A′** by neglecting the currents I_{aL} and I_{pL} in these neighborhoods, respectively. HSPICE simulations of the cell static transfer characteristics are shown in Fig. 3. The currents in (1a) are plotted in Fig. 3 as well, as a function of storage node voltage V_L. The above approximations can be seen to be valid, in the neighborhoods of **B** and **A**.

With these approximations, (1a) and (1b) in the neighborhood of **B** and **A′** reduce to

$$I_{nR} \cong I_{pR} \tag{2a}$$

$$I_{nL} \cong I_{aL}. \tag{2b}$$

For sub-100-nm generations, even if the subthreshold leakage current were merely two orders of magnitude smaller than the MOSFET on current, which corresponds to a device threshold voltage of barely 200 mV, the approximations assumed in (2a) and (2b) would still be valid. We can see this by looking at Fig. 3 on the right-hand side, corresponding to a linear scale of cell transistor currents. At regions in the neighborhood of **B** and **A**, the off currents of cell transistors would barely be a few percent

of the on currents, permitting (2a) and (2b) to maintain validity for scaled generations as well.

At **B**, the transistor M_{nR} operates in the saturation region and transistor M_{pR} operates in the linear region. From the Transregional model, neglecting the small exponential terms, we have

$$I_{pR} = \frac{W_{pR}\mu_{op}C_{ox}}{L\left(1+\theta_p\left(V_{dd}-V_L-V_{tpR}\right)\right)\left(1+\dfrac{V_{dd}-V_R}{LE_{cp}}\right)} \times \left(V_{dd}-V_L-V_{tpR}-\frac{V_{dd}-V_R}{2}\right)\left(V_{dd}-V_R\right) \tag{3}$$

$$I_{nR} = \frac{W_{nR}\mu_{\rm on}C_{ox}}{L\left(1+\theta_n\left[V_L-V_{tnR}\right]\right)}\frac{1}{\left(1+\dfrac{V_{dsatnR}}{LE_{cn}}\right)} \times \left\{\left(V_{dd}-V_{tnR}\right)V_{dsatnR}-\frac{V_{dsatnR}^2}{2}\right\} \tag{4a}$$

with

$$V_{dsatnR} = LE_{cn}\left(\sqrt{1+\frac{2\left(V_L-V_{tnR}\right)}{\eta LE_{cn}}}\right). \tag{4b}$$

Substituting (3) and (4) into (2a), we get a quadratic equation in $(V_{dd}-V_R)$ whose solution yields an approximation to the static transfer characteristic $F1$ of inverter I, in the neighborhood of **B**:

$$F1 \cong V_L+V_{tpR}+(V_{dd}-V_L-V_{tpR}) \times \sqrt{1-\frac{2I_{nR}}{\dfrac{W_{pR}\mu_{op}C_{ox}}{L(1+\theta_p[V_{dd}-V_L-V_{tpR}])}(V_{dd}-V_{\rm in}-V_{tpR})^2}}. \tag{5}$$

At point **A′**, transistor M_{nL} operates in the linear region and transistor M_{aL} in the saturation region. From the Transregional model, neglecting the small exponential terms

$$I_{nL} = \frac{W_{nL}\mu_{\rm on}C_{ox}}{L\left(1+\theta_n(V_R-V_{tnL})\right)\left(1+\dfrac{V_L}{LE_{cn}}\right)} \times \left(V_R-V_{tnL}-\frac{V_L}{2}\right)V_L \tag{6}$$

$$I_{aL} = \frac{W_{aL}\mu_{\rm on}C_{ox}}{L\left(1+\theta_n[V_{dd}-V_L-V_{taL}]\right)} \times \left\{\frac{1}{\left(1+\dfrac{V_{dsataL}}{LE_{cn}}\right)} \times \left((V_{dd}-V_L-V_{taL})V_{dsataL}-\frac{V_{dsataL}^2}{2}\right)\right\} \tag{7a}$$

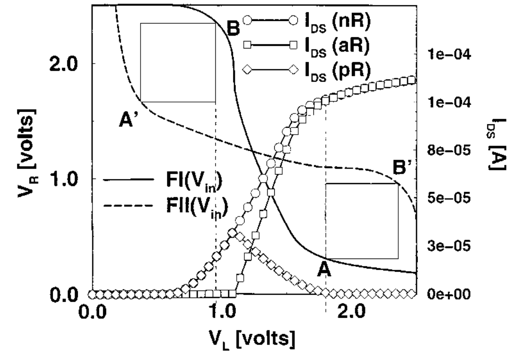

Fig. 3. HSPICE simulations of the cell static transfer characteristics. Parameter values used are listed in Table I. Transistor currents given by (1a) and (1b) in the neighborhood of the diagonally opposite corners of the maximum square, **B** and **A’**, can be approximated using (2a) and (2b).

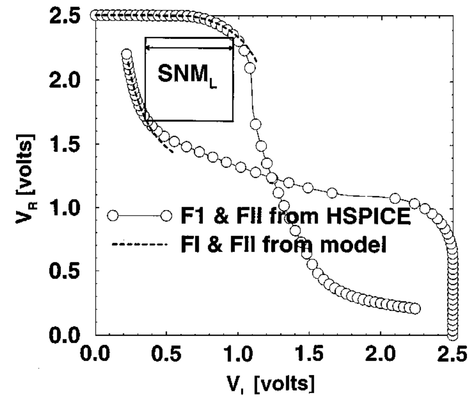

Fig. 4. The analytical models (5), (8) that approximate the static transfer characteristics in the neighborhood of the diagonally opposite corners of the maximum square are verified with HSPICE.

where

$$V_{dsataL} = LE_{cn}\left(\sqrt{1+\frac{2(V_{dd}-V_L-V_{taL})}{\eta LE_{cn}}}\right). \tag{7b}$$

On substituting (6) and (7) in (2b), we get a linear equation in V_R, solving which yields an approximation to $F2$ in the neighborhood of **A′** as

$$F2 \cong V_R = \frac{I_{aL}}{\dfrac{W_{nL}\mu_{\rm on}C_{ox}V_L}{L\left(1+\theta_n[V_{dd}-V_{tnL}]\right)\left(1+\dfrac{V_L}{LE_{cn}}\right)}}+\frac{V_L}{2}+V_{tnL}. \tag{8}$$

The above approximations to $F1$ (5) and $F2$ (8) are plotted in Fig. 4 and compared with the static transfer characteristics generated from HSPICE simulations. $F1$ and $F2$ are in excellent agreement with the static transfer characteristics around the corners of the maximum square permitting $F1$ and $F2$ to be employed below to analytically model the cell SNM.

The SNM is modeled as the side of the square nested between $F1$ and $F2$ with the *longest diagonal*, whose equation is given by

$$V_R = V_L + c. \tag{9}$$

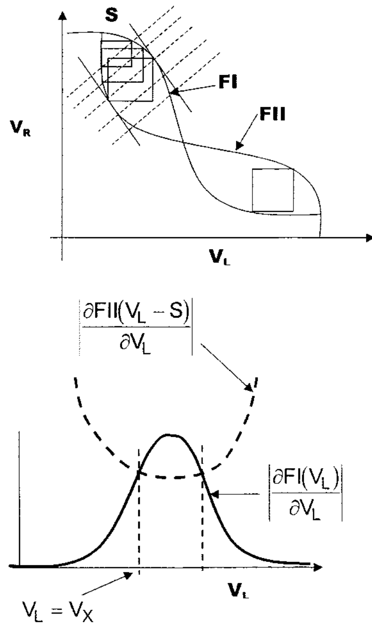

Fig. 5. The maximum square corresponds to the nested square with the longest diagonal and is determined by requiring the slopes of the static transfer characteristics to be equal when they touch the diagonally opposite corners of the nested squares.

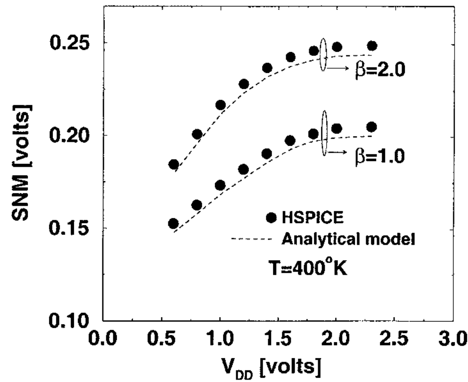

Fig. 6. SNM dependence for cell ratios of $\beta = 1, 2$ on V_{dd} using analytical model and HSPICE for a 0.18 μm CMOS process.

The intersection of this family of diagonals with $F1$ and $F2$ yields squares of side S (Fig. 5). Substituting (9) into (5) and (8) yields

$$F1(V_L) = V_L + c \tag{10a}$$

$$F2(V_L - S) = V_L - S + c. \tag{10b}$$

The side of a square is obtained by subtracting (10b) from (10a) in (11) below, and its maximum value obtained by equating the first partial derivative of S with respect to V_L to zero.

$$S = F1(V_L) - F2(V_L - S) \tag{11}$$

$$\left.\frac{\partial S}{\partial V_L}\right|_{S=\text{SNM}} = \frac{\partial F1(V_L)}{\partial V_L} - \frac{\partial F2(V_L - \text{SNM})}{\partial V_L} = 0. \tag{12}$$

Physically, (12) is equivalent to saying that the slopes of $F1$ and $F2$ are equal when $F1$ and $F2$ touch the diagonally opposite corners of the largest square. Substituting (5) and (8) into (12) yields a solution V_X, as the node voltage V_L at which $F1$ touches the corner of the maximum square. This solution of V_X substituted into (11) yields the SNM as

$$\begin{aligned}\text{SNM}_L &= V_X + V_{tpR} + (V_{dd} - V_X - V_{tpR}) \\ &\times \sqrt{1 - \frac{2I_{nRx}}{\frac{W_{pR}\mu_{op}C_{ox}}{L(1+\theta_p[V_{dd}-V_X-V_{tpR}])}(V_{dd}-V_X-V_{tpR})^2}} \\ &- \left[\frac{I_{aLx}}{\frac{W_{nL}\mu_{\text{on}}C_{ox}(V_X - \text{SNM}_L)}{L(1+\theta_n[V_{dd} - V_{tnL}])\left(1 + \frac{V_X - \text{SNM}_L}{LE_{cn}}\right)}} + \frac{V_X - \text{SNM}_L}{2} + V_{tnL}\right]\end{aligned} \tag{13}$$

where I_{nRx} is the saturation drain current of transistor M_{nR} when its gate–source voltage equals V_X and I_{aLx} is the saturation drain current of M_{aL} when its gate–source voltage equals $V_{dd} - V_X$. The suffix "L" of SNM in (13) corresponds to the maximum square between the corners **B** and **A′**. By swapping the cell right-hand-side parameters for the left-hand-side parameters in (13), the size of the maximum square nested between the corners **B′** and **A** can be obtained as

$$\begin{aligned}\text{SNM}_R &= V_X + V_{tpL} + (V_{dd} - V_X - V_{tpL}) \\ &\times \sqrt{1 - \frac{2I_{nLx}}{\frac{W_{pL}\mu_{op}C_{ox}}{L(1+\theta_p[V_{dd}-V_X-V_{tpL}])}(V_{dd}-V_X-V_{tpL})^2}} \\ &- \left[\frac{I_{aRx}}{\frac{W_{nR}\mu_{\text{on}}C_{ox}(V_X - \text{SNM}_R)}{L(1+\theta_n[V_{dd} - V_{tnR}])\left(1 + \frac{V_X - \text{SNM}_R}{LE_{cn}}\right)}} + \frac{V_X - \text{SNM}_R}{2} + V_{tnR}\right]\end{aligned} \tag{14}$$

with the SNM of the cell given by the smaller of (13) or (14). From (13) and (14) it can be seen that only transistors M_{pR}, M_{nR}, M_{aL} and M_{nL} contribute to SNM_L and transistors M_{pL}, M_{nL}, M_{aR} and M_{nR} contribute to SNM_R.

$$\text{SNM} = \min\left[\text{SNM}_L, \text{SNM}_R\right]. \tag{15}$$

Only for a perfectly symmetrical unperturbed cell is SNM_L equal to SNM_R. Mismatches between the right- and left-hand-side transistors of the cell produces an increase in $\text{SNM}_{L(R)}$ and a decrease in $\text{SNM}_{R(L)}$ with increases in SNM_R and SNM_L due to mismatches never occurring simultaneously. This model for SNM is plotted in Fig. 6 and verified with the SNM measured from HSPICE simulations of the same cell. Parameters used by the Transregional model and HSPICE in Figs. 3 and 4 are identical and are listed in Table I.

Given the variations in the threshold voltage of any of the six cell transistors, (13) and (14) permit assessing to what extent the SNM of the cell increases or decreases. The next section

TABLE I
PARAMETER VALUES USED IN TRANSREGIONAL MOSFET MODEL AND HSPICE

Symbol	Parameter	NFET Parameters	PFET parameters
V_{dd} (V)	Supply voltage	VDD=2.5	
L(μm)	Channel length	L=0.25 microns	
t_{ox}(A)	Gate oxide thickness	TOX=4.5E-9	
$\mu_{on,p}$ (V/cm-sec)	low field mobility	UO=305.46	UO=104.7
$v_{satn,p}$ (cm/sec)	Electron saturation velocity	VMAX=1E7	VMAX=8.3365E5
L_d (μm)	Lateral diffusion into channel from source/drain diffusion.	LD=0.025U	LD=0.025U
x_j (μm)	Junction depth	XJ=0.05U	XJ=0.05U
N_a (cm^{-3})	Substrate doping	NSUB=6.51E17	NSUB=6.51E17
ϕ_f (V)	Fermi potential in neutral bulk	PHI=0.456	PHI=0.456
N_g (cm^{-3})	Doping concentration in polysilicon gate	NGATE=1E19	NGATE=1E19
-	Type of gate material used: TPG=1, same as S/D diffusion	TPG=1	TPG=1
V_{to} (V)	Long-channel device threshold voltage	VTO=0.60	VTO=-0.60
θ (V^{-1})	Vertical field mobility degradation factor	THETA=0.1966	THETA=0.0679
ς_{jb} (F/cm^2)	Zero-bias bulk junction capacitance per unit area	CJ=1.9752E-3	CJ=1.9752E-3
-	Step function doping profile at junction boundaries	MJ=0.5	MJ=0.5
ζ_{jsw} (F/cm)	Zero-bias side-wall bulk junction capacitance per unit length	CJSW=7.9008E-11	CJSW=7.9008E-11
-	Bulk side-wall junction grading coefficient: 0.5 corresponds to a step junction.	MJSW=0.5	MJSW=0.5

describes how the above SNM model is employed to model stochastic distributions in SNM given the distributions of threshold voltage for each of the cell transistors.

III. STOCHASTIC DISTRIBUTIONS OF SNM

Using the "cube model" [3], a MOSFET may be viewed as an array of MOS capacitors separating the source from the drain. The distribution density function of effective doping concentration $f(n_a)$, the doping density required for a uniformly doped MOSFET without fluctuations to achieve a specific threshold voltage, is derived from a fundamental device analysis in [3]

$$f(n_a) = \sqrt{\frac{2}{\pi^2(\alpha^2+\gamma^2)}}\left\{\frac{(\varepsilon_s\varphi_B)^{1/4}}{N_a^{13/12}}\right\}\left[\exp\left\{\frac{-(p-\eta)^2}{2(\alpha^2+\gamma^2)}\right\}\right] \times\left[1+\frac{\gamma(p-\eta)}{(\alpha^2+\gamma^2)}\left\{\frac{1-2p}{2LN_a^{1/3}\sqrt{p(1-p)}}\right\}\right] \times\left[\frac{\exp\left\{\frac{-\left(n_aXN_a^{-2/3}-XN_a^{1/3}\right)^2}{2XN_a^{1/3}}\right\}}{1+\mathrm{erf}\left(\sqrt{\frac{XN_a^{1/3}}{2}}\right)}\right] \tag{16}$$

$$\gamma = \frac{\sqrt{p(1-p)}}{LN_a^{1/3}} \tag{17}$$

$$\alpha = 0.149\exp\left(-0.0636\,LN_a^{1/3}\right) \tag{18}$$

$$\eta = 0.59. \tag{19}$$

In (16)–(19), n_a is the variable doping concentration for an individual MOS capacitor, N_a is the average doping concentration, and X is the depth of the device active region. Based on the effective doping concentration, the threshold voltage distribution density function F_{Vts} is derived in [3] as

$$F_{Vts} = \frac{W}{L}\left(1-\int_0^{n_a} f(t)\,dt\right)^{(W/L)-1} f(n_a)\times\frac{dn_a}{dV_{ts}} \tag{20}$$

where $V_{ts} = V_{th} + \Delta V_{th}$, and V_{th} and ΔV_{ts} are the long channel threshold voltage and the short channel threshold voltage roll-off, respectively [7]. W and L are the channel width and length, respectively. For uniformly doped MOSFETs the threshold voltage distribution and standard deviations are calculated in [3] using (16) and (20).

Given the above stochastic distributions of threshold voltage of each cell transistor, a methodology to assess the cumulative impact of intrinsic fluctuations in all cell transistors on SNM

TABLE II
INPUT PARAMETERS FOR CALCULATING THRESHOLD VOLTAGE AND SNM DISTRIBUTIONS DUE TO INTRINSIC FLUCTUATIONS [3]

year	1997	1999	2001	2003	2006	2009	2012
L (nm)	250	180	150	130	100	70	50
T_{ox} (nm)	4.5	3.5	2.8	2.3	1.7	1.2	0.8
V_{dd} (V)	2.2	1.8	1.5	1.2	1.0	0.8	0.5
V_{th} (V)	0.45	0.40	0.35	0.33	0.30	0.28	0.2
N_a (cm^{-3})	5.95e17	8.0e17	9.5e17	1.22e18	1.8e18	2.9e18	4.85e18
σVth (mV)	21	23	25	27	28	30	32

is described below. The threshold voltages of the cell transistors may be viewed as six *independent random variables* and the SNM, given by (13) or (14) as a function of four of these six random variables. Since the microscopic threshold voltage fluctuations of each cell transistor are independent of each other, their cumulative impact on cell SNM may be assessed as the sum of the fluctuations in SNM produced individually by threshold voltage fluctuations in each of the six cell transistors.

$$\Delta\mathrm{SNM}_L = \Delta\mathrm{SNM}_{aL} + \Delta\mathrm{SNM}_{nL} + \Delta\mathrm{SNM}_{nR} + \Delta\mathrm{SNM}_{pR} \tag{21a}$$

$$\Delta\mathrm{SNM}_R = \Delta\mathrm{SNM}_{pL} + \Delta\mathrm{SNM}_{nL} + \Delta\mathrm{SNM}_{nR} + \Delta\mathrm{SNM}_{aR} \tag{21b}$$

where $\Delta\mathrm{SNM}_{ij}$, in the RHS of (21) is the fluctuation in $\mathrm{SNM}_{L(R)}$ produced by a fluctuation in *only* the threshold voltage of cell transistor M_{ij} with $i \in a, n, p$ and $j \in R, L$. The pdf of cell $\mathrm{SNM}_{L(R)}$, may be determined by *convolving* [11] the individual pdfs of SNM produced by fluctuations in threshold voltage in each of the cell transistors.

$$f(\mathrm{SNM}_L) = f(\mathrm{SNM}_{aL}) * f(\mathrm{SNM}_{nL}) * f(\mathrm{SNM}_{nR}) * f(\mathrm{SNM}_{pR}) \tag{22a}$$

$$f(\mathrm{SNM}_R) = f(\mathrm{SNM}_{pL}) * f(\mathrm{SNM}_{nL}) * f(\mathrm{SNM}_{nR}) * f(\mathrm{SNM}_{aR}). \tag{22b}$$

Given the pdfs of the threshold voltage of a cell transistor M_{ij}, the pdf of SNM_{ij}, $f(\mathrm{SNM}_{ij})$ due to fluctuations *only* in threshold voltage of M_{ij} is obtained using [11]

$$f(\mathrm{SNM}_{ij}) = \frac{f(V_{Tij})}{\dfrac{\partial(\mathrm{SNM}_{L(R)})}{\partial V_{Tij}}}. \tag{23}$$

Since the partial derivative in the denominator of (23) is analytically intractable, it is calculated numerically for each transistor M_{ij} using (13) or (14) for a number of V_T in the neighborhood of V_{T0}. The cell SNM varies linearly in the neighborhood of $VT0$ and the denominator of (23) is approximated as a constant in this neighborhood. The threshold voltage distributions, $f(V_{Tij})$ from [3] are approximated as Gaussian using

$$f(V_{Tij}) \cong \frac{1}{\sqrt{2\pi\sigma_{V_{Tij}}^2}} \exp\left(-\frac{(V_{Tij} - V_{T0})^2}{2\sigma_{V_{Tij}}^2}\right) \tag{24}$$

where $\sigma_{V_{Tij}}$ equals the standard deviation in threshold voltage of transistor M_{ij} and V_{T0} equals its mean threshold voltage.

Substituting (24) and the numerically calculated partial derivative of SNM wrt V_{Tij} into (23) for each of the cell transistors yields the individual pdf of SNM due to fluctuations in threshold voltage of each cell transistor. Convolving these independent pdfs yields the joint pdf of cell SNM in (22) using

$$f_W(w) = \int_{-\infty}^{\infty} f_Y(y) f_X(w-y)\, dy \tag{25}$$

where the pdf of $W = X + Y$, the sum of two independent random variables X and Y, equals the convolution of their pdfs.

The next section applies this methodology of calculating the joint pdf of cell SNM to the technology nodes at the far end of the NTRS where intrinsic fluctuations in device threshold voltage are shown to have a devastating effect on SRAM cell stability.

IV. CMOS SRAM STABILITY PROJECTIONS

The physical and stochastic models developed in the previous two sections are now applied to the CMOS technology nodes across the 1997 NTRS to calculate the stochastic distributions in cell SNM for each node. Threshold voltage distribution functions are calculated for each node using the input parameters listed in Table II from the roadmap, for minimum-geometry uniformly doped MOSFETs. The threshold voltage distribution functions calculated using (16)–(20) [3] are plotted in Fig. 7 with standard deviations in threshold voltage listed in Table II as well.

The threshold voltage distribution function is approximated as a Gaussian with an identical distribution function assumed for each of the minimum geometry cell transistors. The individual distributions in SNM, due to variations in each cell transistor M_{ij}, given by $f(\mathrm{SNM}_{ij})$ are calculated for each of the cell transistors. The individual sensitivities and pdfs of SNM_L due to the four cell transistors M_{aL}, M_{nL}, M_{nR} and M_{pR} are plotted in Figs. 8 and 9, respectively, for the 50 nm generation. These figures reveal cell SNM to be *most sensitive* to threshold voltage fluctuations in the access and pull-down NFETs and *least sensitive* to the fluctuations in the pull-up PFET device. The joint pdf of SNM is now calculated for four representative technology nodes using (22a) or (22b) and plotted in Fig. 10. This calculation proceeds assuming a ΔT of 100 K above room temperature. The calculations of SNM distributions at high temperature constitutes the worst case since cell SNM decreases as device threshold voltages are lowered, with increases in temperature. The standard deviations in cell SNM (Table III) show an

TABLE III
CALCULATED VALUES OF VARIATIONS IN SNM AROUND ITS MEAN VALUE: $T = 400$ K

L	250nm	180nm	130nm	70nm	50nm
SNM (mV)	256	209	143	82	60
σ SNM (mV)	8	9	11	14	16

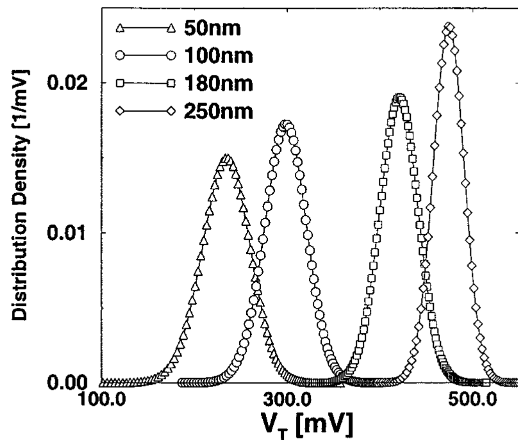

Fig. 7. Distribution density functions for threshold voltage for each of the 1997 NTRS generations using models from [3].

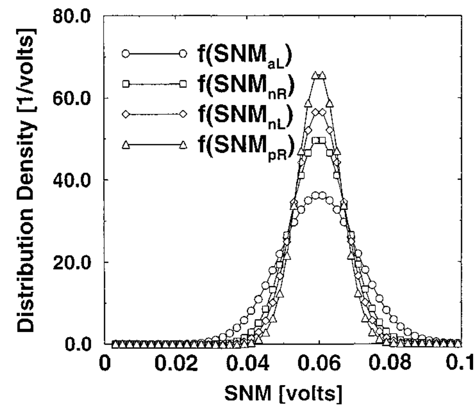

Fig. 9. Distribution density function in SNM due to variations in each cell transistor. Device parameters used for the 50-nm node are listed in Table II. SNM is most sensitive to access NFETs and least sensitive to pull-up P-channel devices.

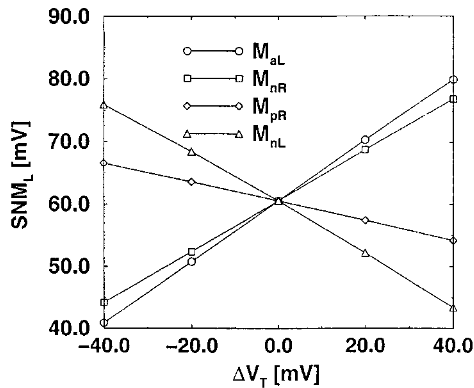

Fig. 8. Sensitivities of SNM_L to variations in device threshold voltage of each cell transistor. The SNM is least sensitive to V_t variations of the pull-up PFETs and most sensitive to V_t variations in the access transistors and the pull-down NFETs, with the slope of the SNM Vs ΔV_t curve reaching as high as 0.5 for the access devices. Plot shows calculations for the 50-nm generation. Device and circuit parameters are defined in Table II.

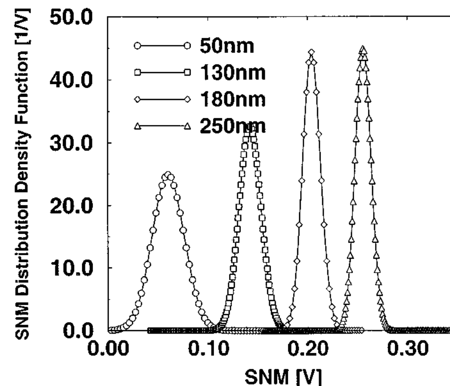

Fig. 10. Joint distribution density functions of SNM due to intrinsic threshold voltage fluctuations in all cell transistors using (22). Device parameters used are listed in Table II.

increase from 8 mV for the 250-nm generation to 16 mV for the 50-nm generation. Expressed as a percentage of the SNM, the standard deviation in SNM due to intrinsic atomic fluctuations increases from 3% to 26%.

At the device level, one proposed solution to alleviate the effects of intrinsic fluctuations [12] has been to use retrograde doping profiles in cell transistors and also use channel lengths that are marginally larger than minimum feature size. This alleviates the problem but does not eliminate it altogether. Circuit techniques that boost cell storage node voltages away from each other would improve cell SNM, making it more immune to noise, and are proposed in [13] as a solution that holistically addresses cell stability, subthreshold leakage, and performance degradation in scaled CMOS SRAMs.

V. CONCLUSION

New physical and stochastic models for 6T CMOS SRAM cell SNM are derived. These enable accurately assessing the impact of stochastic variations in device threshold voltage due to random placement of dopant atoms on cell stability by conjointly employing physical short-channel MOSFET drain current and threshold voltage roll-off models in tandem with stochastic models for intrinsic fluctuations of device threshold voltage. Stochastic distributions of cell SNM across the 1997 NTRS technology nodes calculated using these models demonstrate substantial reductions in cell SNM for sub-100-nm technology generations.

REFERENCES

[1] R. W. Keyes, "The effect of randomness in the distribution of impurity atoms on FET threshold," *App. Phys.*, vol. 8, pp. 251–259, 1975.

[2] T. Mizuno, J. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuations using an 8K MOSFET array," in *Proc. Symp. VLSI Tech.*, Jun. 1993, pp. 41–42.

[3] X. Tang, V. De, and J. D. Meindl, "Intrinsic MOSFET parameter fluctuations due to random dopant placement," *IEEE Trans. VLSI Syst.*, vol. 5, pp. 369–376, Dec. 1997.

[4] D. Burnett, K. Erington, C. Subramanian, and K. Baker, "Implications of fundamental threshold voltage variations for high-density SRAM and logic circuits," in *Proc. Symp. VLSI Tech.*, June 1994, pp. 15–16.

[5] E. Seevinck, F. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 748–754, Oct. 1987.

[6] A. J. Bhavnagarwala, B. L. Austin, K. A. Bowman, and J. D. Meindl, "A minimum total power methodology for projecting limits on CMOS GSI," *IEEE Trans. VLSI Syst., Special Issue on Low Power*, vol. 8, pp. 235–251, June 2000.

[7] K. A. Bowman, B. L. Austin, J. C. Eble, X. Tang, and J. D. Meindl, "A physical alpha-power law MOSFET model," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1410–1414, Oct. 1999.

[8] A. Agrawal, V. De, and J. D. Meindl, "Opportunities for scaling FETs for gigascale integration (GSI)," in *Proc. 23rd ESSDERC*, Sept. 1993, pp. 919–926.

[9] "The national technology roadmap for semiconductors," SIA, 1997.

[10] J. Lohstroh, E. Seevinck, and J. Groot, "Worst-case noise margin criteria for logic circuits and their mathematical equivalence," *IEEE J. Solid State Circuits*, vol. SC-18, pp. 803–806, Dec. 1983.

[11] P. Peebles Jr., *Probability, Random Variables and Random Signal Principles*. New York: McGraw Hill, 1987, ch. 3–4.

[12] X. Tang, V. K. De, and J. D. Meindl, "MOSFET fluctuation limits on gigascale integration (GSI)," in *1998 Eur. Solid-State Device Research Conf. (ESSDERC'98)*, Bordeaux, France, Sept. 1998, pp. 508–511.

[13] A. J. Bhavnagarwala and J. D. Meindl, "Dynamic threshold CMOS SRAM cells for fast portable applications," in *Proc. 14th IEEE Int. ASIC/SOC Conf.*, Arlington, VA, Sept. 2000, pp. 359–363.

Azeez J. Bhavnagarwala (S'92) was born in Madras, India. He received the B.S. degree (cum laude) in 1992 in electrical engineering from Rensselaer Polytechnic Institute (RPI), Troy, NY, and from the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland. He received the M.S. degree in electrical engineering from RPI in 1994. He is currently working toward the Ph.D. degree in electrical engineering at the Georgia Institute of Technology, Atlanta.

He was with Integrated Device Technology (IDT) in 1996, and with LSI Logic in 1999 working on interconnect and device modeling. His research interests are voltage scaling constraints for CMOS technologies.

Xinghai Tang (S'96–M'99) was born in Heilongjiang, R.O.C. He received the B.S.E.E. and M.S.E.E. degrees from Beijing Institute of Technology, R.O.C., in 1985 and 1988, respectively. He received the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, in 1999.

Currently, he is with the Somerset Design Center of Motorola, Inc., Austin, TX. His primary research interests are high-performance/low-power device structures and circuit techniques. He has authored over 20 technical publications in refereed international conferences and journals.

James D. Meindl (M'56–SM'66–F'68–LF'97) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Carnegie Mellon University, Pittsburgh, PA, in 1955, 1956, and 1958, respectively. He is currently the Director of the Joseph M. Pettit Microelectronics Research Center and the Pettit Chair Professor of Microelectronics at the Georgia Institute of Technology, Atlanta. Previously, he served from 1986 to 1993 as Senior Vice President for Academic Affairs and Provost of Rensselaer Polytechnic Institute, Troy, NY. From 1967 through 1986 he was with Stanford University, Stanford, CA, where he was John M. Fluke Professor of Electrical Engineering, Associate Dean for Research in the School of Engineering, Director of the Center for Integrated Systems, Director of the Electronics Laboratories, and Founding Director of the Integrated Circuits Laboratory. He is a Co-Founder of Telesensory Systems, Inc., the principal manufacturer of electronic reading aids for the blind, and served as a member of the Board from 1971 through 1984. From 1965 through 1967 he was Founding Director of the Integrated Electronics Division at the U.S. Army Electronics Laboratories, Fort Monmouth, NJ. He is the author of the book *Micropower Circuits* and over 500 technical papers on ultralarge-scale integration, integrated electronics, and medical electronics. He is also editor of the book *Brief Lessons in High Technology*, which elucidates the most important economic event of our lives, the emergence of the information society.

Dr. Meindl is a Life Fellow of the American Association for the Advancement of Science, and a member of the American Academy of Arts and Sciences and the National Academy of Engineering and its Academic Advisory Board. He received the IEEE Third Millennium Medal, the 1999 SIA University Research Award, the 1997 Hamerschlag Distinguished Alumnus Award from Carnegie Mellon University, and the 1991 Benjamin Garver Lamme Medal from the American Society for Engineering Education. He was the recipient of the 1990 IEEE Education Medal for establishment of a pioneering academic program for the fabrication and application of integrated circuits, and the recipient of the 1989 IEEE Solid-State Circuits Medal for contributions to solid-state circuits and solid-state circuit technology. At the 1988 IEEE International Solid-State Circuits Conference, he received the Beatrice K. Winner Award. In 1980 he was the recipient of the IEEE Electron Devices Society J. J. Ebers Award for his contributions to the field of medical electronics and for his research and teaching in solid-state electronics. From 1970 through 1978 he and his students received five outstanding paper awards at IEEE International Solid-State Circuits Conferences, along with one received at the 1985 IEEE VLSI Multilevel Interconnections Conference. His major contributions have been new medical instruments enabled by custom integrated electronics, projections and codification of the hierarchy of physical limits on integrated electronics, and leadership in creation of academic environments promoting high-quality teaching and research.