

Generic Models for Interconnect Delay across Arbitrary Wire-tree Networks

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Abstract[†]

New, generic and compact closed-form expressions for distributed wire-tree delay dependence on input ramp time, tree topology and wire geometries are reported. In agreement to within 5% of HSPICE simulations, these expressions permit rapid, accurate and early estimates of interconnect delay as well as variations in interconnect delay due to variations in interconnect process parameters across arbitrary distributed wire-tree networks.

Introduction

First-order path-tracing RC tree methods [1] based on the Elmore delay model [2] lack in accuracy in estimating delays across distributed wire-tree networks. The Q^{th} order and more accurate Asymptotic Waveform Evaluation (AWE) extensions [3-5] require formulating and solving nodal matrices where computational effort and memory requirements increase with chip and wire-tree complexity even though these techniques are more efficient than real-time HSPICE simulations. With scaling of minimum feature size and increase in chip size, complexity and gate count, not only do interconnect delays consume larger fractions of total path delays but variations in path delay due to back-end-of-line (BEOL) interconnect process variations begin to dominate over front-end-of-line (FEOL) device parameter variations as well [6,7]. Using any of the above RC-tree models to estimate wire-tree delay and/or variations in wire-tree delay would incur increasing costs in accuracy or in computational time and effort with scaling of feature size. Sakurai's accurate (<3% error) closed-form analytical models for distributed interconnect delay [8] that apply only to the case of step excitations at the input of a buffer driving a 2-pin net are extended in this work to the more commonly encountered and complex cases of branched network topologies and linear ramp/exponentially saturating input waveforms. These new models permit fast, accurate and early estimates of delay and variations in delay along arbitrary wire-tree networks with immediate applications to the design and optimization of clock signal distribution nets for minimum skew.

Interconnect response to non-zero rise time

The frequency-domain interconnect response to a step input function [8] given by (1a) in the Appendix, may be analytically extended to the case of a ramp input (1b), (2) by making a Taylor expansion (3a) of the first term on the RHS of (2). This expansion translates the time-domain interconnect response to a step *by exactly half the ramp time* using the Laplace operator in (4b). Comparison of Sakurai's

interconnect response model (5a) shifted by half the ramp time (5b) with HSPICE simulations are shown to be in excellent agreement in Figs. 1 and 2 for different cases of ramp time and wire geometry. The 50%-50% *propagation delay* between buffer input and interconnect response at the far-end of the distributed line is thus *independent of rise time at input*. For the case of an exponentially saturating waveform driving the input of a buffer, since short-channel devices behave as a constant current source for most of the transition at the output, for reasonably fast input transitions, the 20-80% rise time of the exponentially saturating input waveform can be replaced with a linear ramp of identical 20-80% transition time centered around the 50% points [9]. For the case of an interconnect driving another interconnect (as encountered at a branch or between levels in a multilevel interconnect architecture), the frequency-domain response of the interconnect downstream is modeled by (7b), (8b) where a Taylor expansion of the first term in the RHS of (7b) yields the result that the step-input response is shifted *exactly by the time constant of the exciting waveform* (9). Comparison of (9) with HSPICE in Fig. 3 demonstrates excellent agreement of this model as well. Expression for propagation delay (10) shows dependencies on the time constant of the exponentially saturating exciting waveform unlike the case of a linear ramp input.

Response at intermediate nodes in a chain of nets

Exact time-domain solutions for voltage and current waveforms at any arbitrary intermediate position along a uniform distributed 2-pin wire are given by (11) from [8]. This exact solution assumes C_T and R_T given by (6) to be zero. Using the approximations in (12b) and (12c), addition of driver resistance and load capacitance is included into (11) to yield (12a) in the same way that (5a) was derived in [8]. The higher order terms ($k>1$) in the multi exponential expansion of the time domain solution in (12a) make insignificant contributions. The equivalent of position x in (11) and (12a) along the 2-pin wire is modeled as the ratio of resistance seen upstream (for the chain of nets in Fig 4a) to total path resistance (13b). Excellent agreement is observed between (13) and HSPICE for point 'A1' in the schematic of the wire chain shown in Fig 4.

Propagation delay across arbitrary wire tree networks

The response at the end node (C) of the longest path in an arbitrary tree network (Fig. 5) may be modeled accurately by replacing the network between the driver and the node of interest with a 'black box' (dotted lines in Fig 5). The interconnect response given by (14) describes the waveform at the end of the longest path for a given network. The total resistance seen between terminals A and C of the 'black box' given by (15b) and the total capacitance (15c) seen between the same terminals replace the distributed wire

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resistance and capacitance - R and C used in (5). The accuracy of (14), applicable only to the longest path, deteriorates if the tree network has *many short* branches to one of which the above model is applied. This is so because the 'effective capacitance' seen at branch points with high fan-outs would be lower than predicted by (15c). To remedy the inaccuracies due to the shielding of wire capacitance by its resistance, resulting from applying (14) to nodes closer to the source (say, X, D or B in Fig 5), we apply the model for intermediate nodes (13a) to node X in Fig 5 and calculate the propagation delay from node X to node D in the same example using the model for exponentially saturating inputs given by (10). The propagation delay to nodes closer to the source: D, B and X in the example in Fig. 5 can thus be calculated very accurately using (16) and (17). Table I compares the above model with calculations using Elmore's model and HSPICE for the same circuit in Fig 5.

Conclusions and Summary

New, accurate, simple and readily usable closed form analytical expressions are reported that predict propagation delay across arbitrary, distributed wire-tree networks. These expressions *do not* require numerical calculation of 'effective capacitance', are shown to be much more accurate than the commonly used Elmore delay model, and require much less computational complexity than the commonly used AWE numerical techniques as well. These new delay models are within 5% accurate of HSPICE simulations and provide *unprecedented* opportunities to rapidly and accurately estimate delay and variations in delay along arbitrary wire-tree networks.

Appendix: Interconnect response models:

(A) Step [8] and ramp input response of 2-pin net in s-domain: (Figs 1 & 2)

$$(1a) V_{step}(s) = V_{in}(s)H(s) = \frac{1}{s}H(s); (1b) V_{ramp}(s) = V_{in}(s)H(s) = \frac{(1 - e^{-st_{ramp}})}{s^2 t_{ramp}} H(s); (2) V_{ramp}(s) = \frac{(1 - e^{-st_{ramp}})}{st_{ramp}} V_{step}(s)$$

$$\text{Approximation: } (3a) \frac{1 - e^{-x}}{x} \cong e^{-\frac{x}{2}}; (3b) V_{ramp}(s) \cong e^{-\frac{st_{ramp}}{2}} V_{step}(s)$$

$$\text{Laplace Transform pairs: } (4a) e(t) \leftrightarrow E(s); (4b) e(t - t_o) \leftrightarrow e^{-st_o} E(s)$$

$$(5a)[8] \frac{V_{step}(t)}{V_{dd}} = 1 - e^{-\left(\frac{t}{R_T C_T + R_T + C_T + 0.4}\right)}; (5b) \frac{V_{ramp}(t)}{V_{dd}} = 1 - e^{-\left(\frac{t}{R_T C_T + R_T + C_T + 0.4}\right)} \left(\frac{t}{RC} - 0.1\right)$$

$$(6a) R_T = \frac{R_r}{R}; (6b) C_T = \frac{C_L}{C}; (6c) R_{tr} = \frac{V_{dd}}{I_{dsat}[V_{dd}, V_{dd}, 0]}$$

(C) Interconnect response at intermediate nodes along chain of distinguishable nets (Fig 4)

$$(11) [8] \frac{v(x, t)}{V_{dd}} = 1 + \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{(-1)^k}{k - \frac{1}{2}} \cos\left[\left(k - \frac{1}{2}\right)\pi\left(1 - \frac{x}{L}\right)\right] e^{-\left[\left(k - \frac{1}{2}\right)^2 \pi^2\right]\left(\frac{t}{RC}\right)}$$

For loaded nets driven by non-zero driver resistance :

$$(12a) \frac{v(x, t)}{V_{dd}} = 1 + \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{(-1)^k}{k - \frac{1}{2}} \cos\left[\left(k - \frac{1}{2}\right)\pi\left(1 - \frac{x}{L}\right)\right] e^{-\left[\frac{1}{\left(k - \frac{1}{2}\right)^2 \pi^2 + R_T C_T + R_T + C_T}\right]\left(\frac{t}{RC}\right)}$$

$$; \text{ for } k=1 \text{ only, } (12b) \frac{1}{\left(k - \frac{1}{2}\right)^2 \pi^2} \cong 0.4 \text{ and } (12c) \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{(-1)^k}{k - \frac{1}{2}} \cong -e^{-0.4}$$

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(B) Exponentially saturating input response of 2-pin net driven by interconnect: (Fig. 3)

$$(7a) V_{in}(t) = V_{dd} \left(1 - e^{-\frac{t}{\tau}}\right)$$

$$(7b) V_{exp}(s) = V_{in}(s)H(s) = \frac{1}{s(\tau s + 1)} H(s) = \frac{1}{(\tau s + 1)} V_{step}(s)$$

$$\text{Approximation: } (8a) \frac{1}{s\tau + 1} \cong e^{-s\tau} (8b) V_{exp}(s) = e^{-s\tau} V_{step}(s)$$

$$\text{Time-domain response: } (9) \frac{V_{exp}(t)}{V_{dd}} = 1 - \exp\left[-\frac{t - \tau}{C_T + 0.4}\right]$$

Propagation delay:

$$(10) t_{pd_A \rightarrow B} = 0.3\tau + RC[(C_T + 0.4)\ln 2 + 0.1]$$

For node A1 in Fig 4

$$(13a) \frac{V_{A1}(t)}{V_{dd}} = 1 - \cos\left(\frac{\pi}{2}\left(1 - \frac{R_{upstream}}{\sum R_{path}}\right)\right) \times \exp\left(-\frac{\frac{t - t_{ramp}}{2} - 0.1}{R_T C_T + R_T + C_T + 0.4}\right); \quad (13b) \sum R_{path} = R_{int1} + R_{int2} + R_{int3}; \quad (13c) \sum C_{path} = C_{int1} + C_{int2} + C_{int3}$$

$$(13d) R_{upstream} = R_{int1}$$

(D) Wire-tree networks: (Fig 5), At node C in the example of Fig. 5:

$$(14a) \frac{V_{ramp}(t)}{V_{dd} \text{ nodeC}} = 1 - \exp\left(-\frac{\frac{t - t_{ramp}}{2} - 0.1}{\left(\frac{\sum R}{path}\right)\left(\frac{\sum C}{path}\right) R_T C_T + R_T + C_T + 0.4}\right)$$

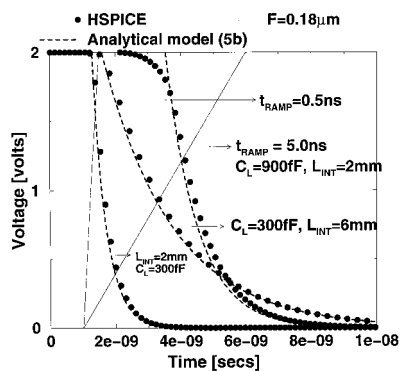
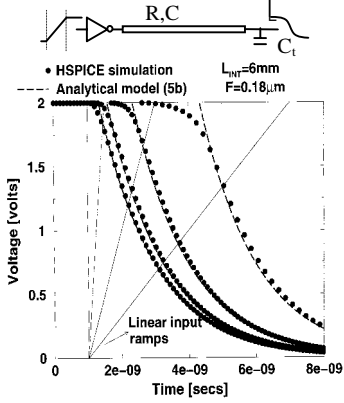
At node X in the example in Fig. 5:

$$(16) \frac{V_{ramp}(t)}{V_{dd} \text{ nodeX}} = 1 - \cos\left(\frac{\pi}{2}\left(1 - \frac{R_{upstream}}{\sum R_{path}}\right)\right) \times \exp\left(-\frac{\frac{t - t_{ramp}}{2} - 0.1}{\left(\frac{\sum R}{path}\right)\left(\frac{\sum C}{path}\right) R_T C_T + R_T + C_T + 0.4}\right)$$

$$(16b) R_{upstream} = R_{int1}$$

Propagation delay to node D in Fig 5: (17a) $t_{pd_A \rightarrow D} = t_{pd_A \rightarrow X} + t_{pd_X \rightarrow D}$

$$(17b) t_{pd} = \sum R_{path} \times \sum C_{path} \left[(R_T C_T + R_T + C_T + 0.4) \ln \left[2 \cos \left(\frac{\pi}{2} \left(1 - \frac{R_{int1}}{\sum R_{path}} \right) \right) \right] \right] + 0.1 + 0.3\tau_x + R_{int3} C_{int3} \left[\left(\frac{C_3}{C_{int3}} + 0.4 \right) \ln 2 + 0.1 \right]$$



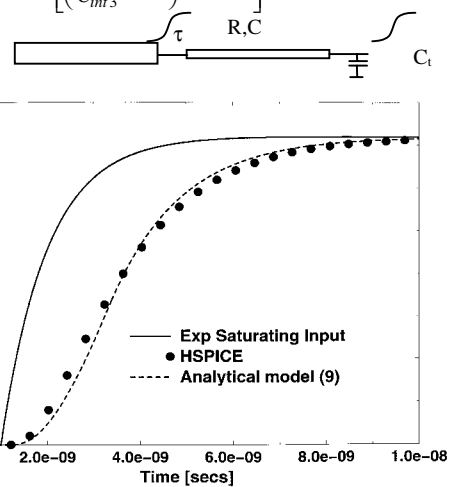
For node C (longest path) in Fig 5

$$(14b) R_T = \frac{R_{tr}}{\sum R_{path}}; \quad (14c) C_T = \frac{C_L}{\sum C_{path}}$$

$$(15a) t_{pd} = \left(\frac{\sum R}{path} \right) \left(\frac{\sum C}{path} \right) (R_T C_T + R_T + C_T + 0.4) \ln(2) + 0.1$$

$$(15b) \left(\frac{\sum R}{path} \right) \text{ (for node C in Fig 5)} = R_{int1} + R_{int2} + R_{int5};$$

$$(15c) \left(\frac{\sum C}{path} \right) \text{ (for node C in Fig 5)} = C_{int1} + C_1 + C_{int2} + C_{int3} + C_3 + C_{int4} + C_4 + C_{int5}$$



Figures 1 & 2: Comparison of 2-pin interconnect response model (5b) with HSPICE for different wire geometries and ramp times

Figure 3: Interconnect response to exponentially saturating inputs

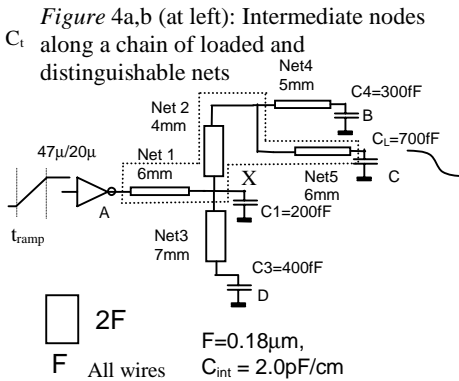
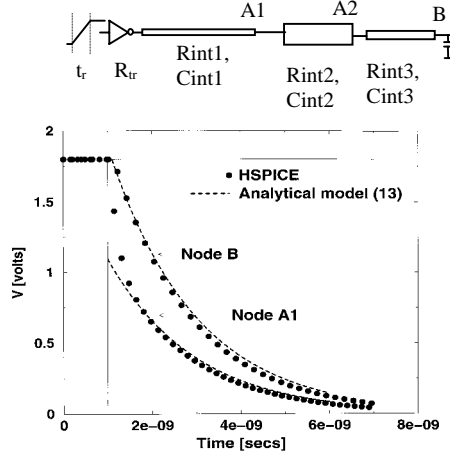


Figure 5: Arbitrary wire-tree network example

node	Propagation delay (ns)				
	HSPICE	New model	Error %	Elmore model	Error %
B	19.05	18.4	3.41	27.2	42.8
C	22.35	22.2	0.70	28.9	29.3
D	14.47	13.7	4.86	21.9	51.3

Table I: Comparison of HSPICE with new model and the Elmore delay model for the circuit in Fig. 5.