

# Dynamic-Threshold CMOS SRAMs for Fast, Portable Applications

A. J. Bhavnagarwala and J. D. Meindl

Georgia Institute of Technology, Atlanta GA 30332  
gt6994b@prism.gatech.edu

## Abstract<sup>†</sup>

*A novel quad-rail CMOS SRAM cell architecture that doubles cell read current, improves cell static noise margin (SNM) by 70%, increases cell immunity to SER, and lowers cell standby power by over an order of magnitude is proposed. These improvements over conventional 6T CMOS SRAM cells, verified with HSPICE simulations on a 0.18 $\mu$ m industrial process are achieved by implementing a scheme of WL transition triggered pulses on power, ground and substrate terminals of cell transistors that share a common WL.*

## 1. Introduction

With scaling of MOSFET dimensions, microscopic variations [1-3] in number and location of dopant atoms in the channel region of the device induce increasingly limiting electrical deviations in device threshold voltage [3]. These atomic level intrinsic fluctuations are most pronounced in minimum geometry transistors commonly used in area constrained circuits such as SRAM cells [4]. Narrow width effects, SER, low voltage operation, temperature and process variations, and parasitic transistor resistance all contribute additionally to the increasing instability of a conventional 6T SRAM cell as well [5-8]. With projected increases in percentage of chip transistors devoted to cache [9], in high performance microprocessors and ASICs, subthreshold leakage currents from an overwhelming number of inactive cells are projected to become larger than the AC currents from a much smaller number of active circuits [10] placing limits on the scaling of threshold voltage of cell transistors. The Bit Line (BL) delay determined primarily by BL capacitance, cell read current and sensitivity of the sense amplifiers, increasingly limits SRAM performance [11] since BL capacitance and sense amplifier sensitivity do not scale as rapidly as minimum feature size [5]. Raising the  $V_T$  of cell transistors reduces standby power dissipation from the cell array but imposes a severe penalty on BL delay by compromising cell read current from minimum geometry cell transistors. Several

innovative SRAM cell architectures [12-14] have been proposed to alleviate one or more of the above limitations facing SRAM cell scaling. However, in all of these (i) the improvements in cell drive obtainable by cell voltage/overdrive boosting are *dampened by the high  $V_T$  of cell transistors* and (ii) the opportunity to *use the substrate terminal of the cell transistors to control leakage and improve cell stability and performance* is not pursued. In this work, we propose a new circuit technique that *does not require trading off subthreshold leakage for cell drive.*

## 2. Speed and stability improvements

Driving the source terminal of cell inverter MOSFETs (Fig. 1 a, b) *marginally* outside the  $V_{dd}$ -Gnd range, by voltages less than the built-in potential of a p-n junction (to avoid forward bias leakage) translates into substantial increases in read current. This increase in read current is larger than that obtained by driving any of the other MOSFET terminals by the same voltage swing because all of the following contribute to drive increase (i) increase in gate-source voltage (ii) increase in drain-source voltage for devices with finite output resistance and (iii) reductions in device threshold voltage due to forward bias on the source-body p-n junction. The series-connected cell access transistors drive more current as well since *the low and high storage nodes of the cell are driven past the  $V_{ss}$  and  $V_{dd}$  voltage levels* (Fig. 2b), boosting the gate-source, drain-source and source-body voltages of the access transistors as well. *Both - the BL discharge path as well as the BLB charge path are dilated* translating into a doubling of cell read current (Fig. 2a). In a conventional CMOS SRAM cell, the stored data is most vulnerable to noise only during a read access [6] because the '0' storage node voltage, rises above ground during a read access due to voltage division along the access and inverter pull-down NFET devices. The ratio of the widths of the pull-down transistor to the access transistor, commonly referred to as the *cell ratio* or *beta ratio*, determines how high the '0' storage node rises during a read access. Smaller cell ratios translate into a bigger voltage drop across the pull-down transistor requiring a smaller noise voltage at the '0' node to trip the cell. Driving the source terminals of

<sup>†</sup> This work was supported by the Defense Advanced Research Project Agency (Contract: F3361595C1623) and the Semiconductor Research Corporation (SJ-374-002)

the cell pull-down NFETs below  $V_{ss}$  ensures enough room for the voltage drop across the pull-down device so that *the '0' storage node does not rise above ground during a read access* (Fig. 2b). An alpha particle hit thus requires more noise charge to drive the storage node through a larger swing to flip the state of the cell. *This directly translates into a higher immunity to SER.* In a conventional CMOS SRAM cell, lowering the BL precharge voltage lowers the '1' storage node voltage during a read access, due to a voltage divider between the precharged BL and the source terminal of the pull-up PFETs. The '1' storage voltage deteriorates very rapidly with lower BL precharge voltages [7] due to the higher on-resistance of the pull-up PFETs compared to the pull-down NFETs, making it necessary in conventional CMOS SRAM cells and for the cells reported in [12-14] to precharge BLs high. *High BL precharge voltages restrict potential opportunities to improve BL delay by simultaneously driving the BL pair in opposite directions during a read access. High BL precharge voltages also require more energy to recover the BL voltage after a write operation or after extended periods of cell inactivity when a clocked (AC) BL load is used.* Clocked BL loads are typically used in high performance SRAMs so that the minimum geometry cell transistors do not have to fight DC BL loads when pulling the BL down during a read access. In the SP-DT SRAM cell, pulsing the source terminals of the pull-up PFETs ensures enough room for voltage drop across the pull-up PFETs when the BL pair is precharged to a low, non-zero voltage ( $V_{dd}/3$ ). The sum of the BL charge and discharge currents (effective read current) of the SP-DT SRAM cell, are double that seen in a conventional cell with identical cell transistor geometries (Fig. 2a). Since the SL and the PL are triggered by  $V_{dd}$ - $V_{ss}$  transitions of the WL, unconventional drivers (Fig. 3 a, b) are required to sense the WL transitions and drive the SL and PL to voltages outside the  $V_{dd}$ - $V_{ss}$  range (Fig. 4).

### 3. Subthreshold leakage improvements

Thresholds are lowered to their nominal values by driving the substrate terminals to  $V_{dd}$  and  $V_{ss}$  when the WL is selected. This technique requires a triple-well process where all of the N channel devices in cells accessed by a common WL are isolated and share a common tub. The same requirements apply to the p-channel devices as well. The substrate-source reverse bias may be as high as  $V_{dd}$ , which raises the device threshold voltages by 100 mV lowering the leakage currents by over an order of magnitude (Fig 5). Special drivers (Fig. 6a, b) triggered by WL transitions are required again to drive the substrate terminals of cell transistors outside the  $V_{dd} - V_{ss}$  range (Fig 7). These drivers may require additional processing since they are driven by larger voltages than those seen by cell transistors. The substrate terminal drivers are loaded by

junction capacitance of each terminal, which is smaller than the two gate-input capacitance seen by the WL driver. This permits the substrate to respond at about the same time as the WL, causing the device thresholds to be at their desired dynamic values when the WL drives the cells.

### 4. Overhead in delay, power and processing

Since the SL, PL, SubP and SubN lines are driven by circuitry after the arrival of the WL signal, the additional delays introduced reduce the gains obtained by doubling the cell read current. The BL response (Fig. 8) shows an improvement in WL-BL delay of 33% in the SP-DT SRAM cell over a conventional cell with identical cell transistor geometries the above overhead in delay notwithstanding. Additional dynamic power is dissipated in driving the SL, PL, SubN and SubP lines. Some of this is recovered by the energy efficient low BL precharge voltage and the overheads may be kept at a minimum with the commonly used hierarchically divided WL architecture [9], with short WLs. Since the SP-DT cells do not require  $V_{dd}$  and Gnd rails, the overhead in cell area comes from only two sources: additional area consumed by separate source and substrate contacts and requirements of a triple-well process impose an additional overhead on cell area as well. However, since the SP-DT cell with minimum geometry transistors is substantially more stable than a conventional SRAM cell, this overhead in cell area may be kept at a minimum by using unity cell ratios. The 1999 Int'l Roadmap for Semiconductors (ITRS) projects multiple supply voltage requirements for analog and RF blocks in a heterogeneous system-on-a-chip making the availability of multiple power supplies for SP-DT cells a lesser concern.

### 5. Summary and Conclusions

A novel CMOS SRAM cell architecture that improves stability by over 70%, WL-BL delay by 33%, BL power by over 50% and subthreshold leakage by over an order of magnitude is reported. The cell requires a marginal overhead in cell area and wiring for its quad-rail power supplies. These improvements are achieved by pulsing the source and substrate terminals of the cell transistors selectively outside the  $V_{dd} - Gnd$  range. This new architecture considers holistically all of the challenges facing conventional scaled CMOS SRAMs of increased leakage, slower BL response and increasing instabilities.

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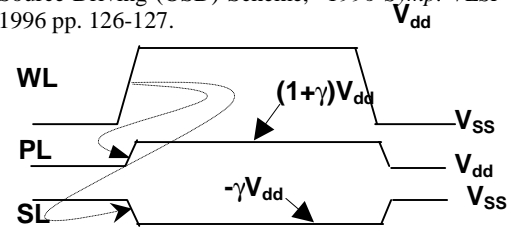
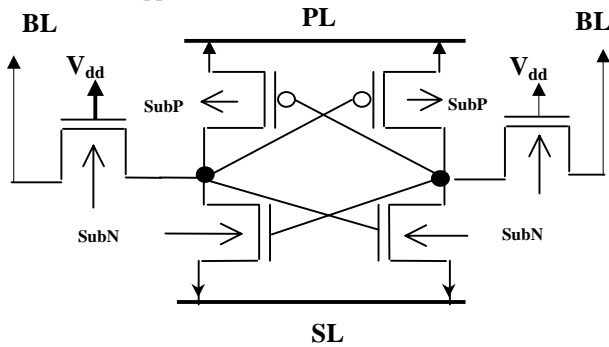


Figure 1 a, b (at left and above): Circuit schematic and timing diagram of a source-pulsed DT CMOS SRAM cell.

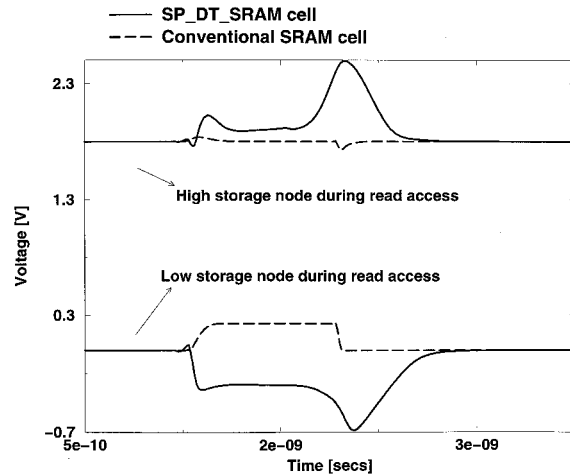
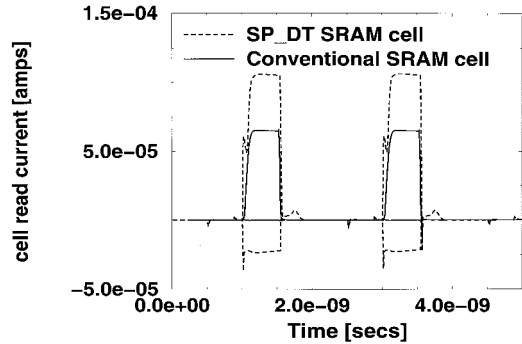


Figure 2a, b (above and at right): HSPICE simulations of cell read current and cell storage node voltage for an industrial 0.18  $\mu\text{m}$  CMOS process.

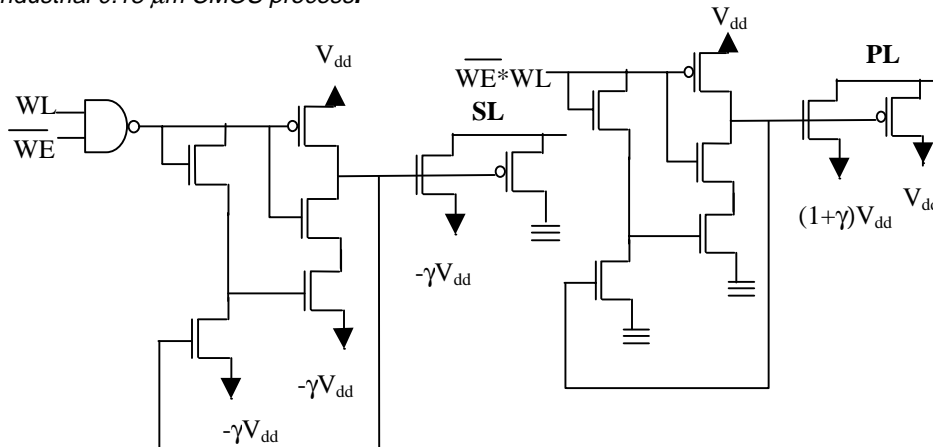


Figure 3 a, b (at left): Circuit schematics of Source Line (SL) and Power Line (PL) drivers. Drivers pulse the SL and PL only during a read access. Devices used in drivers may need additional processing to permit higher gate-source and drain-source voltages.

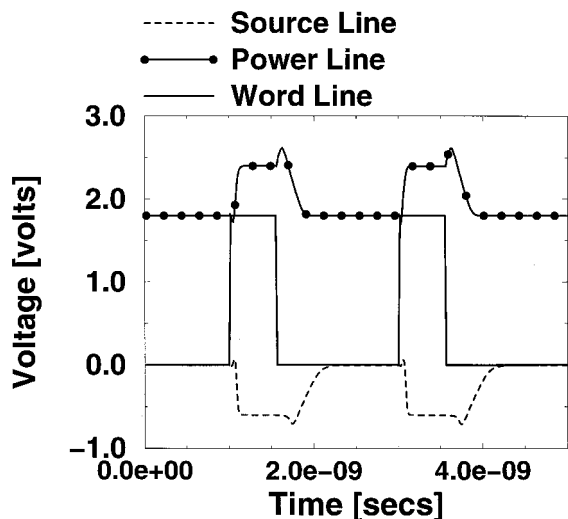


Figure 4: HSPICE simulations of PL and SL waveforms triggered by WL transitions

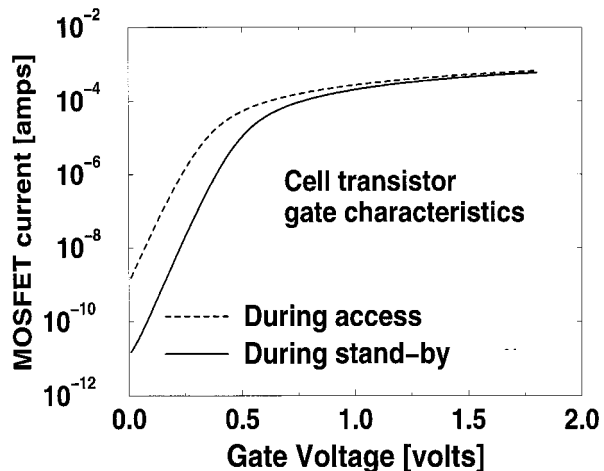


Figure 5: HSPICE subthreshold current characteristics in cell transistors by dynamically reverse biasing source-body junctions by  $V_{dd}$

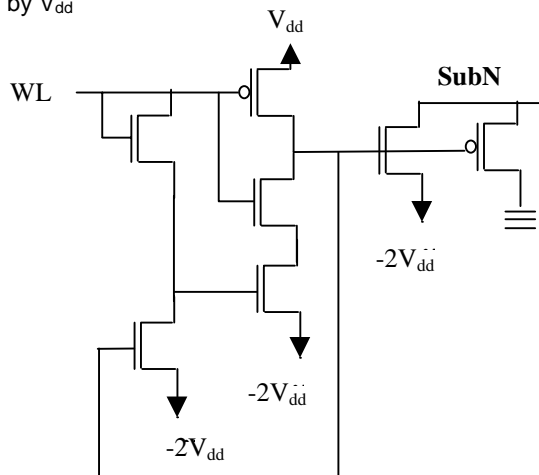
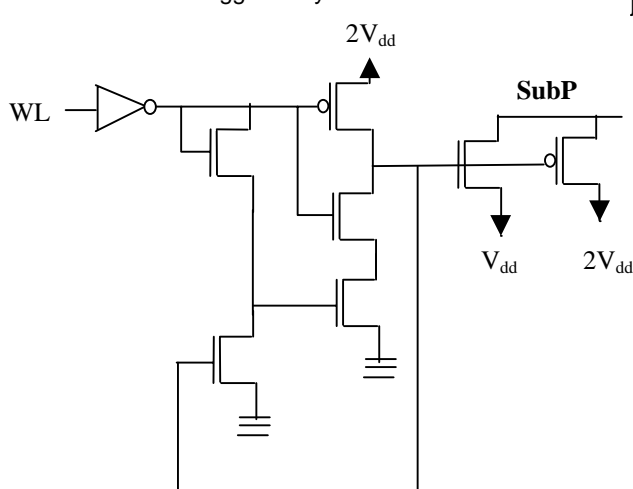


Figure 6 a, b: Circuit schematics of PFET and NFET substrate terminal drivers. Drivers pulse the SubP and SubN substrate terminals of N and P devices shared by all cells accessed by a common WL, only during a read access.

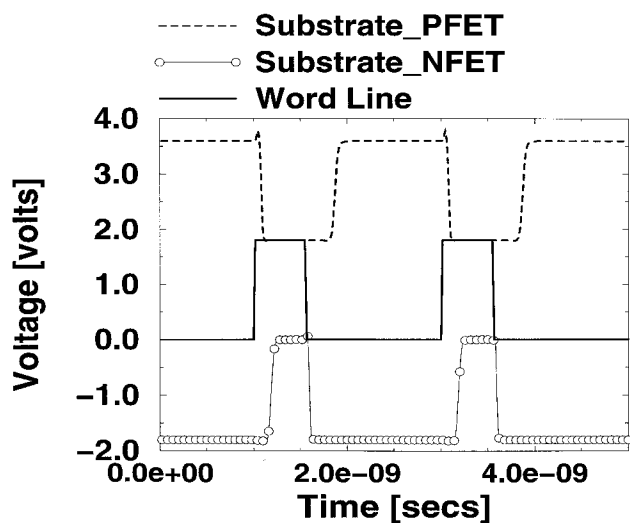


Figure 7: HSPICE simulations of waveforms at the substrate terminals of the PFETs and NFETs triggered by WL transitions for SP\_DT SRAM cells.

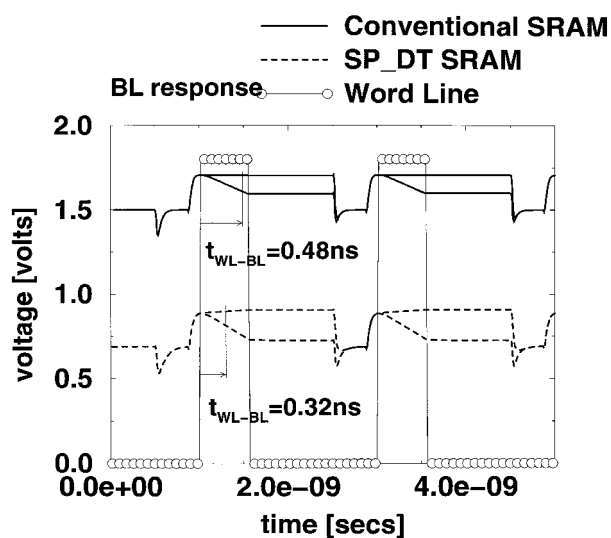


Figure 8: Comparison of BL response in SP\_DT SRAM with a conventional 6T SRAM cell. Identical cell transistor geometries for both cases