Projections for High Performance, Minimum Power CMOS ASIC Technologies: 1998 – 2010

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***Abstract*:- Circuit design techniques minimizing total power drain of a static CMOS gate for a prescribed performance and an operating range of temperatures are employed to project supply voltages, power densities, device threshold voltages & critical path device channel widths for CMOS ASIC technology generations listed in the 1994 NTRS (National Technology Roadmap for Semiconductors) upto the year 2010. These projections are consistent with 1994 NTRS technology and cycle time forecasts and use physical and stochastic models that tightly couple together the device, circuit and system levels of the CMOS ASIC design hierarchy. Verified by HSPICE and actual microprocessor implementations, these models project optimal supply voltages for 0.25 – 0.07μm generations to scale from 900mV to 500mV and power densities to increase from 3 W/cm^2 to 10 W/cm^2 in wire limited high performance CMOS ASIC systems.**

I. Introduction

Reduction of total power dissipation in CMOS circuit designs for ASICs, microprocessors and semiconductor memories has become a key design constraint for future microelectronic systems [1]. This is motivated not only by high performance requirements in a portable environment where the size, weight and lifetime of batteries are critical but also by heat dissipation and packaging issues in larger desktops and parallel machines as well [1,2]. Scaling the supply voltage reduces all components of power drain in digital CMOS circuits and is widely accepted as one of the most effective ways to reduce total power dissipation [1,2,3,4,5] as it is effective globally across the entire system and not just limited to a sub-circuit or sub-block.

Parallelism, system-on-a-chip	**System**
Interconnect architectures, transistor sizing, dynamic logic styles	**Circuit**
SOI, threshold scaling, low temperature operation	**Device**

Figure 1: CMOS design hierarchy for low power

Opportunities to minimize total power drain by scaling operating voltages without incurring a loss in performance exist at each level of the CMOS design hierarchy (Figure 1) and yield the largest power savings when considered simultaneously. A generic static CMOS datapath in a wire-limited ASIC environment is modeled as a chain of critical path gates and conjointly optimized across all levels of the hierarchy using a set of tightly coupled device, circuit and system models (Figure 2) along with 1994 NTRS projections [6] for high performance ASIC chips.

Multiple & single datapath model	**System**	**Clock frequency, Chip size, number of gates, Rent's exponent**
Stochastic wiring distributions	**Circuit**	
Transregional MOSFET model	**Device**	**Minimum feature size, gate oxide thickness, material properties**

Figure 2: A generic static CMOS data-path model and NTRS, stochastic and physical input parameters

II. Transregional MOS device and circuit models

Compact transregional MOSFET models [7], [8] describe device behavior in the sub-threshold, saturation and linear regions of operation and provide continuous and smooth transitions across region boundaries. These models include high field effects on carrier mobilities and are valid for deep sub-micron device geometries. They are physical, do not use fitting parameters and are consequently useful in projecting device performances for future MOS technology generations.

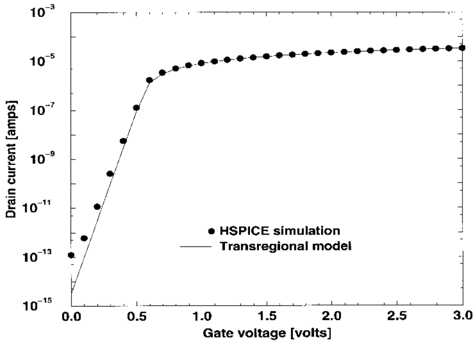

Figure 3: Comparison of Transregional drain current model with HSPICE simulations for 0.25μm CMOS

The transregional nature of the model permits accurate estimation of CMOS circuit performance and stand-by power drain at very low supply voltages – above and below the device threshold voltage. Figures 3 & 4 show HSPICE verification of the transregional models for a 0.25μ CMOS technology.

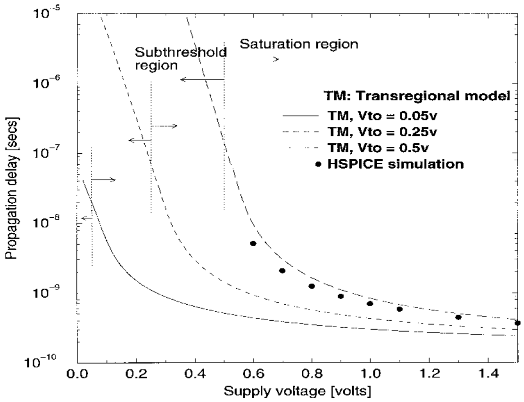

Figure 4: Comparison of static gate performance predicted by transregional model with HSPICE at low voltages for 0.25μm CMOS

III. *Critical path and wiring models for CMOS ASICs*

The performance of a generic static CMOS data-path is modeled assuming a chain of critical path gates, (Figure 5) whose wiring loads are determined from stochastic interconnect distributions (Figure 6) of a random logic network, derived recursively using Rent's rule [9]. In logic-intensive CMOS ASIC chips, packing densities are interconnect limited [10] where the effective size of a logic gate is determined by its wireability [11]. The gate pitch is estimated by dividing chip size by gate count and is then multiplied with the average interconnect length obtained from the distribution to calculate the wiring capacitance driven by each critical path gate. Chip size, gate pitch, average interconnection length and the wiring capacitance are listed in Table 1 for each of the 1994 NTRS technology generations.

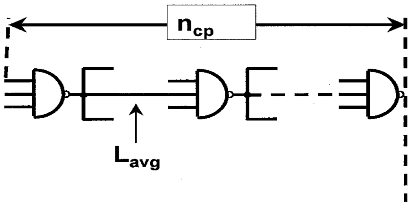

Figure 5: Critical path model

TABLE 1: Average wire lengths using NTRS projections of ASIC die size and transistor count (1997 NTRS data in italics)

Year	F (μm)	T_{ox} (A)	Chip size, cm^2	N_{gates} ($x10^6$)	Gate pitch GP (μm)	L_{avg} (GP)	Cw (fF)
1998	*0.25*	60	*6.6*	*4.4*	*12.25*	11.89	87.4
2001	*0.18*	50.5	*7.5*	*8.75*	*9.25*	13.00	72.2
2004	*0.13*	42.4	*9.0*	*18.00*	*7.07*	14.25	60.4
2007	*0.10*	35.7	*11.0*	*45.83*	*4.89*	16.01	47.1
2010	*0.07*	30	*14.0*	*93.33*	*3.87*	17.47	40.6

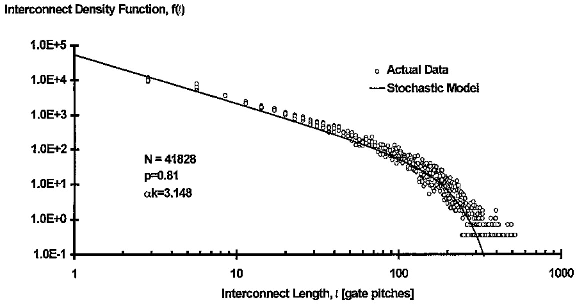

Figure 6 [9]: Stochastic wiring distribution comparison with an actual microprocessor implementation

The supply voltage, cycle time, NFET & PFET channel widths of critical path gate devices, wiring loads, device threshold voltage and range of operating temperature are analytically coupled together to explore trade-offs for minimum power in supply voltage, channel width and threshold voltage design space for a prescribed cycle time (Figures 7 & 8). The coupled cycle time model includes the competing temperature dependent effects of threshold voltage reduction and carrier mobility degradation on performance. Cycle time requirements are met at the temperature within the operating range that corresponds to the lowest performance

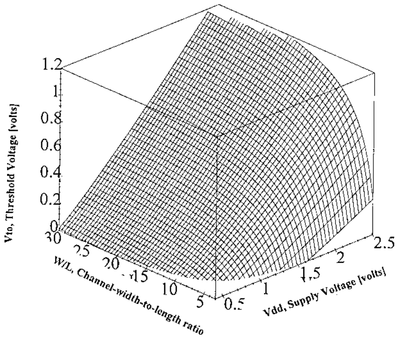

Figure 7: V_{dd}, (W/L) and V_{to} interdependence for a constant cycle time of 2.22ns for 0.25mm CMOS

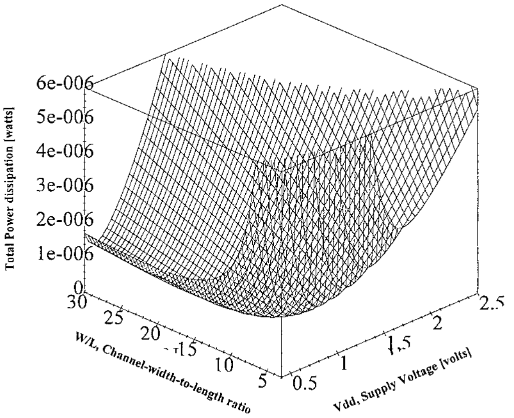

Figure 8: Total power dissipation dependence on V_{dd} and (W/L) for a constant cycle time. Threshold voltage varies along surface to maintain constant cycle time

IV. *Minimum power CMOS circuit design*

Operating voltages are scaled until the rate of change of static and dynamic power are equal. Further scaling of voltages beyond this point to meet a required performance increases total power drain due to a dominating static component (Figure 9,10). Channel widths of critical path gate devices are increased to compensate for performance loss asymptotically for lower V_{dd} until increases in total power due to larger gates dominate over reductions in total power due to smaller V_{dd} [2] (Figure 11).

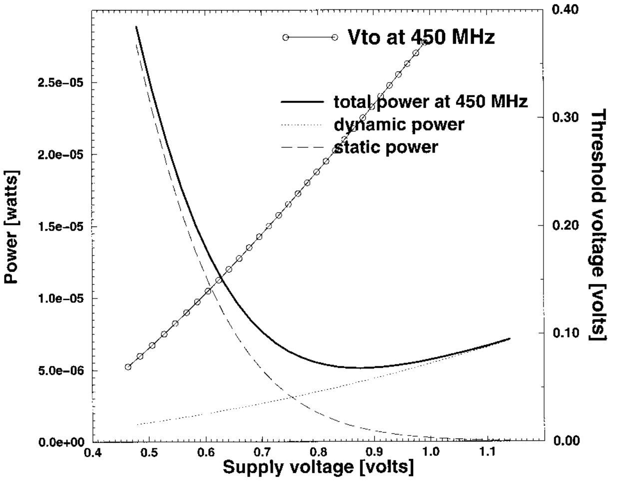

Figure 9: Dependence of total power on supply voltage at a constant cycle time for 0.25μm CMOS.

PFETs and NFETs have different carrier mobilities, threshold voltage dependencies on temperature and critical fields at which their carrier velocities saturate. While minimizing total power dissipation per gate, N and P channel devices are required to have the same threshold voltages and switching speed at any given supply voltage by constraining the device (W/L) ratios. Simultaneous solutions, corresponding to minimum power, of threshold voltage, critical path gate device channel widths and supply voltage for a given cycle time yield reductions in total power to less than a fourth of the NTRS projections [12]. Optimal supply voltages lie inside the 450mV - 900mV range for logic circuits.

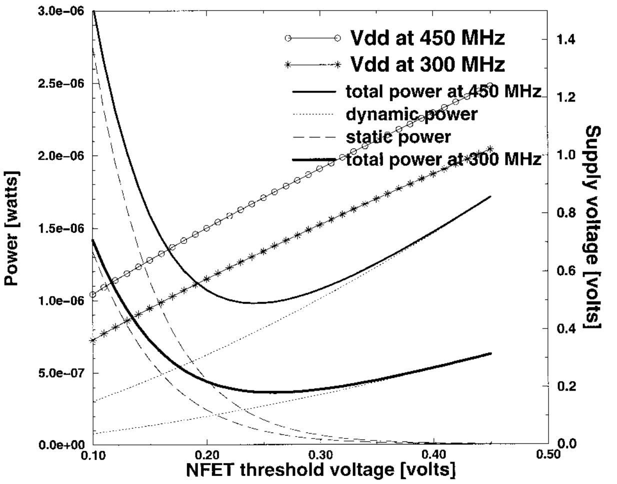

Figure 10: Dependence of total power on cycle time and device threshold voltage for 0.25μm CMOS. Supply voltage varies and is constrained to maintain constant cycle time

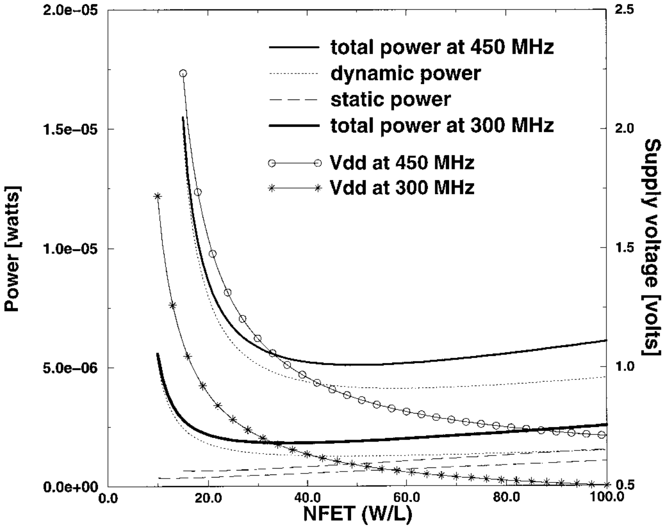

Figure 11: Dependence of total power on cycle time and (W/L) for 0.25μm CMOS. Supply voltage varies and is constrained to maintain constant cycle time

Table II lists the optimal device and circuit design parameters for minimum power. Table III and Figures 12 & 13 compare the supply voltage projections and power densities by the NTRS with those corresponding to minimum power designs.

Table II: Optimal circuit design, ΔT=100 K

Year	**1998**	**2001**	**2004**	**2007**	**2010**
F_c(MHz)	*450*	*600*	*800*	*1000*	*1100*
F(μm)	*0.25*	*0.18*	*0.13*	*0.10*	*0.07*
T_{ox} (A)	*60*	*50.5*	*42.4*	*35.7*	*30*
C_w (fF)	87.4	72.3	60.4	47.1	40.6
V_{ddopt} (V)	0.87	0.74	0.66	0.60	0.50
V_{topt} (V)	0.24	0.25	0.27	0.28	0.29
(W/L)n	50	59	72	73	78
(W/L)p	67	77	91	90	90

Table III: NTRS Vs minimum power projections of supply voltage and power density

year		**1998**	**2001**	**2004**	**2007**	**2010**
F_c (MHz)		*450*	*600*	*800*	*1000*	*1100*
V_{dd} (V)	**NTRS**	*2.5-1.8*	*1.8-0.9*	*0.9*	*0.9*	*0.9*
	Min power	0.87	0.74	0.66	0.60	0.50
Power Density (W/cm^2)	**NTRS**	*19.1*	*17.9*	*15.6*	*15.4*	*12.7*
	Min power	3.41	4.61	6.44	10.57	9.93

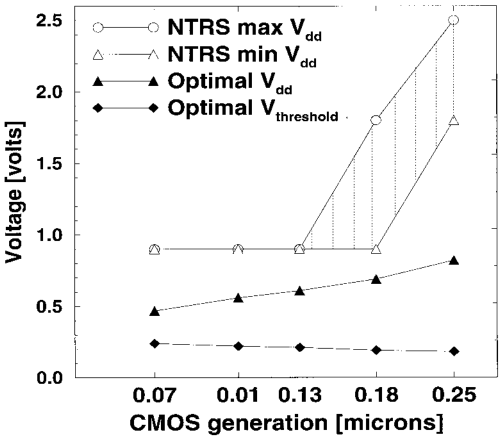

Figure 12: Comparison of NTRS projections for supply voltage with optimal supply voltages corresponding to minimum power

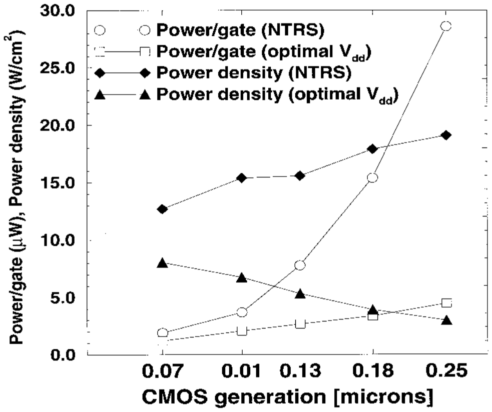

Figure 13: Comparison of NTRS projections of power dissipation per gate and power density with projections corresponding to minimum power

V. Conclusions

Conjoined optimizations for minimum power across the CMOS design hierarchy are used to project the minimum supply voltage, minimum power dissipation per gate and power densities for high performance CMOS ASIC generations listed in the NTRS. These projections are consistent with performance and technology forecasts by the NTRS such as clock cycle time, transistor count per chip and chip size.

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