Analytical Models for Coupled Distributed RLC Lines with Ideal and Non-Ideal Return Paths

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Abstract

New analytical models that describe distributed RLC interconnects with ideal and non-ideal return paths are used to optimize the time delay and crosstalk of a state-of-the-art high-speed global interconnect structure that incorporates co-planar ground lines such that the delay and crosstalk are reduced by 12% and 38%, respectively.

I. Introduction

Due to rapidly increasing clock frequencies, interconnect inductance is significantly affecting wire delay and crosstalk. High-speed *off*-chip interconnects have nearly *ideal* return paths because of nearby ground planes, but high-speed *on*-chip interconnects have *non-ideal* return paths because of nearby orthogonal lines. This paper presents new analytical models that describe interconnects with ideal and non-ideal return paths. Furthermore, these models are used to optimize the time delay and crosstalk of state-of-the-art high-speed global interconnect structures that incorporate co-planar ground lines [1,2].

II. Ideal Ground Plane Case

For a single, two and three coupled distributed RLC lines a rigorous solution to the delay and crosstalk problems has been found [3]. For the five coupled line case, by finding the eigen vectors of the capacitance matrix, three new modes of propagation are found which yield a rigorous solution for five conductors. It has been assumed that the two near aggressors as well as two far aggressors have equal potential. All three modes propagate with the speed of light in the dielectric and therefore, the equivalent inductance of each mode can be found in accordance with its equivalent capacitance. Fig. 1 shows a comparison between HSPICE simulations and the analytical expressions. Fig. 2 compares the worst case crosstalk in two, three, and five coupled line models and shows that the impact of far aggressors is negligible in the ideal return path case (less than 4%). The worst case peak crosstalk in the five line case is

$$V_{peaknoise}=\begin{pmatrix} 0.8\dfrac{Z_{com}}{Z_{com}+R_{tr}}e^{-\frac{rl}{2Z_{com}}}-0.4\dfrac{Z_{dif1}}{Z_{dif1}+R_{tr}}e^{-\frac{rl}{2Z_{dif1}}} \\ -0.4\dfrac{Z_{dif2}}{Z_{dif2}+R_{tr}}e^{-\frac{rl}{2Z_{dif2}}} \end{pmatrix}V_{dd}, \qquad (1)$$

where $Z_{com}=\dfrac{\sqrt{\varepsilon_r}}{c_g c_0}$, $Z_{dif1}=\sqrt{\varepsilon_r}\Big/\left(c_g+\dfrac{5+\sqrt{5}}{2}c_m\right)c_0$, $Z_{dif2}=\sqrt{\varepsilon_r}\Big/\left(c_g+\dfrac{5-\sqrt{5}}{2}c_m\right)c_0$, c_0 is speed of light in vacuum, c_g and c_m are ground and mutual capacitances per

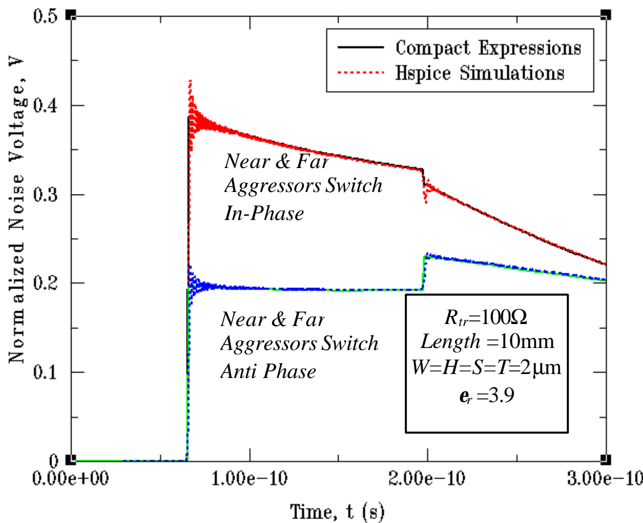

Figure 1: HSPICE verification of the compact model for five coupled RLC lines over a ground plane. Crosstalk over the middle quiet line is shown when near and far aggressors switch in and out of phase.

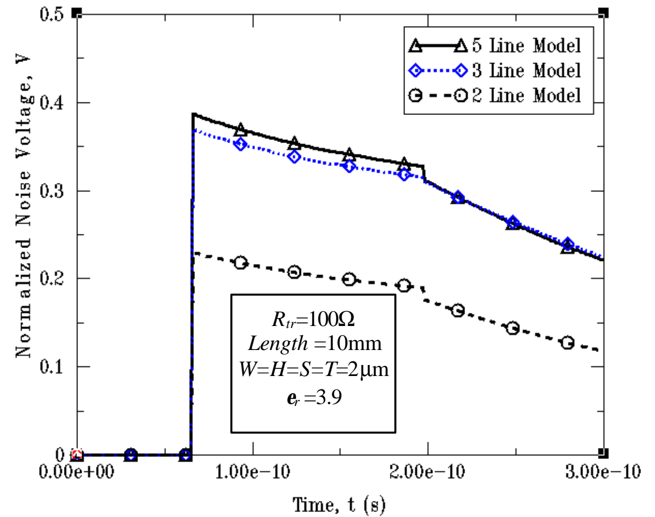

Figure 2: Comparing the induced noise on the quiet middle line with 1, 2 and 4 aggressors over a ground plane.

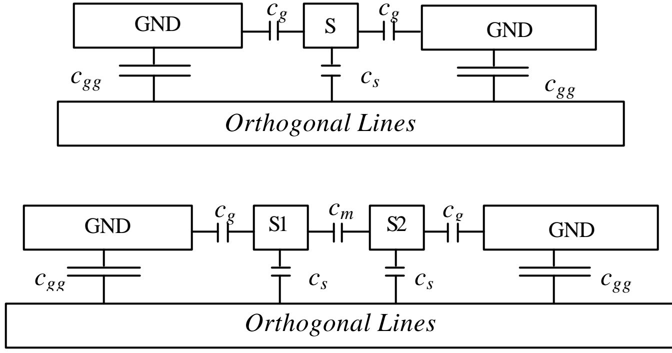

Figure 3: The cross-section of single and double sided shielding structures over orthogonal lines. All width, spacing and thickness dimensions are equal to 2μm except the ground lines, which are 5 times wider.

unit length, respectively and l is the length of interconnects.

III. Non-ideal Return Path Case

Fig. 3 shows the cross-section of one and two signal lines between two ground lines when instead of the ground plane there are orthogonal lines. At high frequencies, the return current is mainly through the nearby ground lines due to the proximity effect, especially, if the ground lines are wide enough [4]. The structures of Fig. 3 are very similar to the periodic structures, which are very common in microwave circuits [5] and since the distance between the lower orthogonal lines is much smaller than the signal wavelength, these structures can be considered as smooth transmission lines with excessive capacitance [6]. The orthogonal lines have no impact on inductance values and therefore, inductance values can be found by neglecting the orthogonal lines.

A. Single Line between Ground Lines

The inductance per unit length can be found by

$$l_s = \varepsilon_r / (c_0^2 c_g). \tag{2}$$

Having the capacitance and inductance values, the waveform of the single line between ground lines can be found using either the rigorous or low-loss approximate solutions [3]. The propagation speed of the traveling wave is

$$v = \frac{1}{\sqrt{1 + c_s/c_g}} \times \frac{c_0}{\sqrt{\varepsilon_r}}, \tag{3}$$

where c_s is the capacitance per unit length of the signal line to the lower orthogonal lines. This propagation speed is typically 10% to 20% slower than the speed of light in the same dielectric (Fig. 4). For the top most layer (x) c_s is the capacitance to just the lower orthogonal interconnects. For the lower layer (y), however, c_s consists of the capacitance to both lower and upper orthogonal layers. This makes the wave speed different in x and y directions.

B. Two Lines between Ground Lines

For the two signal line case, each signal line and its nearby ground line can be considered as a transmission line. The self and mutual inductances can be found by

$$\begin{bmatrix} l_s & l_m \\ l_m & l_s \end{bmatrix} \begin{bmatrix} c_g + c_m & -c_m \\ -c_m & c_g + c_m \end{bmatrix} = (\varepsilon_r / c_0^2)[I], \tag{4}$$

using the capacitance values when orthogonal lines don't exist. The total capacitances of the lines in common and differential modes are found by

$$c_{com} = c_g + \frac{c_s c_{gg}}{c_s + c_{gg}}, \tag{5}$$

and

$$c_{dif} = c_g + 2c_m + c_s, \tag{6}$$

respectively. Knowing the solutions of common and differential modes, any switching pattern can be solved. Fig. 5 shows how well the mentioned model matches with HSPICE simulations for both active and quiet lines. For

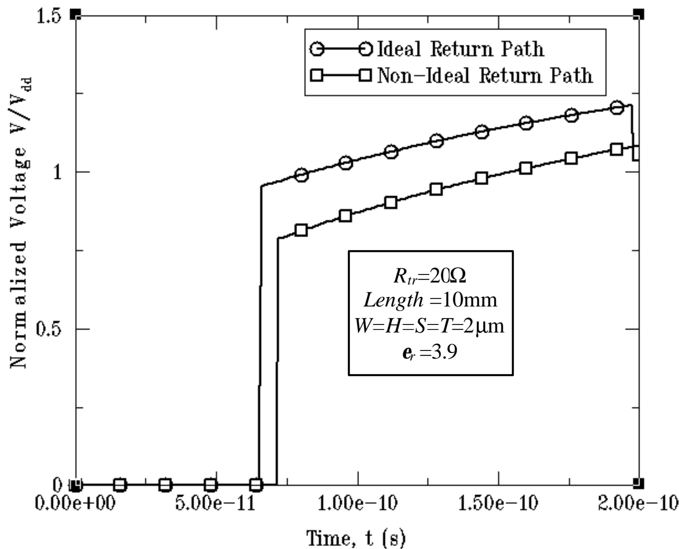

Figure 4: Comparing the time-of-flight in the ideal and non-ideal return path cases. In the non-deal case ToF is larger.

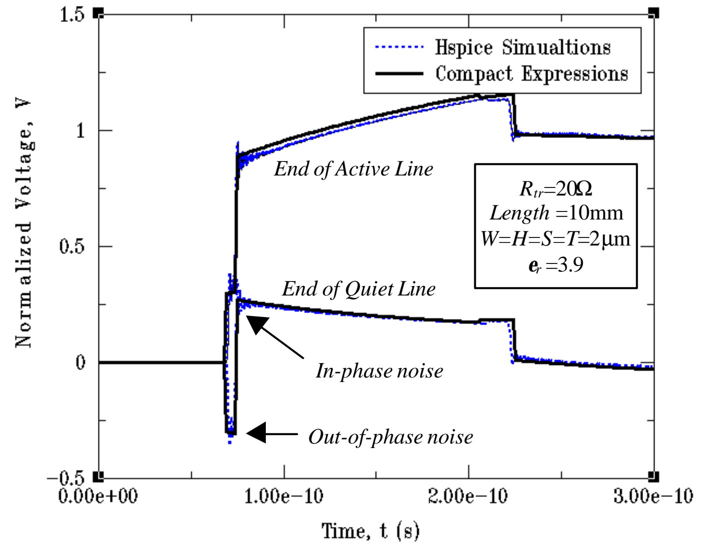

Figure 5: HSPICE verification of the compact models for two signal lines over orthogonal lines.

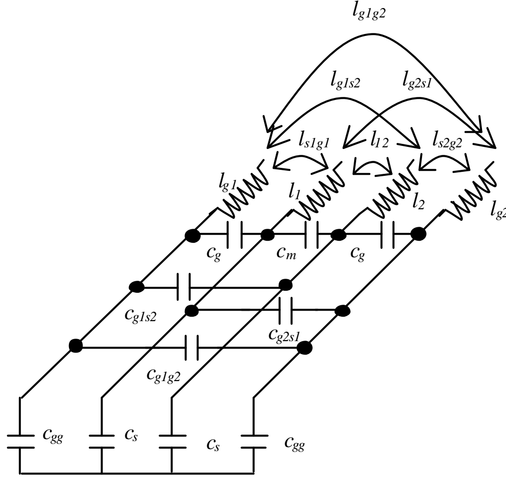

Figure 6: A segment of the equivalent circuit used for HSPICE simulations. 1000 segments are used in all simulations.

HSPICE simulations all self and mutual inductance values shown in Fig. 6 are found by RAPHAEL [7]. The differential mode is always faster than the common mode and therefore, an out-of-phase pulse appears at the end of the quiet line for a time proportional to the ratio of the vertical to horizontal capacitances (c_s / c_g). Therefore, for the higher aspect ratios, the out-of-phase pulse is narrower and if it is too narrow it might not have enough energy to cause false switching or damage the gate of the receiver.

A low-loss approximation evaluates the peak crosstalk of the two-line case very accurately. Peak out-of-phase noise is

$$V_n^- = -\frac{Z_0^-}{Z_0^- + R_{tr}} e^{-\frac{rl}{2Z_0^-}}, \tag{7}$$

and peak in-phase noise is

$$V_n^+ = -\frac{Z_0^-}{Z_0^- + R_{tr}} e^{-\frac{rl}{2Z_0^-}} + \frac{Z_0^+}{Z_0^+ + R_{tr}} e^{-\frac{rl}{2Z_0^+}}, \tag{8}$$

where

$Z_0^+ = \sqrt{\frac{l_s + l_m}{c_g + c_s}}$ and $Z_0^- = \sqrt{\frac{l_s - l_m}{c_g + 2c_m + c_s}}$ are the common and differential mode characteristic impedances, respectively.

Fig. 7 shows the peak crosstalk versus the resistance per unit length of the lines. When the line resistance is low, the out-of-phase noise is dominant, and decreasing the resistance increases the noise exponentially. Therefore, this region should be avoided especially since the delay does not improve for very small line resistance. The minimum permissible resistance per unit length, r_{min}, can be found by equating in-phase and out-of-phase noise voltages. Neglecting the driver resistance ($R_{tr} \approx 0$), the exact expression for r_{min} can be approximated by

$$r_{\min} = \frac{\sqrt{\varepsilon_r}}{l c_0 c_m} \ln 2, \tag{9}$$

where l is length of the interconnects. For $r > r_{min}$, the maximum peak crosstalk can be found by differentiating (8). The result can be approximated by

$$V_{peak,\max} = \frac{\pi}{4} \frac{c_m}{\sqrt{c_g (c_g + c_s)} + c_m}, \tag{10}$$

with less than 3% error for all typical on-chip interconnects dimensions. The resistance per unit length at which the maximum crosstalk happens is

$$r_{\max} = \frac{\sqrt{\varepsilon_r}}{l c_0 c_m} \ln\left[1 + \frac{2c_m}{\sqrt{c_g (c_g + c_s)}}\right]. \tag{11}$$

Because driver resistance is assumed to be zero, (10) gives the worst-case crosstalk and therefore, can be used to design a robust interconnect structure independent of the driver resistance. It is worth noting that in both (9) and

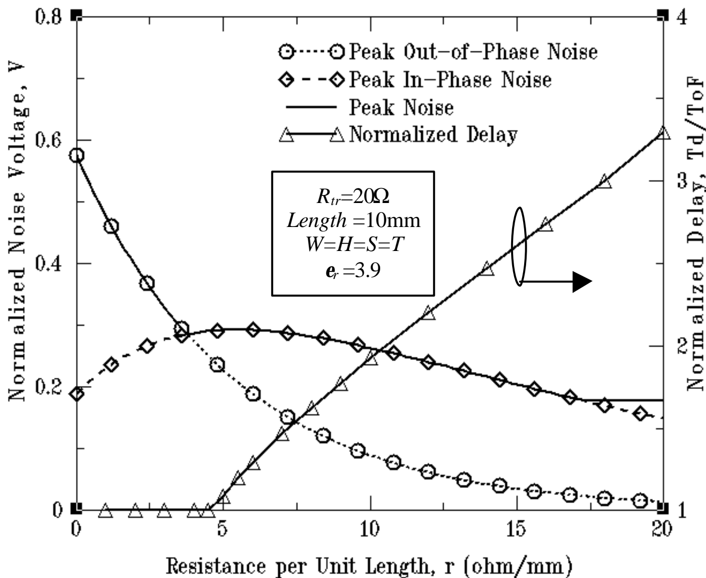

Figure 7: The induced in and out of phase noises over the quiet line and normalized delay versus the resistance per unit length for the two-line case.

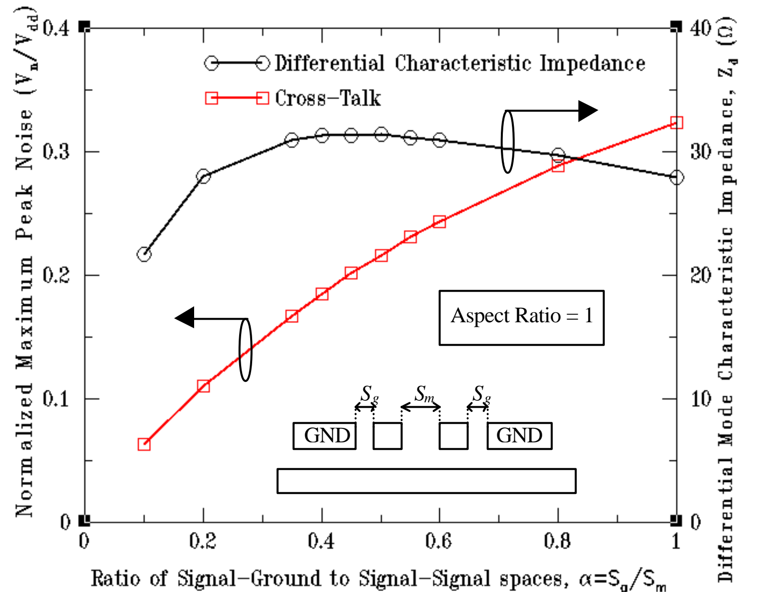

Figure 8: The maximum peak crosstalk and the differential mode characteristic impedance versus the ratio of signal-ground to signal-signal spaces.

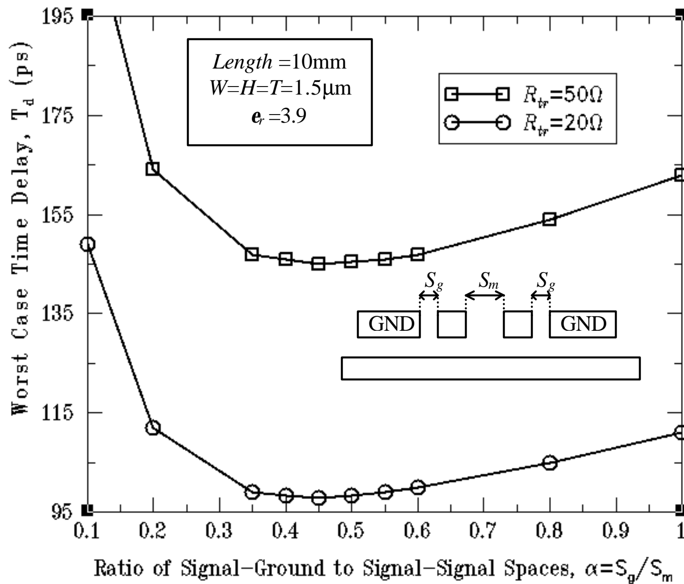

Figure 9: Worst case time delay versus the ratio of signal-ground to signal-signal spaces.

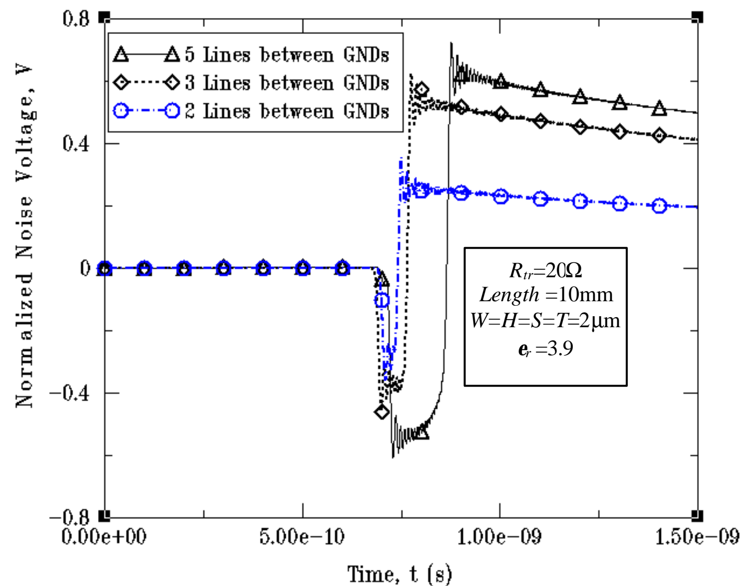

Figure 10: The HSPICE simulations for the worst case cross-talk on the middle quiet line when there are 2, 3 and 5 signal lines between the ground lines.

(11) the resistance per unit length, *r*, and the length, *l*, are interchangeable. This means that if the cross-section of interconnects is fixed then there is a minimum length that should be avoided (given by (9)) and there is a specific length (given by (11)) at which the maximum crosstalk happens.

Two signal lines between ground lines are widely used in high-speed microprocessors at the top layer of interconnects [1, 2]. The derived models are used to optimize the delay and also decrease the crosstalk in the two line case. Fig. 8 shows the maximum peak crosstalk and also the characteristic impedance in differential mode versus the ratio of ground-signal to signal-signal spaces, α, when the aspect ratio of wires is 1. The higher the characteristic impedance the smaller the attenuation, and therefore, a smaller delay is achieved if delay is not time-of-flight (ToF) limited. The optimum value for α is 0.45, since it minimizes the worst case delay (Fig. 9) and also limits the crosstalk to $0.2V_{dd}$. In this way the worst case delay and crosstalk are reduced by 12% and 38%, respectively, compared to equal spacing case (α=1) with no penalty. In addition, α=0.45 results in the smallest delay independent of the aspect ratio. However, for larger aspect ratios α should be a little smaller to have $0.2V_{dd}$ crosstalk (e.g. α=0.4 for aspect ratio of 2).

C. More than Two Signal Lines between Ground Lines

Fig. 10 compares the worst case crosstalk for two, three and five signal line cases and shows that unlike the ideal return path case, far aggressors have a large impact and crosstalk is increased by 30% from the three to five line case. Hence, due to large crosstalk it is not feasible to have more than two signal lines between the ground lines if the inductive effects are dominant. For similar dimensions, the worst case crosstalk of the five conductor case is 35% larger than the case in which the lower orthogonal lines are substituted by a ground plane.

IV. Conclusions

This paper presents new analytical models that describe interconnects with ideal and non-ideal return paths. A new five conductor model illustrates that far aggressors have negligible impact on the worst-case crosstalk when ideal ground planes are present. However, it is shown that non-ideal return paths can significantly increase signal crosstalk because: 1) far reaching inductive coupling is increased due the lack of ground planes, and 2) an out-of-phase noise pulse is induced in a quiet line due to a faster differential mode. To overcome this problem, a global interconnect structure that incorporates co-planar ground lines surrounding *two* conductors is shown to be a viable solution for high-speed top-level global interconnects. Using the new analytical models in this paper, the signal and ground line spacing for the two-line structure is optimized to reduce time delay and crosstalk by 12% and 38%, respectively.

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